



**2.5V/3.3V 2.5GHz  
DIFFERENTIAL 2-CHANNEL  
PRECISION CML DELAY LINE**

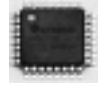
**SuperLite™  
SY55856U**

## FEATURES

- Guaranteed AC parameters over temp and voltage
  - > 2.5GHz  $f_{MAX}$
  - < 384ps prop delay
  - < 120ps  $t_r/t_f$
- Delay either clock or data
- 50ps increments
- $\pm 350$ ps total delay
- Source terminated CML outputs
- Full differential I/O
- Wide supply voltage spectrum: 2.3V to 3.6V
- Available in a tiny 32-pin EPAD-TQFP package

## APPLICATIONS

- Data communications systems
- Telecom systems
- High-speed backplanes
- Signal de-skewing
- Pulse alignment
- Digitally controlled delay lines



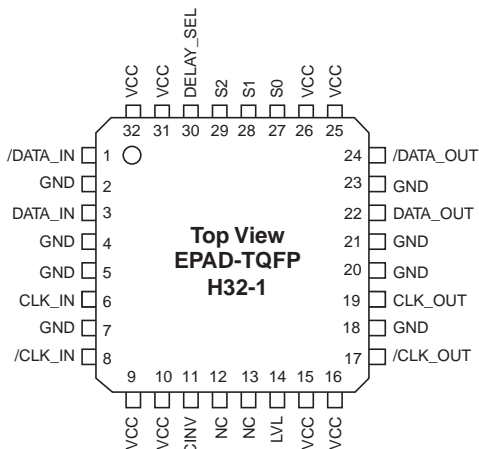
SuperLite™

## DESCRIPTION

The SY55856U is a 2.5GHz, two-channel, fully differential CML (Current Mode Logic) delay line. The device is optimized to adjust the relative delay between two channels, such as clock and data, in 50ps increments. Both inputs may be adjusted in either direction in 7 increments of 50ps, for a total adjustment range of  $\pm 350$ ps. In addition, the clock input maybe inverted through the CINV control pin.

The SY55856U inputs are designed to accept single-ended or differential CML signals. The differential CML outputs are optimized for 50 $\Omega$  loads (50 $\Omega$  source terminated), thus only requires a single 100 $\Omega$  resistor across the output pair. Output rise and fall time is an extremely fast 110ps(max) and the differential swing is 400mV. The maximum throughput of the SY55856U is guaranteed to exceed 2.5GHz (5Gbps).

**PACKAGE/ORDERING INFORMATION**



**32-Pin EPAD-TQFP (H32-1)**

**Ordering Information<sup>(1)</sup>**

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY55856UHI	H32-1	Industrial	55856U	Sn-Pb
SY55856UHITR <sup>(2)</sup>	H32-1	Industrial	55856U	Sn-Pb
SY55856UHG <sup>(3)</sup>	H32-1	Industrial	55856U with Pb-Free bar line indicator	NiPdAu Pb-Free
SY55856UHGTR <sup>(2, 3)</sup>	H32-1	Industrial	55856U with Pb-Free bar line indicator	NiPdAu Pb-Free

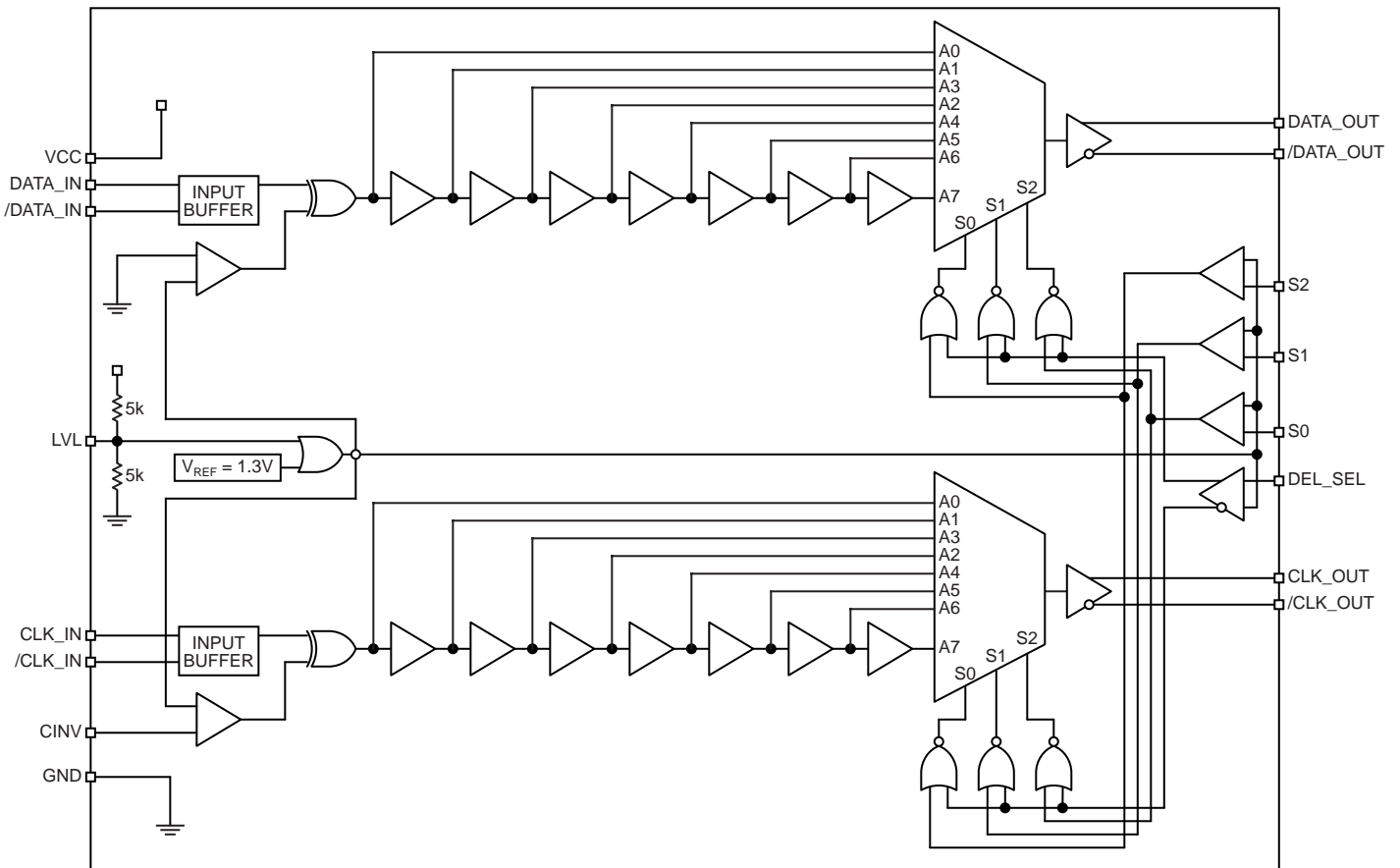
**Notes:**

1. Contact factory for die availability. Dice are guaranteed at T<sub>A</sub> = 25°C, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package recommended for new designs.

**PIN DESCRIPTION**

Pin Number	Pin Name	Pin Function
1, 3	/DATA_IN, DATA_IN	CML Input (Differential). This is one of the CML inputs, the data in signal. A delayed version of this signal appears at DATA_OUT, /DATA_OUT.
2, 4, 5, 7, 18, 20, 21, 23	GND	Ground.
22, 24	DATA_OUT, /DATA_OUT	CML Output (Differential). This is one of the CML outputs, the data output. It is a delayed version of DATA_IN, /DATA_IN.
6, 8	CLK_IN, /CLK_IN	CML Input (Differential). This is one of the differential CML inputs, the clock in signal. A delayed version of this input appears at CLK_OUT, /CLK_OUT.
17, 19	/CLK_OUT, CLK_OUT	CML Output (Differential). This is one of the CML outputs, the clock output. It is a delayed, copy of CLK_IN, /CLK_IN.
9, 10, 15, 16, 25, 26, 31, 32	VCC	Power Supply.
11	CINV	VT Input (Single Ended). This is the clock inversion select signal. This input optionally inverts the CLK_IN, /CLK_IN signal which results in an inverted CLK_OUT, /CLK_OUT. A voltage below the VT threshold results in no inversion. A voltage above the threshold value results in an inversion from the clock input to the clock output. Refer to the “VT input” section below.
14	LVL	Analog Input. This input determines what level differentiates logic high from logic low. This input affects the behavior of the CINV, S0, S1 and S2 inputs. Please refer to the “VT input” section below for more details. For the control interface, see Figure 3a. For TTL control interface, see Figure 3b.
30	DELAY_SEL	VT Input (Single Ended). CML compatible control logic. This is the delay path control input. Logic high delays the clock signal with respect to the data signal. A logic low delays the data signal with respect to the clock signal. Inputs S2, S1 and S0 control amount of delay.
27, 28, 29	S0, S1, S2	VT Input (Single Ended). CML compatible control logic. This is the delay selection control input. These three bits define how much relative delay will occur between the data and clock signals, as per the truth table shown in Table 2. For the control logic interface, see Figure 3a. For TTL control interface, see Figure 3b. S0=LSB.
12, 13	NC	No Connect.

**BLOCK DIAGRAM**



**FUNCTIONAL DESCRIPTION**

**Establishing Static Logic Inputs**

The true pin of a CML input pair is internally biased to ground through a 75kΩ resistor. The complement pin of a CML input pair is internally biased halfway between V<sub>CC</sub> and ground by a voltage divider consisting of two 75kΩ resistors. To keep a CML input at static logic zero at V<sub>CC</sub> > 3.0V, leave both inputs unconnected. For V<sub>CC</sub> ≤ 3.0V, connect the complement input to V<sub>CC</sub> and leave the true input unconnected. To make an input static logic one, connect the true input to V<sub>CC</sub>, and leave the complement input unconnected. These are the only safe ways to cause CML inputs to be at a static value. In particular, no CML input should be directly connected to ground. All NC pins in the figures below should be left unconnected.

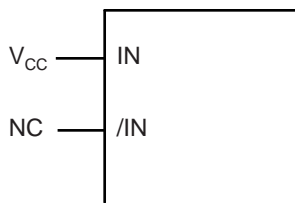
**VT (Variable Threshold) Inputs**

Five inputs to SY55856U, CINV, DELAY\_SEL, S0, S1, and S2, are variable threshold inputs. The LVL input determines

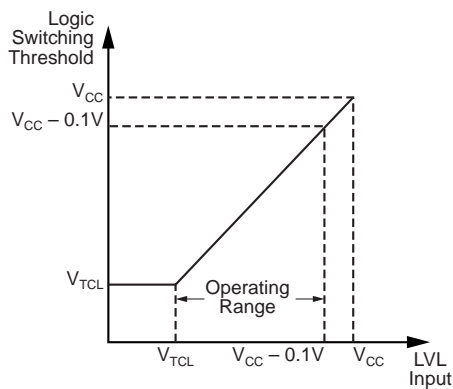
the Voltage threshold that differentiates logic high from logic low for these five inputs only. If LVL is left unconnected, the

VT inputs will switch at about  $\frac{V_{CC} + GND}{2}$  or V<sub>TCL</sub>, whichever is higher. To obtain a logic switching threshold different from this, the LVL input must be driven with the actual desired threshold voltage. The user may drive the LVL pin with any voltage between V<sub>CC</sub> - 0.1V and ground. For example, driving LVL with a voltage set at V<sub>CC</sub> - 1.3V causes the VT inputs to accept single ended PECL outputs and switch appropriately.

Note that VT inputs are internally clamped so that the threshold will not fall below VTCL Volts. Since driving the LVL input to ground causes the threshold to be somewhere between V<sub>TCL</sub> (min) and V<sub>TCL</sub> (max), it is expected that the user will keep the Voltage at the LVL pin at or above V<sub>TCL</sub> (max). Please refer to Figure 3 for clarification.

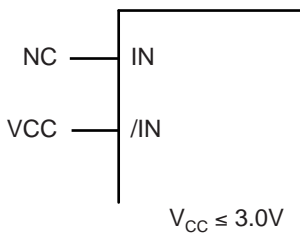
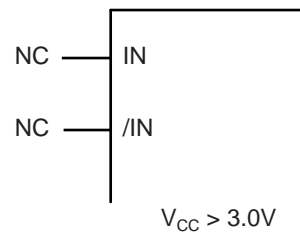


**Figure 1. Hard Wiring a Logic "1" (1)**

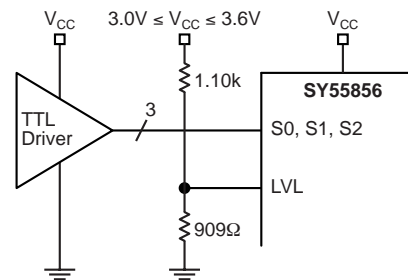


**Figure 3a. Logic Switching Threshold**

**Note 1.** IN is either the DATA\_IN or the CLK\_IN input. /IN is either the /DATA\_IN or the /CLK\_IN input.



**Figure 2. Hard Wiring a Logic "0" (1)**



**Figure 3b. Interfacing TTL-to-CML Select (CINV, DELAY\_SEL, S0, S1, S2)**

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Symbol	Rating	Value	Unit	
V <sub>CC</sub>	Power Supply Voltage	-0.5 to +6.0	V	
V <sub>IN</sub>	Input Voltage	-0.5 to V <sub>CC</sub> +5.0	V	
V <sub>OUT</sub>	CML Output Voltage	-0.5 to V <sub>CC</sub> +5.0	V	
T <sub>A</sub>	Operating Temperature Range	-40 to +85	°C	
T <sub>LEAD</sub>	LeadcTemperature (soldering, 20sec.)	260	°C	
T <sub>store</sub>	Storage Temperature Range	-55 to +125	°C	
θ <sub>JA</sub>	Package Thermal Resistance (Junction-to-Ambient) Exposed pad soldered to PCB GND pin	- Still Air	28	°C/W
		- 500lfpm	20	°C/W
θ <sub>JC</sub>	Package Thermal Resistance (Junction-to-Case)	4	°C/W	

**Note 1.** Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**CML TERMINATION**

All CML inputs accept a CML output from any other member of this family. All CML outputs are source terminated 50Ω differential drivers as shown in Figure 4. SY55856U expects its inputs to be externally terminated.

SY55856U inputs are designed to accept a termination resistor between the true and complement inputs of a CML differential input pair, as shown in Figure 4.

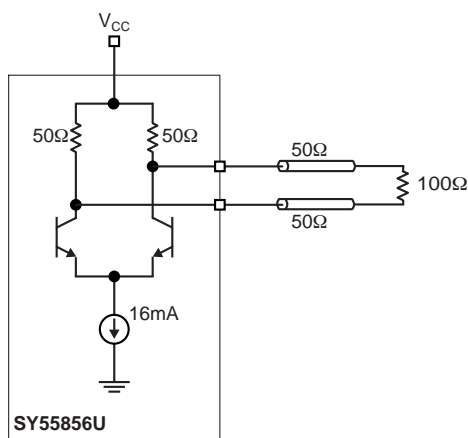


Figure 4. 50Ω Load CML Output

## TRUTH TABLES

DATA_IN	CLK_IN	CINV	DATA_OUT	/DATA_OUT	CLK_OUT	/CLK_OUT
0	0	0	0	1	0	1
0	0	1	0	1	1	0
0	1	0	0	1	1	0
0	1	1	0	1	0	1
1	0	0	1	0	0	1
1	0	1	1	0	1	0
1	1	0	1	0	1	0
1	1	1	1	0	0	1

**Table 1. Input to Output Connectivity**

S2	S1	S0	DATA_OUT (D_SEL=0) (ps)	CLK_OUT (D_SEL=1) (ps)
0	0	0	350	0
0	0	1	300	50
0	1	0	250	100
0	1	1	200	150
1	0	0	150	200
1	0	1	100	250
1	1	0	50	300
1	1	1	0	350

**Table 2. Nominal Differential Delay Values**

**Note:**

- Table 2 defines the approximate relative delay between the two paths. For example, if S2, S1, S0 = 000, and an edge appears at CLK\_IN at the same instant as an edge appears at DATA\_IN, then an edge at CLK\_OUT will appear about 350ps earlier than an edge at DATA\_OUT. That is, negative values imply CLK\_OUT being shifted early with respect to DATA\_OUT. Likewise, a positive value in the third column implies that CLK\_OUT is shifted late with respect to DATA\_OUT. Please consult the "AC ELECTRICAL CHARACTERISTICS" section for more precise delay values.

## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	T <sub>A</sub> = -40°C			T <sub>A</sub> = +25°C			T <sub>A</sub> = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V <sub>CC</sub>	Power Supply Voltage	2.3	—	3.6	2.3	—	3.6	2.3	—	3.6	V	
I <sub>CC</sub>	Power Supply Current	—	—	140	—	115	140	—	—	140	mA	No Load

## VT INPUTS DC ELECTRICAL CHARACTERISTICS

V<sub>CC</sub> = 2.3V to 3.6V; GND = 0V; T<sub>A</sub> = -40°C to +85°C<sup>(1)</sup>

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>ILVL</sub>	Analog Input <sup>(2)</sup>	V <sub>TCL</sub>	—	V <sub>CC</sub> - 0.1	V
V <sub>IHVT</sub>	V <sub>T</sub> Input High Voltage <sup>(3,4)</sup>	V <sub>SW</sub> + 0.1	—	V <sub>CC</sub>	V
V <sub>ILVT</sub>	V <sub>T</sub> Input High Voltage <sup>(3,4)</sup>	0.0	—	V <sub>SW</sub> - 0.1	V
V <sub>IST</sub>	Input Switching Threshold Differential Voltage <sup>(5)</sup>	100	50	—	mV
V <sub>TCL</sub>	Threshold Clamp Voltage	1.2	—	1.4	V

**Note 1.** DC parameters are guaranteed after thermal equilibrium has been established.

**Note 2.** The LVL input determines the voltage switching threshold that differentiates logic high from logic low for the V<sub>T</sub> inputs S0, S1, S2, DELAY\_SEL, and CINV. LVL may be driven to V<sub>CC</sub>, but this is not useful, as the V<sub>T</sub> inputs could then not get high enough to reliably indicate logic high. Also, as shown in Figure 3, the LVL input internally clamps at V<sub>TCL</sub>. If LVL is left unconnected, the V<sub>T</sub> inputs will switch at about the maximum of

$$\frac{V_{CC} + GND}{2} \left( = \frac{V_{CC}}{2} \right) \text{ and } V_{TCL}.$$

**Note 3.** V<sub>T</sub> inputs are S0, S1, S2, DELAY\_SEL, and CINV.

**Note 4.** V<sub>SW</sub> is the threshold switching voltage. It is equal to the voltage at the LVL pin, when this voltage is above V<sub>TCL</sub> (max). V<sub>SW</sub> is some value between V<sub>TCL</sub> (min) and V<sub>TCL</sub> (max) when the Voltage at the LVL pin is below V<sub>TCL</sub> (max).

**Note 5.** V<sub>IST</sub> is the voltage difference needed to guarantee a stable logic level. Logic high must be at least V<sub>IST</sub> above V<sub>SW</sub>. Logic low must be at most V<sub>IST</sub> below V<sub>SW</sub>. Thus, the minimum input swing on a given V<sub>T</sub> input pin, that is, |V<sub>IHVT</sub> - V<sub>ILVT</sub>|, must be at least 2×V<sub>IST</sub>.

## CML DC ELECTRICAL CHARACTERISTICS

V<sub>CC</sub> = 2.3V to 3.6V; GND = 0V; T<sub>A</sub> = -40°C to +85°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V <sub>ID</sub>	Differential Input Voltage	100	—	—	mV	
V <sub>IH</sub>	Input HIGH Voltage	1.6	—	V <sub>CC</sub>	V	
V <sub>IL</sub>	Input LOW Voltage	1.5	—	V <sub>IH</sub> - 0.1	V	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> - 0.040	V <sub>CC</sub> - 0.010	V <sub>CC</sub>	V	No Load
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> - 1.00	V <sub>CC</sub> - 0.800	V <sub>CC</sub> - 0.65	V	No Load
V <sub>OUT</sub> (Swing)	Output Voltage Swing <sup>(6)</sup>	0.650	0.800	1.00	V	No Load
		—	0.400	—		50Ω Environment
R <sub>OUT</sub>	Output Source Impedance (CLK_OUT, /CLK_OUT and DATA_OUT, /DATA_OUT)	40	50	60	Ω	

**Note 6.** V<sub>OUT(SWING)</sub> is defined as the swing on one output of a differential pair, that is |V<sub>OH</sub> - V<sub>OL</sub>| on one pin. The swing for common mode noise immunity purposes is 2 × V<sub>OUT(SWING)</sub>. Actual voltage levels and differential swing will depend on customer termination scheme. Typically, a 400mV swing is available in a 50Ω environment. Refer to “CML Termination” figures for more details.

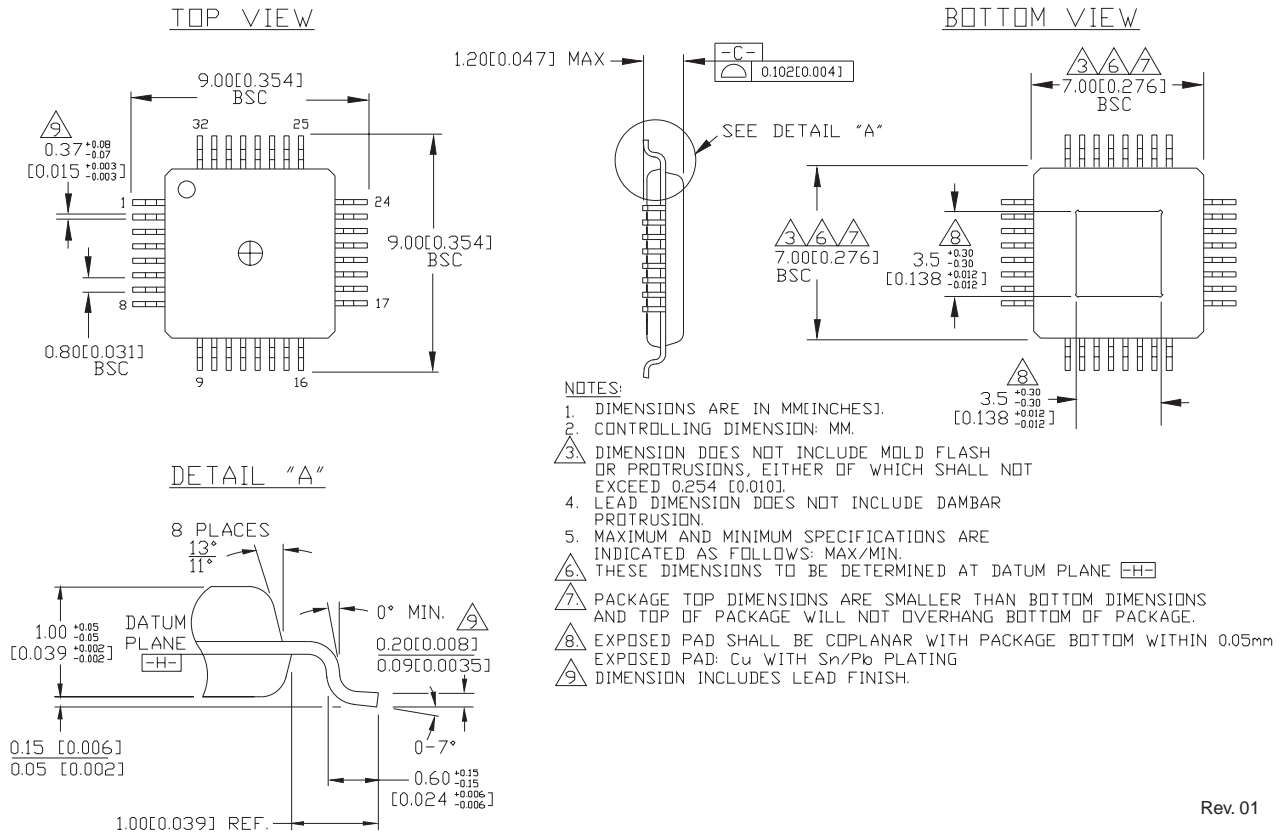
**AC ELECTRICAL CHARACTERISTICS<sup>(7)</sup>** $V_{CC} = 2.3V$  to  $3.6V$ ;  $GND = 0V$ 

Symbol	Parameter	$T_A = -40^\circ C$		$T_A = +25^\circ C$		$T_A = +85^\circ C$		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
$f_{MAX}$	Maximum Frequency	2.5	—	2.5	—	2.5	—	GHz
$\Delta t$	Delay step size	36	52	36	52	36	52	ps
$t_{PLH}$ $t_{PHL}$	Delay line insertion delay <sup>(8)</sup>	232	384	232	384	232	384	ps
$t_{DELAY}$	Delay line range	250	365	290	420	335	465	ps
$t_{JITTER}$	Output jitter	—	<1	—	<1	—	<1	ps <sub>RMS</sub>
$t_{SKEW}$	Delay line duty cycle skew ( $ t_{PLH} - t_{PHL} $ )	—	50	—	50	—	50	ps
DC	Duty cycle	45	55	45	55	45	55	%
$t_r/t_f$	CML Output rise/fall time (20% to 80%)	—	100	—	110	—	120	ps

**Note 7.** Tested using the 50W load, as shown in Figure 4.**Note 8.** Delay line insertion delay is the minimum input-to-output delay with select control set to S2:S0 = 0 for CLK\_OUT and S2:S0 = 7 for DATA\_OUT. This resulting delay is the inherent propagation delay.



**32-PIN EPAD-TQFP (DIE UP) (H32-1)**



Rev. 01

**MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA**

TEL + 1 (408) 944-0800 FAX + 1 (408) 474-1000 WEB <http://www.micrel.com>

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