FEATURES

- **550MHz count frequency**
- **Extended 100E V_{EE} range of –4.2V to –5.5V**
- **Look-ahead-carry input and output**
- **Fully synchronous up and down counting**
- **Asynchronous Master Reset**
- **Internal 75KΩ input pull-down resistors**
- **Available in 28-pin PLCC package**

PIN NAMES

Pin	Function
D_0–D_5	Preset Data Inputs
Q_0–Q_5	Differential Data Outputs
S_1, S_2	Mode Control Pins
MR	Master Reset
CLK	Clock Input
C_{OUT}, $\overline{C}_{OUT}$	Carry Out Output (Active LOW)
$\overline{CL}_{OUT}$	Look-Ahead-Carry Output
$\overline{C}_{IN}$	Carry-In Input (Active LOW)
$\overline{CL}_{IN}$	Look-Ahead-Carry Input
V_{CCO}	V_{CC} to Output

DESCRIPTION

The SY10/100E136 are 6-bit synchronous, presettable, cascadable universal counters. These devices generate a look-ahead-carry output and accept a look-ahead-carry input. These two features allow for the cascading of multiple E136s for wider bit width counters that operate at very nearly the same frequency as the stand-alone counter.

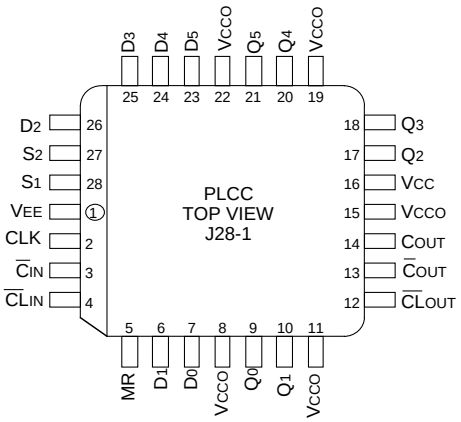
The $\overline{CL}_{OUT}$ output will pulse LOW for one clock cycle one count before the E136 reaches terminal count. The $\overline{C}_{OUT}$ output will pulse LOW for one clock cycle when the counter reaches terminal count. For more information on utilizing the look-ahead-carry features of the device, please refer to the applications section of this data sheet. The differential C_{OUT} output facilitates the E136's use in programmable divider and self-stopping counter applications.

Unlike the H136 and other similar universal counter designs, the E136 carry-out and look-ahead-carry-out signals are registered on chip. This design alleviates the glitch problem seen on many counters where the carry-out signals are merely gated. Because of this architecture, there are some minor functional differences between the E136 and H136 counters. The user, regardless of familiarity with the H136, should read this data sheet carefully. Note specifically (see block diagram) the operation of the carry-out outputs and the look-ahead-carry-in input when utilizing the Master Reset.

When left open, all of the input pins will be pulled LOW via an input pulldown resistor. The Master Reset is an asynchronous signal which, when asserted, will force the Q outputs LOW.

The Q outputs need not be terminated for the E136 to function properly. In fact, if these outputs will not be used in a system, it is recommended that they be left open to save power and minimize noise. This practice will minimize switching noise which can reduce the maximum count frequency of the device, or significantly reduce margins against other noise in the system.

PACKAGE/ORDERING INFORMATION



28-Pin PLCC (J28-1)

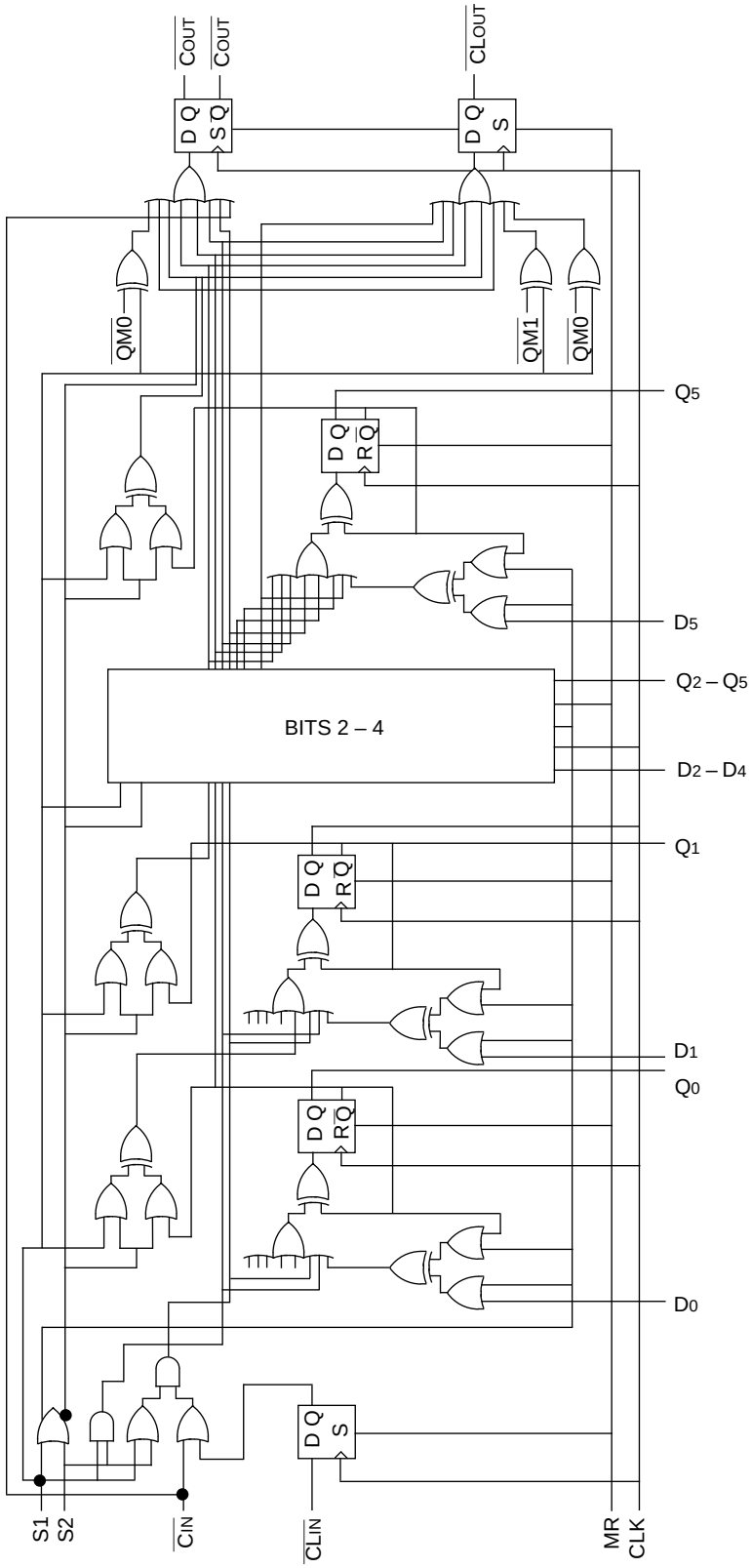
Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY10E136JC	J28-1	Commercial	SY10E136JC	Sn-Pb
SY10E136JCTR[2]	J28-1	Commercial	SY10E136JC	Sn-Pb
SY100E136JC	J28-1	Commercial	SY100E136JC	Sn-Pb
SY100E136JCTR[2]	J28-1	Commercial	SY100E136JC	Sn-Pb
SY10E136JC	J28-1	Commercial	SY10E136JC	Sn-Pb
SY10E136JCTR[2]	J28-1	Commercial	SY10E136JC	Sn-Pb
SY100E136JC	J28-1	Commercial	SY100E136JC	Sn-Pb
SY100E136JCTR[2]	J28-1	Commercial	SY100E136JC	Sn-Pb
SY10E136JZ[3]	J28-1	Commercial	SY10E136JZ with Pb-Free bar-line indicator	Matte-Sn
SY10E136JZTR[2, 3]	J28-1	Commercial	SY10E136JZ with Pb-Free bar-line indicator	Matte-Sn
SY100E136JZ[3]	J28-1	Commercial	SY100E136JZ with Pb-Free bar-line indicator	Matte-Sn
SY100E136JZTR[2, 3]	J28-1	Commercial	SY100E136JZ with Pb-Free bar-line indicator	Matte-Sn

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

BLOCK DIAGRAM[1]



E136 Universal Up/Down Counter Logic Diagram

Note:

1. This diagram is provided for understanding of logic operation only. It should not be used for propagation delays as many gate functions are achieved internally without incurring a full gate delay.

TRUTH TABLE[1]

S_1	S_2	$\overline{C}_{IN}$	MR	CLK	Function
L	L	X	L	Z	Preset Parallel Data Inputs
L	H	L	L	Z	Increment (Count Up)
L	H	H	L	Z	Hold Count
H	L	L	L	Z	Decrement (Count Down)
H	L	H	L	Z	Hold Count
H	H	X	L	Z	Hold Count
X	X	X	H	X	Reset (Qn = LOW; C_{OUT} = HIGH)

Note:

1. Expanded truth table included on following pages.

EXPANDED TRUTH TABLE[1]

Function	S_1	S_2	MR	$\overline{C}_{IN}$	$\overline{CL}_{IN}$	CLK	D_5	D_4	D_3	D_2	D_1	D_0	Q_5	Q_4	Q3	Q_2	Q_1	Q_0	$\overline{C}_{OUT}$	$\overline{CL}_{OUT}$
Preset	L	L	L	X	X	Z	L	L	L	L	H	H	L	L	L	L	H	H	H	H
Down	H	L	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	H	L	H	H
	H	L	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	L	H	H	L
	H	L	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	L	L	L	H
	H	L	L	L	L	Z	X	X	X	X	X	X	H	H	H	H	H	H	H	H
Preset	L	L	L	X	X	Z	H	H	H	H	L	L	H	H	H	H	L	L	H	H
Up	L	H	L	L	L	Z	X	X	X	X	X	X	H	H	H	H	L	H	H	H
	L	H	L	L	L	Z	X	X	X	X	X	X	H	H	H	H	H	L	H	L
	L	H	L	L	L	Z	X	X	X	X	X	X	H	H	H	H	H	H	L	H
	L	H	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	L	L	H	H
	L	H	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	L	H	H	H
	L	H	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	H	L	H	H
Hold	H	H	L	X	X	Z	X	X	X	X	X	X	L	L	L	L	H	L	H	H
	H	H	L	X	X	Z	X	X	X	X	X	X	L	L	L	L	H	L	H	H
Down	H	L	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	L	H	H	L
Hold	H	L	L	H	L	Z	X	X	X	X	X	X	L	L	L	L	L	H	H	H
Down	H	L	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	L	L	L	H
Hold	H	L	L	H	L	Z	X	X	X	X	X	X	L	L	L	L	L	L	H	H
	H	L	L	H	L	Z	X	X	X	X	X	X	L	L	L	L	L	L	H	H
	H	L	L	H	H	Z	X	X	X	X	X	X	L	L	L	L	L	L	H	H
Hold	H	L	L	L	H	Z	X	X	X	X	X	X	L	L	L	L	L	L	L	H
	H	L	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	L	L	L	H
Hold	H	H	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	L	L	L	H
Preset	L	L	L	X	X	Z	H	H	H	H	L	L	H	H	H	H	L	L	H	H
Up	L	H	L	L	L	Z	X	X	X	X	X	X	H	H	H	H	L	H	H	H
	L	H	L	L	L	Z	X	X	X	X	X	X	H	H	H	H	H	L	H	L
Hold	L	H	L	H	L	Z	X	X	X	X	X	X	H	H	H	H	H	L	H	H
Up	L	H	L	L	L	Z	X	X	X	X	X	X	H	H	H	H	H	H	L	H
Hold	L	H	L	H	L	Z	X	X	X	X	X	X	H	H	H	H	H	H	H	H
	L	H	L	H	H	Z	X	X	X	X	X	X	H	H	H	H	H	H	H	H
Hold	L	H	L	L	L	Z	X	X	X	X	X	X	H	H	H	H	H	H	L	H
Up	L	H	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	L	L	H	H
	L	H	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	L	H	H	H
	L	H	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	H	L	H	H
	L	H	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	H	H	H	H
Reset	X	X	H	X	X	X	X	X	X	X	X	X	L	L	L	L	L	L	H	H

Note:

1. Z = LOW-to-HIGH transition

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA	—
I_{EE}	Power Supply Current										mA	—
	10E	—	125	150	—	125	150	—	125	150		
	100E	—	125	150	—	125	150	—	140	170		

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
f_{COUNT}	Maximum Count Frequency	550	650	—	550	650	—	550	650	—	MHz	—
t_{PD}	Propagation Delay to Output										ps	—
	CLK to Q	850	1150	1450	850	1150	1450	850	1150	1450		
	MR to Q	850	1150	1450	850	1150	1450	850	1150	1450		
	CLK to $\overline{C}_{OUT}$	800	1150	1300	800	1150	1300	800	1150	1300		
	CLK to $\overline{CL}_{OUT}$	825	1150	1400	825	1150	1400	825	1150	1400		
t_S	Set-up Time										ps	—
	S_1, S_2	1500	650	—	1500	650	—	1500	650	—		
	$\overline{D}$	800	400	—	800	400	—	800	400	—		
	$\overline{CL}_{IN}$	150	0	—	150	0	—	150	0	—		
	$\overline{C}_{IN}$	800	400	—	800	400	—	800	400	—		
t_H	Hold Time										ps	—
	S_1, S_2	150	–200	—	150	–200	—	150	–200	—		
	$\overline{D}$	150	–250	—	150	–250	—	150	–250	—		
	$\overline{CL}_{IN}$	300	0	—	300	0	—	300	0	—		
	$\overline{C}_{IN}$	150	–250	—	150	–250	—	150	–250	—		
t_{RR}	Reset Recovery Time	1000	700	—	1000	700	—	1000	700	—	ps	—
t_{PW}	Minimum Pulse Width CLK, MR	700	400	—	700	400	—	700	400	—	ps	—
t_r t_f	Rise/Fall Times 20% to 80%										ps	—
	$\overline{C}_{OUT}$	275	—	600	275	—	600	275	—	600		
	Other	300	—	700	300	—	700	300	—	700		

APPLICATIONS INFORMATION

Overview

The SY10E/100E136 are 6-bit synchronous, presettable, cascadable universal counters. Using the S_1 and S_2 control pins, the user can select between preset, count up, count down and hold count. The Master Reset pin will reset the internal counter and set the $\overline{C}_{OUT}$, $\overline{CL}_{OUT}$ and $\overline{CL}_{IN}$ flip-flops. Unlike previous 136-type counters, the carry-out outputs will go to a high state during the preset operation. In addition, since the carry-out outputs are registered, they will not go low if terminal count is loaded into the register. The look-ahead-carry-out output functions similarly.

Note from the schematic the use of the master information from the least significant bits for control of the two carry-out functions. This architecture not only reduces the carry-out delay, but is essential to incorporate the registered carry-out functions. In addition to being faster, the resulting carry-out signals are stable and glitch free because these functions are registered.

Cascading Multiple E136 Devices

Many applications require counters significantly larger than the 6 bits available with the E136. For these applications, several E136 devices can be cascaded to increase the bit width of the counter to meet the needs of the application.

In the past, cascading several 136-type universal counters necessarily impacted the maximum count frequency of the resulting counter chain. This performance impact was the result of the terminal count signal of the lower order counters having to ripple through the entire counter chain. As a result, past counters of this type were not widely used in large bit counter applications.

An alternative counter architecture similar to the E016 binary counter was implemented to alleviate the need to ripple propagate the terminal count signal. Unfortunately, these types of counters require external gating for cascading designs of more than two devices. In addition to requiring additional components, these external gates limit the cascaded count frequency to a value less than the free running count frequency of a single counter. Although there is a performance impact with this type of architecture, it is minor compared to the impact of the ripple propagate designs. As a result, the E016-type counters have been used extensively in applications requiring very high speed, wide bit width synchronous counters.

Several improvements have been incorporated to past universal counter designs in the E136 universal counter. These enhancements make the E136 the unparalleled leader in its class. With the addition of look-ahead-carry features on the terminal count signal, very large counter chains can be designed which function at very nearly the same clock frequency as a single free running device. More importantly, these counter chains require no external gating. Figure 1 below illustrates the interconnect scheme for using the look-ahead-carry features of the E136 counter.

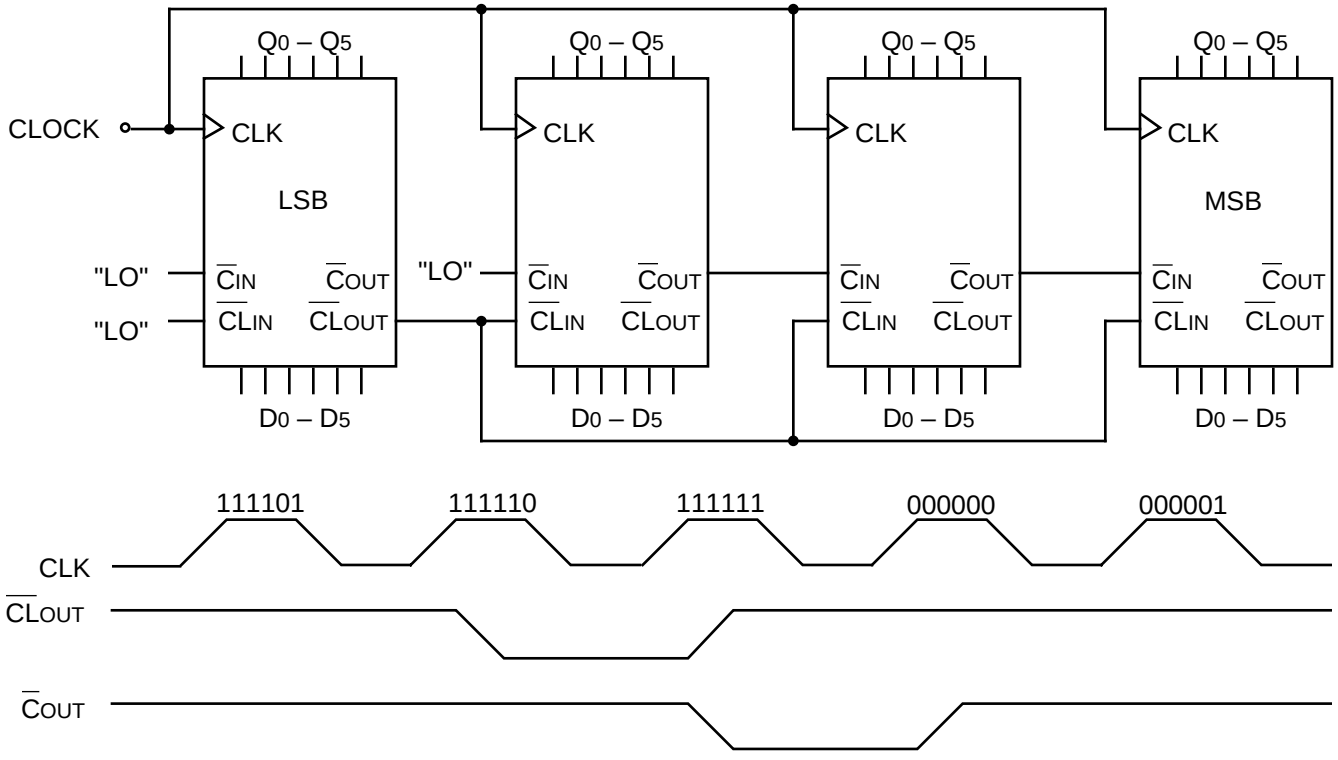


Figure 1. 24-bit Cascaded E136 Counter

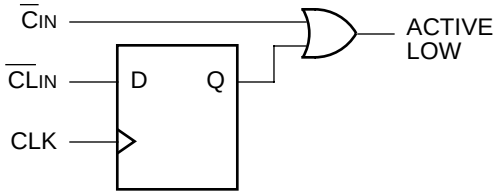


Figure 2. Look-Ahead-Carry Input Structure

Note from the waveforms that the look-ahead-carry output ($\overline{CL}_{OUT}$) pulses low one clock pulse before the counter reaches terminal count. Also note that both $\overline{CL}_{OUT}$ and the carry-out pin ($\overline{C}_{OUT}$) of the device pulse low for only one clock period. The input structure for look-ahead-carry-in ($\overline{CL}_{IN}$) and carry-in ($\overline{C}_{IN}$) is pictured in Figure 2.

The $\overline{CL}_{IN}$ input is registered and then OR'ed with the $\overline{C}_{IN}$ input. From the truth table one can see that both the $\overline{C}_{IN}$ and the $\overline{CL}_{IN}$ inputs must be in a LOW state for the E136 to be enabled to count (either count up or count down). The $\overline{CL}_{IN}$ inputs are driven by the $\overline{CL}_{OUT}$ output of the lower order E136 and, therefore, are only asserted for a single clock period. Since the $\overline{CL}_{IN}$ input is registered, it must be asserted one clock period prior to the $\overline{C}_{IN}$ input.

If the counter previous to a given counter is at terminal count, its $\overline{C}_{OUT}$ output, and thus the $\overline{C}_{IN}$ input of the given counter will be in the "LOW" state. This signals the given counter that it will need to count one upon the next terminal count of the least significant counter (LSC). The $\overline{CL}_{OUT}$ output of the LSC will pulse low one clock period before it reaches terminal count. This $\overline{CL}_{OUT}$ signal will be clocked into the $\overline{CL}_{IN}$ input of the higher order counters on the following positive clock transition. Since both $\overline{C}_{IN}$ and $\overline{CL}_{IN}$ are in the LOW state, the next clock pulse will cause the least significant counter to roll over and all higher order counters, if signaled by the $\overline{C}_{IN}$ inputs, to count by one.

During the clock pulse in which the higher order counter is counting by one, the $\overline{CL}_{IN}$ is clocking in the high signal presented by the $\overline{CL}_{OUT}$ of the LSC. The $\overline{C}_{IN}$s in the higher order counter will ripple through the chain to update the count status for the next occurrence of terminal count on the LSC. This ripple propagation will not affect the count frequency as it has 2^6-1 or 63 clock pulses to ripple through without affecting the count operation of the chain.

The only limiting factor which could reduce the count frequency of the chain as compared to a free running single device will be the set-up time of the $\overline{CL}_{IN}$ input. This limit will consist of the CLK to $\overline{CL}_{OUT}$ delay of the E136, plus the $\overline{CL}_{IN}$ set-up time, plus any path length differences between the $\overline{CL}_{OUT}$ output and the clock.

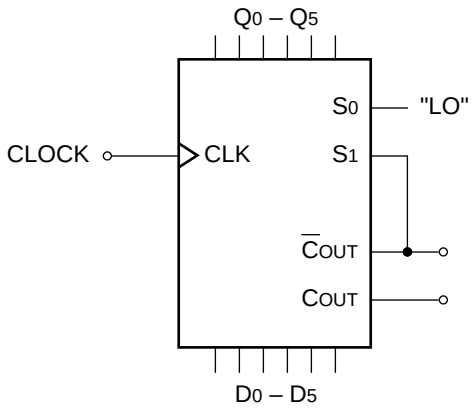


Figure 3. 6-bit Programmable Divider

Programmable Divider

Using external feedback of the $\overline{C}_{OUT}$ pin, the E136 can be configured as a programmable divider. Figure 3 illustrates the configuration for a 6-bit count-down programmable divider. If for some reason a count-up divider is preferred, the $\overline{C}_{OUT}$ signal is simply fed back to S_2 rather than S_1. Examination of the truth table for the E136 shows that when both S_1 and S_2 are LOW, the counter will parallel load on the next positive transition of the clock. If the S_2 input is low and the S_1 input is high, the counter will be in the count-down mode and will count towards an all zero state upon successive clock pulses. Knowing this and the operation of the $\overline{C}_{OUT}$ output, it becomes a trivial matter to build programmable dividers.

For a programmable divider, one must to load a predesignated number into the counter and count to terminal count. Upon terminal count, the counter should automatically reload the divide number. With the architecture shown in Figure 3, when the counter reaches terminal count, the $\overline{C}_{OUT}$ output, and thus the S_1 input, will go LOW. This, combined with the low on S_2 will cause the counter to load the inputs present on D_0–D_5. Upon loading the divide value into the counter, $\overline{C}_{OUT}$ will go HIGH as the counter is no longer at terminal count, thereby placing the counter back into the count mode.

Divide Ratio	Preset Data Inputs					
	D5	D4	D3	D2	D1	D0
2	L	L	L	L	L	H
3	L	L	L	L	H	L
4	L	L	L	L	H	H
5	L	L	L	H	L	L
*	*	*	*	*	*	*
*	*	*	*	*	*	*
36	H	L	L	L	H	H
37	H	L	L	H	L	L
38	H	L	L	H	L	H
*	*	*	*	*	*	*
*	*	*	*	*	*	*
62	H	H	H	H	L	H
63	H	H	H	H	H	L
64	H	H	H	H	H	H

Table 1. Preset Inputs Versus Divide Ratio

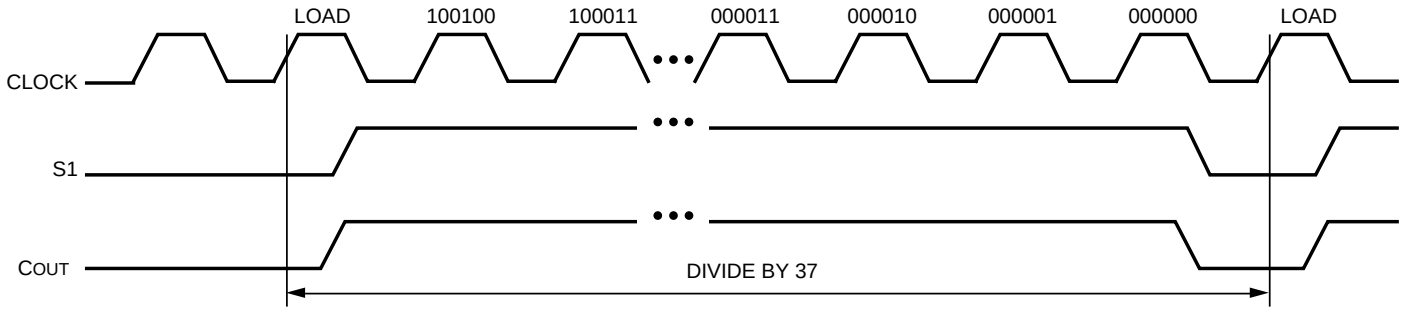


Figure 4. Programmable Divider Waveforms

The exercise of building a programmable divider then becomes simply determining what value to load into the counter to accomplish the desired division. Since the load operation requires a clock pulse, to divide by N, N-1 must be loaded into the counter. A single E136 device is capable of divide ratios of 2 to 64, inclusive. Table 1 outlines the load values for the various divide ratios. Figure 4 presents the waveforms resulting from a divide by 37 operation. Note that the availability of the COUT complimentary output ($\overline{C}$OUT) allows the user to choose the polarity of the divide by output.

For single device programmable counters, the E016 counter is probably a better choice than the E136. The E016 has an internal feedback to control the reloading of the counter. This not only simplifies board design, but also will result in a faster maximum count frequency.

For programmable dividers of larger than 8 bits, the benefits of the E016 diminishes and, in fact, for very wide dividers, the E136 will provide the capability of a faster count frequency. Figure 5 shows the architecture of a 24-bit programmable divider implemented using E136 counters. Note the need for one external gate to control the loading of the entire counter chain. An ideal device for the external gating of this architecture would be the 4-input OR function in the 8-lead SOIC ECLinPS Lite™ family. However, the final decision as to what device to use for external gating requires a balancing of performance needs, cost and available board space. Note that because of the need for external gating, the maximum count frequency of a given sized programmable divider will be less than that of a single cascaded counter.

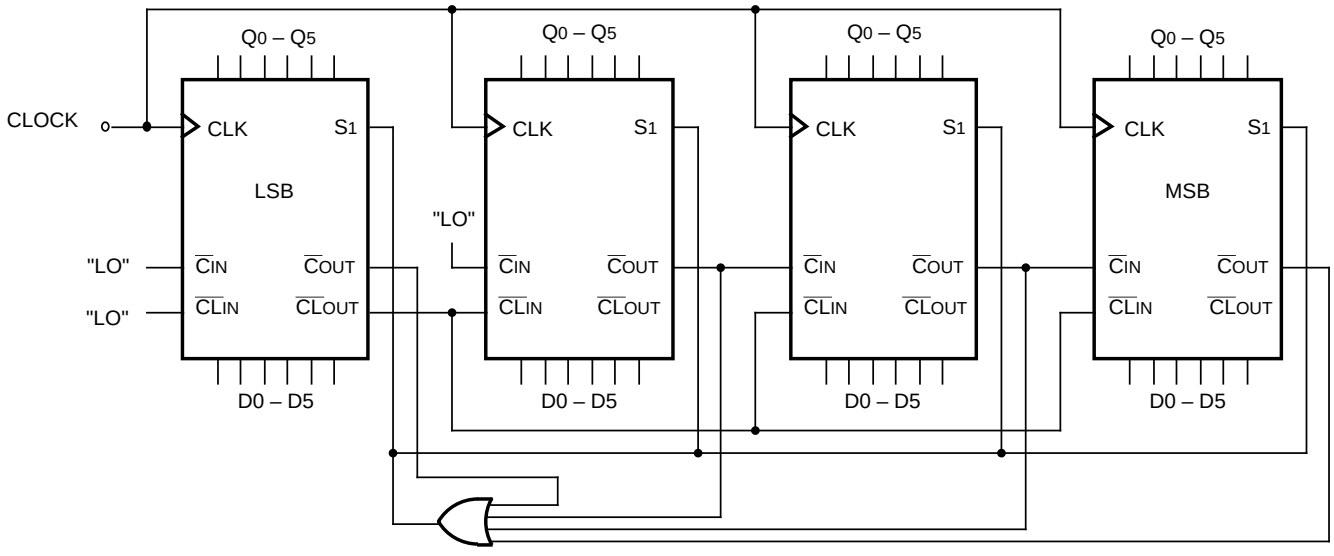
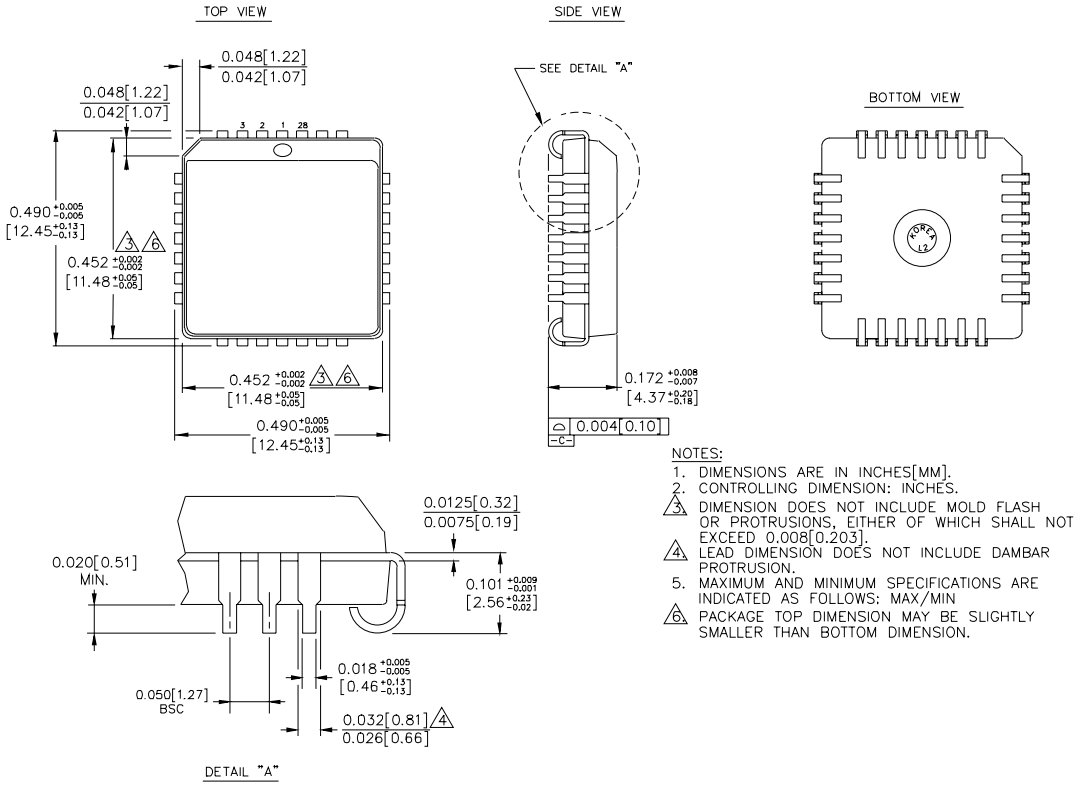


Figure 5. 24-bit Programmable Divider Architecture

28-PIN PLCC (J28-1)



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

Rev. 03

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