



# PIC16(L)F1526/1527

## 64-Pin 8-Bit Flash Microcontroller Product Brief

### High-Performance RISC CPU:

- C Compiler Optimized Architecture
- Only 49 Instructions
- Up to 28 Kbytes Linear Program Memory Addressing
- Up to 1536 Bytes Linear Data Memory Addressing
- Operating Speed:
  - DC – 20 MHz clock input @ 2.5V
  - DC – 16 MHz clock input @ 1.8V
  - DC – 200 ns instruction cycle
- Interrupt Capability with Automatic Context Saving
- 16-Level Deep Hardware Stack with Optional Overflow/Underflow Reset
- Direct, Indirect and Relative Addressing modes:
  - Two full 16-bit File Select Registers (FSRs)
  - FSRs can read program and data memory

### Flexible Oscillator Structure:

- 16 MHz Internal Oscillator Block:
  - Accurate to  $\pm 10\%$
  - Software selectable frequency range from 16 MHz to 31 kHz
- 31 kHz Low-Power Internal Oscillator
- External Oscillator Block with:
  - Four crystal/resonator modes up to 20 MHz
  - Three external clock modes up to 20 MHz
- Fail-Safe Clock Monitor:
  - Allows for safe shutdown if peripheral clock stops
- Two-Speed Oscillator Start-up
- Oscillator Start-up Timer (OST)

### Special Microcontroller Features:

- Operating Voltage Range:
  - 1.8V to 3.6V (PIC16LF152X)
  - 2.3V to 5.5V (PIC16F152X)
- Self-Programmable under Software Control
- Power-on Reset (POR)
- Power-up Timer (PWRT)
- Programmable Ultra Low-Power Brown-Out Reset (ULPBOR)
- Extended Watch-Dog Timer (WDT):
  - Programmable period from 1ms to 256s
- Programmable Code Protection
- In-Circuit Serial Programming™ (ICSP™) via two pins
- In-Circuit Debug (ICD) via Two Pins
- Enhanced Low-Voltage Programming (LVP)
- Power-Saving Sleep mode

### Extreme Low-Power Management PIC16LF152X with nanoWatt XLP:

- Sleep mode: 30 nA @ 1.8V, typical
- Watchdog Timer: 300 nA @ 1.8V, typical
- Timer1 Oscillator: 600 nA @ 32 kHz, 1.8V, typical

### Analog Features:

- Analog-to-Digital Converter (ADC):
  - 10-bit resolution
  - Up to 30 channels
  - Auto acquisition capability
  - Conversion available during Sleep
  - Dedicated ADC RC oscillator
  - Fixed Voltage Reference (FVR) as channel
  - Fixed Voltage Reference (FVR) as ADC positive reference
  - Temperature indicator channel input
- Voltage Reference module:
  - Fixed Voltage Reference (FVR) with 1.024V, 2.048V and 4.096V output levels

### Peripheral Features:

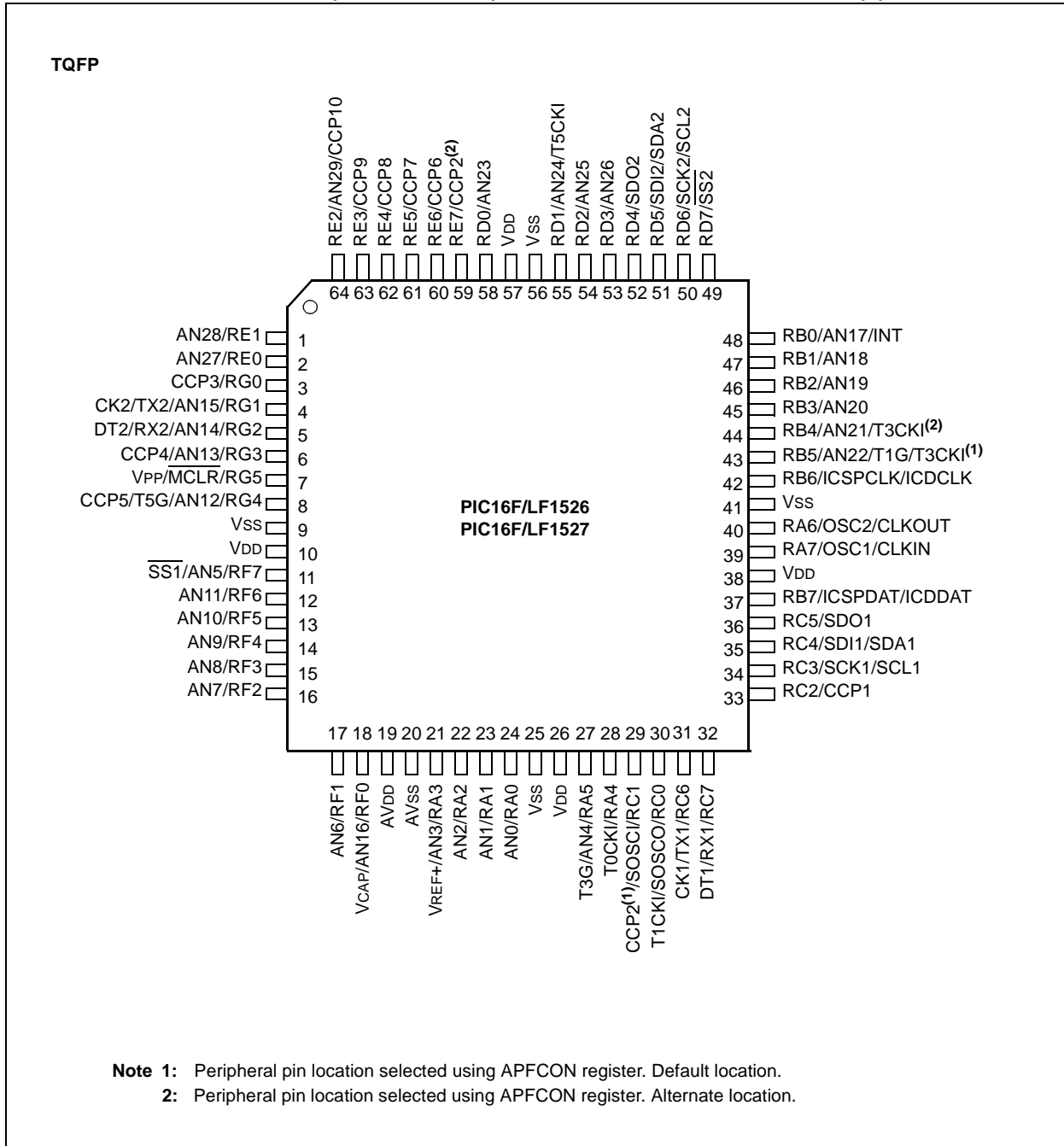
- 53 I/O Pins and 1 Input-only Pin:
  - High current sink/source 25 mA/25 mA
  - Individually programmable weak pull-ups
  - Individually programmable interrupt-on-change (IOC) pins
- Timer0: 8-Bit Timer/Counter with 8-Bit Programmable Prescaler
- Enhanced Timer1, 3, 5:
  - 16-bit timer/counter with prescaler
  - External Gate Input mode
  - Low-power 32 kHz secondary oscillator
- Timer2, 4, 6, 8, 10: 8-Bit Timer/Counter with 8-Bit Period Register, Prescaler and Postscaler
- Ten Capture/Compare/PWM (CCP) modules
  - 16-bit Capture, 200 ns (max. resolution)
  - 16-bit Compare, 200 ns (max. resolution)
  - 10-bit PWM, 20 kHz @ 10 bits (max. frequency)
- Two Master Synchronous Serial Ports (MSSP) with SPI and I<sup>2</sup>C™ with:
  - 7-bit address masking
  - SMBus/PMBus™ compatibility
  - Byte NACKing
- Two Enhanced Universal Synchronous Asynchronous Receiver Transmitters (EUSART):
  - RS-232, RS-485 and LIN compatible
  - Auto-Baud Detect
  - Auto-wake-up on start

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**TABLE 1: PIC16(L)F1526/1527 FAMILY TYPES**

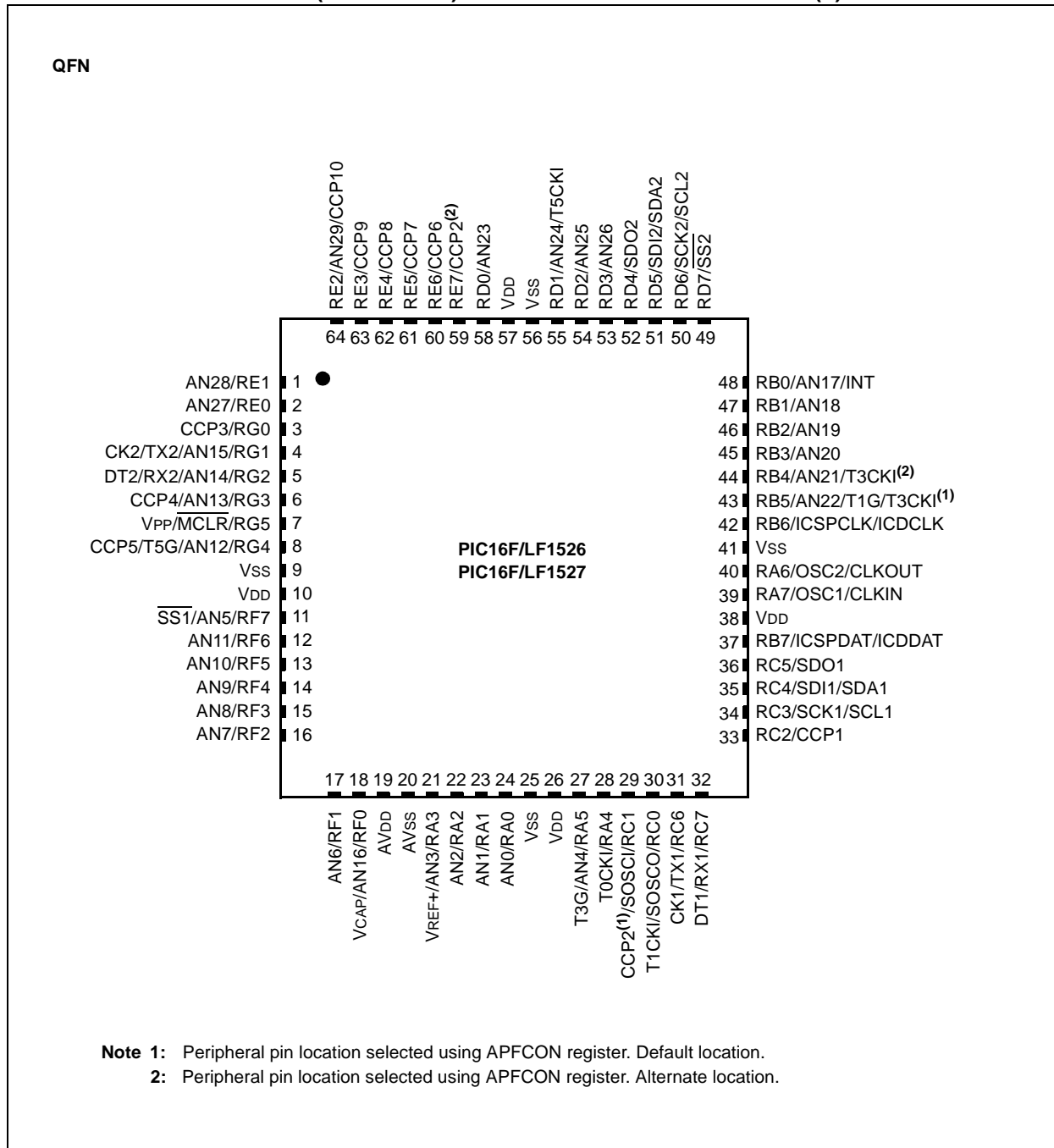
Device	Program Memory Flash (words)	SRAM (bytes)	I/Os	10-bit A/D (ch)	Timers 8/16-bit	EUSART	MSSP (I <sup>2</sup> C™/SPI)	CCP
PIC16F1526 PIC16LF1526	8192	768	54	30	6/3	2	2	10
PIC16F1527 PIC16LF1527	16384	1536	54	30	6/3	2	2	10

**FIGURE 1: 64-PIN TQFP (10MM X 10MM) PACKAGE DIAGRAM FOR PIC16(L)F1526/1527**



# PIC16(L)F1526/1527

**FIGURE 2: 64-PIN QFN (9MM X 9MM) PACKAGE DIAGRAM FOR PIC16(L)F1526/1527**



# PIC16(L)F1526/1527

**TABLE 2: 64-PIN DEVICE ALLOCATION TABLE (PIC16(L)F1526/1527)**

I/O	64-Pin TQFP, QFN	A/D	Timers	CCP	USART	SSP	Interrupt	Pull-up	Basic
RA0	24	AN0	—	—	—	—	—	—	—
RA1	23	AN1	—	—	—	—	—	—	—
RA2	22	AN2	—	—	—	—	—	—	—
RA3	21	AN3	—	—	—	—	—	—	VREF+
RA4	28	—	T0CKI	—	—	—	—	—	—
RA5	27	AN4	T3G	—	—	—	—	—	—
RA6	40	—	—	—	—	—	—	—	OSC2/CLKOUT
RA7	39	—	—	—	—	—	—	—	OSC1/CLKIN
RB0	48	AN17	—	—	—	—	INT/ IOC	Y	—
RB1	47	AN18	—	—	—	—	IOC	Y	—
RB2	46	AN19	—	—	—	—	IOC	Y	—
RB3	45	AN20	—	—	—	—	IOC	Y	—
RB4	44	AN21	T3CKI <sup>(2)</sup>	—	—	—	IOC	Y	—
RB5	43	AN22	T1G/T3CKI <sup>(1)</sup>	—	—	—	IOC	Y	—
RB6	42	—	—	—	—	—	IOC	Y	ICSPCLK/ICDCLK
RB7	37	—	—	—	—	—	IOC	Y	ICSPDAT/ICDDAT
RC0	30	—	SOSCO/T1CKI	—	—	—	—	—	—
RC1	29	—	SOSCI	CCP2 <sup>(1)</sup>	—	—	—	—	—
RC2	33	—	—	CCP1	—	—	—	—	—
RC3	34	—	—	—	—	SCK1/SCL1	—	—	—
RC4	35	—	—	—	—	SDI1/SDA1	—	—	—
RC5	36	—	—	—	—	SDO1	—	—	—
RC6	31	—	—	—	TX1/CK1	—	—	—	—
RC7	32	—	—	—	RX1/DT1	—	—	—	—
RD0	58	AN23	—	—	—	—	—	Y	—
RD1	55	AN24	T5CKI	—	—	—	—	Y	—
RD2	54	AN25	—	—	—	—	—	Y	—
RD3	53	AN26	—	—	—	—	—	Y	—
RD4	52	—	—	—	—	SDO2	—	Y	—
RD5	51	—	—	—	—	SDI2, SDA2	—	Y	—
RD6	50	—	—	—	—	SCK2, SCL2	—	Y	—
RD7	49	—	—	—	—	SS2	—	Y	—
RE0	2	AN27	—	—	—	—	—	Y	—
RE1	1	AN28	—	—	—	—	—	Y	—
RE2	64	AN29	—	CCP10	—	—	—	Y	—
RE3	63	—	—	CCP9	—	—	—	Y	—
RE4	62	—	—	CCP8	—	—	—	Y	—
RE5	61	—	—	CCP7	—	—	—	Y	—
RE6	60	—	—	CCP6	—	—	—	Y	—

**Note 1:** Peripheral pin location selected using APFCON register. Default Location.

**2:** Peripheral pin location selected using APFCON register. Alternate Location.

**3:** Weak pull-up always enabled when MCLR is enabled, otherwise the pull-up is under user control.

# PIC16(L)F1526/1527

**TABLE 2: 64-PIN DEVICE ALLOCATION TABLE (PIC16(L)F1526/1527) (CONTINUED)**

I/O	64-Pin TQFP, QFN	A/D	Timers	CCP	USART	SSP	Interrupt	Pull-up	Basic
RE7	59	—	—	CCP2 <sup>(2)</sup>	—	—	—	Y	—
RF0	18	AN16	—	—	—	—	—	—	VCAP
RF1	17	AN6	—	—	—	—	—	—	—
RF2	16	AN7	—	—	—	—	—	—	—
RF3	15	AN8	—	—	—	—	—	—	—
RF4	14	AN9	—	—	—	—	—	—	—
RF5	13	AN10	—	—	—	—	—	—	—
RF6	12	AN11	—	—	—	—	—	—	—
RF7	11	AN5	—	—	—	SS1	—	—	—
RG0	3	—	—	CCP3	—	—	—	—	—
RG1	4	AN15	—	—	TX2/CK2	—	—	—	—
RG2	5	AN14	—	—	RX2/DT2	—	—	—	—
RG3	6	AN13	—	CCP4	—	—	—	—	—
RG4	8	AN12	T5G	CCP5	—	—	—	—	—
RG5	7	—	—	—	—	—	—	Y <sup>(3)</sup>	MCLR/VPP
VDD	10, 26, 38, 57	—	—	—	—	—	—	—	VDD
VSS	9, 25, 41, 56	—	—	—	—	—	—	—	VSS
AVDD	19	—	—	—	—	—	—	—	AVDD
AVSS	20	—	—	—	—	—	—	—	AVSS

**Note 1:** Peripheral pin location selected using APFCON register. Default Location.

**2:** Peripheral pin location selected using APFCON register. Alternate Location.

**3:** Weak pull-up always enabled when MCLR is enabled, otherwise the pull-up is under user control.

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NOTES:

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