UCS2112

USB Dual-Port Power Switch and Current Monitor

Features

- Dual-Port Power Switches:
  - 2.9V to 5.5V source voltage range
  - 3.0A continuous current per V_{BUS} port with 40 mΩ On resistance per switch
  - Independent port power switch enable pins
  - DUAL fault ALERT# active drain output pins
  - Constant Current or Trip mode current limiting behaviors
  - Undervoltage and overvoltage lockout
  - Back-drive, back-voltage protection
  - Auto-recovery fault handling with low test current
  - BOOST# logic output to increase DC-DC converter output under large load conditions
  - A_DET# open-drain outputs for device attach detection per port
- SMBus 2.0/I^2C Mode Features:
  - Eight programmable current limits assignable to each power switch
  - Other SMBus addresses available upon request
  - Block read and block write
- Self-contained current monitoring (no external sense resistor required)
- Fully programmable per-port charge rationing and behaviors
- Per-port BC1.2 V_{BUS} Discharge Function
- Wide Operating Temperature Range:
  - -40°C to +105°C
- UL recognized and EN/IEC 60950-1 (CB) certified.

Description

The UCS2112 is a dual USB port power switch configuration which can provide 3.0A continuous current (3.4A maximum) per V_{BUS} port with precision overcurrent limiting (OCL), port power switch enables, auto-recovery fault handling, undervoltage and overvoltage lockout, back-drive protection and back-voltage protection, and dynamic thermal management.

The UCS2112 is well suited for both stand-alone and applications having SMBus/I^2C communications.

For applications with SMBus, the UCS2112 provides per-port current monitoring and eight programmable current limits per switch, ranging from 0.53A to 3.0A continuous current (3.4A maximum). Per-port charge rationing is also provided ranging from 3.8 mAh to 246.3 Ah.

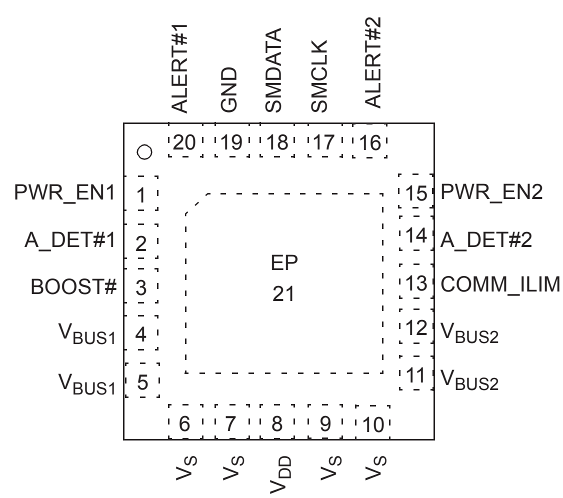
In Stand-alone mode, the UCS2112 provides eight current limits for both switches, ranging from 0.53A + 0.53A to 3A + 3A total continuous current (see Table 1-1).

Both power switches include an independent V_{BUS} discharge function and constant current mode current limiting for BC1.2 applications.

The UCS2112 is available in a 4x4 mm 20-pin QFN package.

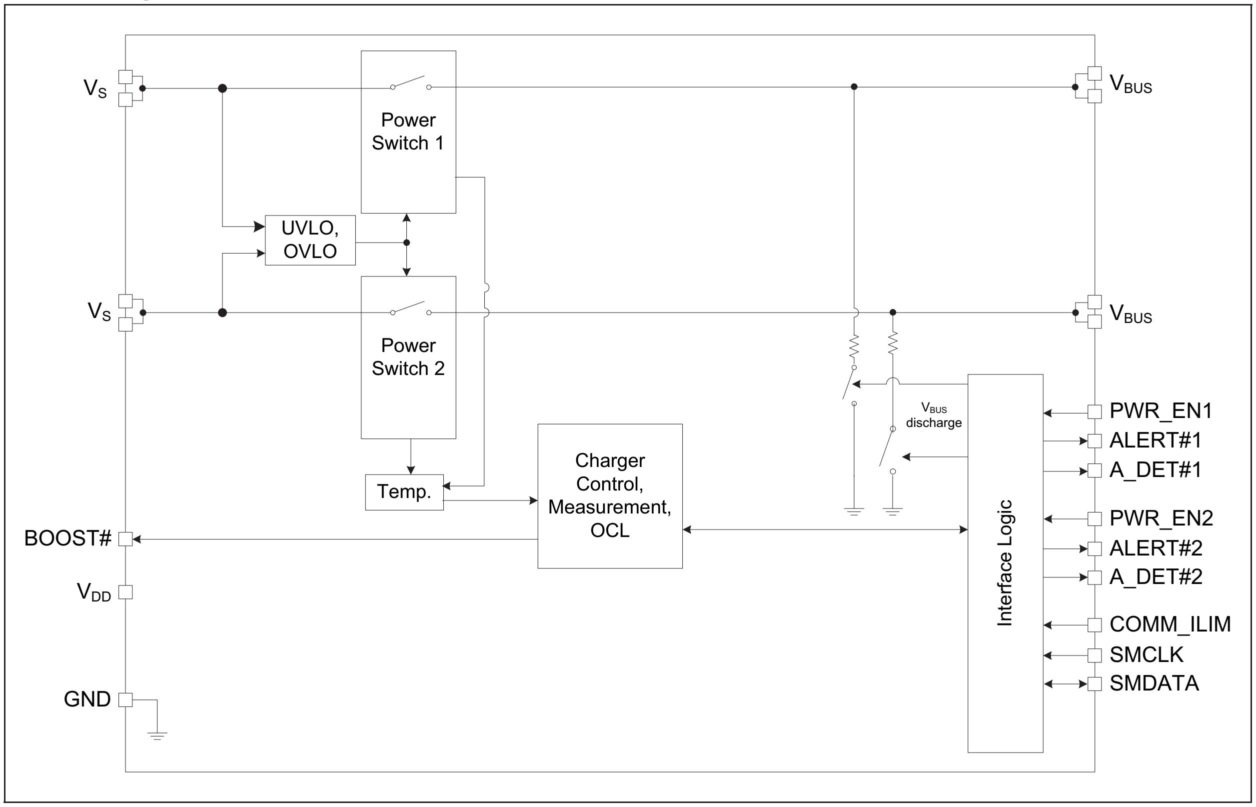
Package Type

UCS2112
4x4 QFN*



* Includes Exposed Thermal Pad (EP); see Table 3-1.

Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Voltage on V_{DD}, V_S, and V_{BUS} pins .... -0.3 to +6V
Pull-Up Voltage (V_{PULLUP}) .... -0.3 to V_{DD} + 0.3
Port Power Switch Current .... Internally limited
Voltage on any Other Pin to Ground .... -0.3 to V_{DD} + 0.3V
Current on any Other Pin .... ±10 mA
Package Power Dissipation .... See Table 1-1
Operating Ambient Temperature Range .... -40°C to +105°C
Storage Temperature Range .... -55°C to +150°C

† Notice: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: POWER DISSIPATION SUMMARY

Board	Package	θ_{JC}	θ_{JA}	De-Rating Factor above +25°C	T_A < +25°C Power Rating	T_A = +70°C Power Rating	T_A = +85°C Power Rating
High K (Note 1)	20-pin QFN 4x4 mm	6 °C/W	41 °C/W	24.4 mW/°C	2193 mW	1095 mW	729 mW
Low K (Note 1)	20-pin QFN 4x4 mm	6 °C/W	60 °C/W	16.67 mW/°C	1498 mW	748 mW	498 mW

Note 1: A High K board uses a thermal via design with the thermal landing soldered to the PCB ground plane with 0.3 mm (12 mil) diameter vias in a 3x3 matrix (9 total) at 0.5 mm (20 mil) pitch. The board is multi-layer with 1-ounce internal power and ground planes and 2-ounce copper traces on top and bottom. A Low K board is a two-layer board without thermal via design with 2-ounce copper traces on the top and bottom.

TABLE 1-2: ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise specified, V_{DD} = 4.5V to 5.5V, V_S = 2.9V to 5.5V, V_{PULLUP} = 3V to 5.5V, T_A = -40°C to 105°C. All typical values at V_{DD} = V_S = 5V, T_A = 27°C.

Characteristic	Symbol	Min.	Typ.	Max.	Unit	Conditions
Power and Interrupts – DC						
Supply Voltage	V_{DD}	4.5	5	5.5	V	
Supply Current in Active (I_{DD_ACT} + I_{S1_ACT} + I_{S2_ACT})	I_{ACTIVE}	—	850	—	µA	Average current I_{BUS} = 0 mA
Supply Current in Sleep (I_{DD_SLEEP} + I_{S1_SLEEP} + I_{S2_SLEEP})	I_{SLEEP}	—	6	20	µA	Average current $V_{PULLUP} \leq V_{DD}$
Supply Current in Detect (I_{DD_DET} + I_{S1_DET} + I_{S2_DET})	I_{DETECT}	—	200	—	µA	Average current No portable device attached (Note 1)

Note 1: This parameter is characterized, not 100% tested.
2: This parameter is ensured by design and not 100% tested.
3: The current measurement full scale range maximum value is 3.4A. However, the UCS2112 cannot report values above I_{LIM} (if $I_{BUS\_R2MIN} \leq I_{LIM}$) or above I_{BUS_R2MIN} (if $I_{BUS\_R2MIN} > I_{LIM}$ and $I_{LIM} \leq$ 1.6A).

TABLE 1-2: ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Unless otherwise specified, V_{DD} = 4.5V to 5.5V, V_S = 2.9V to 5.5V, V_{PULLUP} = 3V to 5.5V, T_A = -40°C to 105°C. All typical values at V_{DD} = V_S = 5V, T_A = 27°C.

Characteristic	Symbol	Min.	Typ.	Max.	Unit	Conditions
Power-on Reset						
V_{DD} Low Threshold	V_{DD_TH}	—	4	—	V	V_{DD} voltage increasing
V_{DD} Low Hysteresis	$V_{DD\_TH\_HYST}$	—	500	600	mV	V_{DD} voltage decreasing (Note 1)
I/O Pins – SMCLK, SMDATA, PWR_EN, ALERT#, A_DET#, BOOST# - DC Parameters						
Output Low Voltage	V_{OL}	—	—	0.4	V	I_{SINK_IO} = 8 mA SMDATA, ALERT#, A_DET#, BOOST#
Input High Voltage	V_{IH}	2.0	—	—	V	PWR_EN, SMDATA, SMCLK
Input Low Voltage	V_{IL}	—	—	0.8	V	PWR_EN, SMDATA, SMCLK
Leakage Current	I_{LEAK}	—	—	±5	µA	Powered or unpowered $V_{PULLUP} \leq V_{DD}$ T_A < 85°C (Note 1)
Interrupt Pins – AC Parameters						
ALERT# Pin Blanking Time	t_{BLANK}	—	25	—	ms	Blanking time, coming out of Reset
ALERT# Pin Interrupt Masking Time	t_{MASK}	—	5	—	ms	
BOOST# Pin Minimum Assertion Time	t_{BOOST_MAT}	—	1	—	s	
BOOST# Pin Assertion Current	I_{BOOST}	—	1.9	—	A	
SMBus/I²C Timing						
Input Capacitance	C_{IN}	—	5	—	pF	
Clock Frequency	f_{SMB}	10	—	400	kHz	
Spike Suppression	t_{SP}	—	—	50	ns	
Bus Free Time Stop to Start	t_{BUF}	1.3	—	—	µs	
Start Setup Time	$t_{SU:STA}$	0.6	—	—	µs	
Start Hold Time	$t_{HD:STA}$	0.6	—	—	µs	
Stop Setup Time	$t_{SU:STO}$	0.6	—	—	µs	
Data Hold Time	$t_{HD:DAT}$	0	—	—	µs	When transmitting to the master
Data Hold Time	$t_{HD:DAT}$	0.3	—	—	µs	When receiving from the master
Data Setup Time	$t_{SU:DAT}$	0.6	—	—	µs	
Clock Low Period	t_{LOW}	1.3	—	—	µs	
Clock High Period	t_{HIGH}	0.6	—	—	µs	
Clock / Data Fall Time	t_{FALL}	—	—	300	ns	Min = 20+0.1C_{LOAD} ns (Note 1)
Clock / Data Rise Time	t_{RISE}	—	—	300	ns	Min = 20+0.1C_{LOAD} ns (Note 1)

Note 1: This parameter is characterized, not 100% tested.
2: This parameter is ensured by design and not 100% tested.
3: The current measurement full scale range maximum value is 3.4A. However, the UCS2112 cannot report values above I_{LIM} (if $I_{BUS\_R2MIN} \leq I_{LIM}$) or above I_{BUS_R2MIN} (if $I_{BUS\_R2MIN} > I_{LIM}$ and $I_{LIM} \leq$ 1.6A).

TABLE 1-2: ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Unless otherwise specified, V_{DD} = 4.5V to 5.5V, V_S = 2.9V to 5.5V, V_{PULLUP} = 3V to 5.5V, T_A = -40°C to 105°C. All typical values at V_{DD} = V_S = 5V, T_A = 27°C.

Characteristic	Symbol	Min.	Typ.	Max.	Unit	Conditions
Capacitive Load	C_{LOAD}	—	—	400	pF	Per bus line (Note 1)
Timeout	$t_{TIMEOUT}$	25	—	35	ms	Disabled by default (Note 1)
Idle Reset	t_{IDLE_RESET}	350	—	—	µs	Disabled by default (Note 1)
Port Power Switch						
Port Power Switch – DC Parameter						
Overvoltage Lockout	V_{S_OV}	—	6	—	V	Note 2
V_S Low Threshold	V_{S_UVLO}	—	2.5	—	V	Note 2
V_S Low Hysteresis	$V_{S\_UVLO\_HYST}$	—	100	—	mV	Note 2
On Resistance	R_{ON_PSW}	—	40	60	mΩ	4.75V < V_S < 5.25V
V_S Leakage Current	I_{LEAK_VS}	—	—	5	µA	Sleep state into V_S pin on one channel (Note 1)
Back-Voltage Protection Threshold	V_{BV_TH}	—	150	—	mV	V_{BUS} > V_S V_S > V_{S_UVLO}
Back-drive Current	I_{BD_1}	—	0	3	µA	V_{DD} < V_{DD_TH}, Leakage current from V_{BUS} pins to the V_{DD} and the V_S pins (Note 1)
	I_{BD_2}	—	0	2	µA	V_{DD} > V_{DD_TH}, Leakage current from V_{BUS} pins to the V_{DD} (in Detect State) or the V_S pins (in Active State) (Note 1)
Selectable Current Limits	I_{LIM1}	—	530	—	mA	I_{LIM} Resistor = 0 or 47 kΩ (530 mA setting)
	I_{LIM2}	—	960	—	mA	I_{LIM} Resistor = 10 kΩ or 56 kΩ (960 mA setting)
	I_{LIM3}	—	1070	—	mA	I_{LIM} Resistor = 12 kΩ or 68 kΩ (1070 mA setting)
	I_{LIM4}	—	1280	—	mA	I_{LIM} Resistor = 15 kΩ or 82 kΩ (1280 mA setting)
	I_{LIM5}	—	1600	—	mA	I_{LIM} Resistor = 18 kΩ or 100 kΩ (1600 mA setting)
	I_{LIM6}	—	2130	—	mA	I_{LIM} Resistor = 22 kΩ or 120 kΩ (2130 mA setting)
	I_{LIM7}	2500	2670	2900	mA	I_{LIM} Resistor = 27 kΩ or 150 kΩ (2670 mA setting)
	I_{LIM8}	3000	3200	3400	mA	I_{LIM} Resistor = 33 kΩ or V_{DD} (3200 mA setting)
Pin Wake Time	t_{PIN_WAKE}	—	3	—	ms	
SMBus Wake Time	t_{SMB_WAKE}	—	4	—	ms	

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TABLE 1-2: ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Unless otherwise specified, V_{DD} = 4.5V to 5.5V, V_S = 2.9V to 5.5V, V_{PULLUP} = 3V to 5.5V, T_A = -40°C to 105°C. All typical values at V_{DD} = V_S = 5V, T_A = 27°C.

Characteristic	Symbol	Min.	Typ.	Max.	Unit	Conditions
Idle Sleep Time	t_{IDLE_SLEEP}	—	200	—	ms	
Thermal Regulation Limit	T_{REG}	—	110	—	°C	Die Temperature at which current limit will be reduced
Thermal Regulation Hysteresis	T_{REG_HYST}	—	10	—	°C	Hysteresis for t_{REG} functionality. Temperature must drop by this value before I_{LIM} value restored to normal operation
Thermal Shutdown Threshold	T_{TSD}	—	135	—	°C	Die Temperature at which port power switch will turn off
Thermal Shutdown Hysteresis	T_{TSD_HYST}	—	35	—	°C	After shutdown due to T_{TSD} being reached, die temperature drop required before port power switch can be turned on again
Auto-Recovery Test Current	I_{TEST}	—	190	—	mA	Portable device attached, V_{BUS}= 0V, Die temp < T_{TSD}
Auto-Recovery Test Voltage	V_{TEST}	—	750	—	mV	Portable device attached, V_{BUS} = 0V before application, Die temp < T_{TSD} Programmable, 250 - 1000 mV, default listed
Discharge Impedance	$R_{DISCHARGE}$	—	100	—	W	
Port Power Switch – AC Parameters						
Turn-On Delay	t_{ON_PSW}	—	200	—	ms	Depends on the V_{BUS} Discharge setting. Programmable 100 – 400 ms, default listed
Turn-Off Time	$t_{OFF\_PSW\_INA}$	—	0.75	—	ms	PWR_EN inactive toggle to switch off time C_{BUS} = 120 µF
Turn-Off Time	$t_{OFF\_PSW\_ERR}$	—	1	—	ms	Over-current Error, V_{BUS} Min Error, or Discharge Error to switch off C_{BUS} = 120 µF
Turn-Off Time	$t_{OFF\_PSW\_ERR1}$	—	100	—	ns	TSD or Back-drive Error to switch off C_{BUS} = 120 µF
V_{BUS} Output Rise Time	t_{R_BUS}	—	1.1	—	ms	Measured from 10% to 90% of V_{BUS}, C_{LOAD} = 220 µF I_{LIM} = 1.0A
Soft Turn-On Rate	$\Delta I_{BUS}/\Delta_t$	—	100	—	mA/µs	
Temperature Update Time	t_{DC_TEMP}	—	200	—	ms	

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Characteristic	Symbol	Min.	Typ.	Max.	Unit	Conditions
Short-Circuit Response Time	t_{SHORT_LIM}	—	1.5	—	µs	Time from detection of short to current limit applied. No C_{BUS} applied
Short-Circuit Detection Time	t_{SHORT}	—	6	—	ms	Time from detection of short to port power switch disconnect and ALERT# pin assertion.
Latched Mode Cycle Time	t_{UL}	—	7	—	ms	From PWR_EN edge transition from inactive to active to begin error recovery
Auto-Recovery Mode Cycle Time	t_{CYCLE}	—	25	—	ms	Time delay before error condition check Programmable 15-50 ms, default listed
Auto-Recovery Delay	t_{TST}	—	20	—	ms	Portable device attached, V_{BUS} must be $\geq V_{TEST}$ after this time Programmable 10-25 ms, default listed
Discharge Time	$t_{DISCHARGE}$	—	200	—	ms	Amount of time discharge resistor applied Programmable 100-400 ms, default listed
Port Power Switch Operation With Trip Mode Current Limiting						
Region 2 Current Keep-out	$I_{BUS\_R2MIN\_1}$	—	—	0.1	A	Note 2
Minimum V_{BUS} Allowed at Output	$V_{BUS\_MIN\_1}$	2.0	—	—	V	Note 2
Port Power Switch Operation With Constant Current Limiting (Variable Slope)						
Region 2 Current Keep-out	I_{BUS_R2MIN}	—	—	2.13	A	Note 2
Minimum V_{BUS} Allowed at Output	V_{BUS_MIN}	2.0	—	—	V	Note 2
Current Measurement – DC						
Current Measurement Range	I_{BUS_M}	0	—	3400	mA	Range (Note 2 and Note 3)
Reported Current Measurement Resolution	ΔI_{BUS_M}	—	13.3	—	mA	1 LSB
Current Measurement Accuracy		—	±2	—	%	200 mA < I_{BUS} < I_{LIM}
		—	±2	—	LSB	I_{BUS} < 200 mA

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Characteristic	Symbol	Min.	Typ.	Max.	Unit	Conditions
Current Measurement – AC						
Sampling Rate	—	—	1.1	—	ms	Note 2
Conversion Time both channels	t_{CONV}	—	2.2	—	ms	All registers updated in digital (Note 2)
Charge Rationing – DC						
Accumulated Current Measurement Accuracy	—	—	±4.5	—	%	
Charge Rationing – AC						
Current Measurement Update Time	t_{PCYCLE}	—	1	—	s	
Attach / Removal Detection						
V_{BUS} Bypass – DC						
On Resistance	R_{ON_BYP}	—	45	—	Ω	
Leakage Current	I_{LEAK_BYP}	—	—	3	µA	Switch off T_A < +85°C (Note 1)
Current Limit	I_{DET_CHG}/ I_{BUS_BYP}	—	500	—	µA	V_{DD} = 5V and V_{BUS}> 4.75V
V_{BUS} Charge Time for Attachment	t_{DET_CHARGE}	—	800	—	ms	C_{BUS} = 500 µF maximum
Attach/Removal Detection – DC						
Attach Detection Threshold	I_{DET_QUAL}	—	800	—	µA	Programmable 200-1000 µA, default listed
Primary Removal Detection Threshold	$I_{REM\_QUAL\_ACT}$	—	700	—	µA	Programmable 100-900 µA, default listed. Active power state
	$I_{REM\_QUAL\_DET}$	—	800	—	µA	Programmable, default listed. Detect power state
Attach/Removal Detection – AC						
Attach Detection Time	t_{DET_QUAL}	—	100	—	ms	Time from Attach to A_DET# assert.
Removal Detection Time	t_{REM_QUAL}	—	1000	—	ms	

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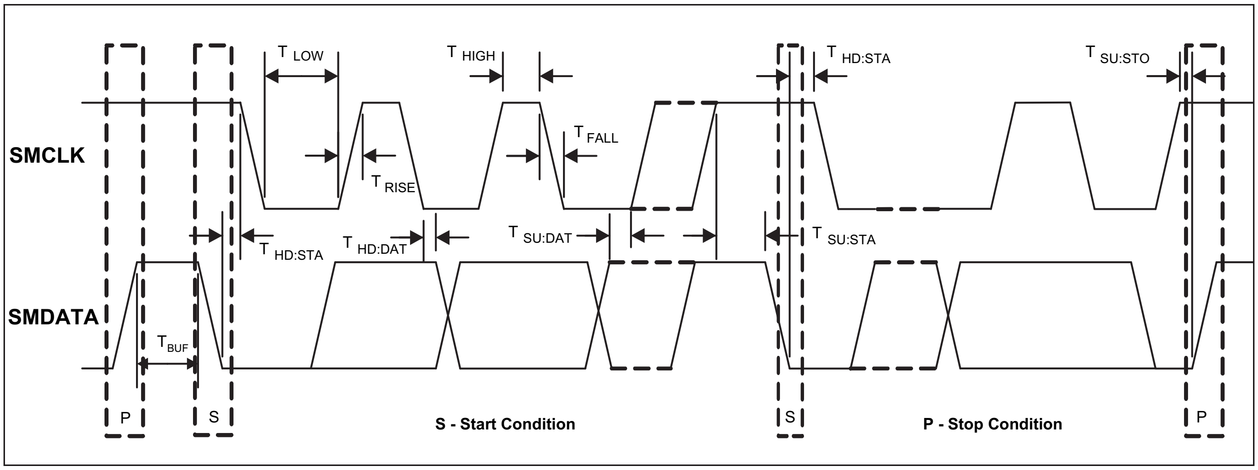


FIGURE 1-1: SMBus Timing.

TABLE 1-3: TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Temperature Range	T_A	-40	—	+105	°C	
Operating Junction Temperature	T_J	-40	—	+125	°C	
Storage Temperature Range	T_A	-55	—	+150	°C	
Thermal Package Resistances – see Table 1-1.						

1.1 ESD and Transient Performance

TABLE 1-4: ESD RATINGS

ESD Specification	Rating or Value
Human Body Model (JEDEC JESD22-A114) – All pins	8 kV
Charged Device Model (JEDEC JESD22-C101) – All pins	500V

1.1.1 HUMAN BODY MODEL (HBM) PERFORMANCE

HBM testing verifies the ability to withstand ESD strikes like those that occur during handling and manufacturing and is done without power applied to the IC. To pass the test, the device must have no change in operation or performance due to the event.

1.1.2 CHARGED DEVICE MODEL (CDM) PERFORMANCE

CDM testing verifies the ability to withstand ESD strikes like those that occur during handling and assembly with pick and place style machinery and is done without power applied to the IC. To pass the test, the device must have no change in operation or performance due to the event.

NOTES:

2.0 TYPICAL PERFORMANCE CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, $V_{DD} = V_S = 5V$, $T_A = +27°C$.

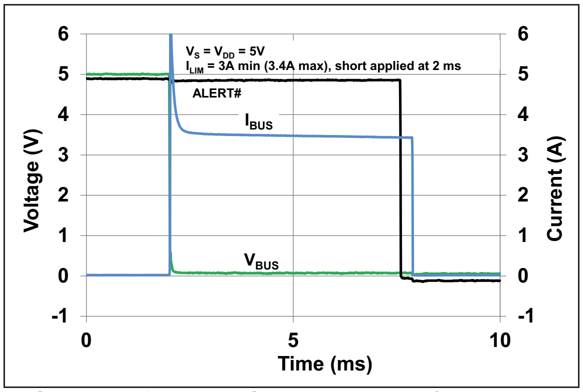


FIGURE 2-1: Short Applied After Power-Up.

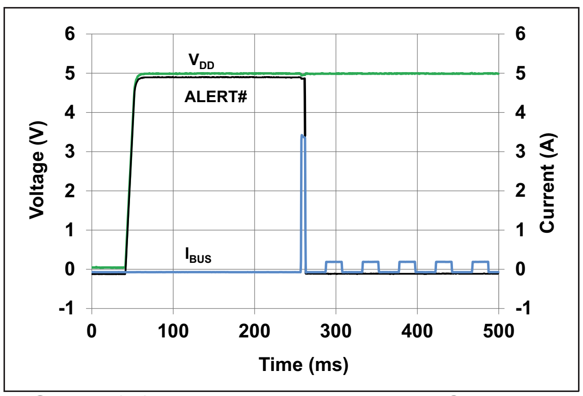


FIGURE 2-2: Power-Up Into a Short.

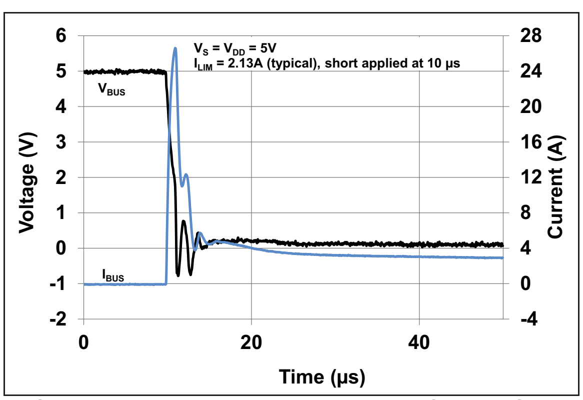


FIGURE 2-3: Internal Power Switch Short Response.

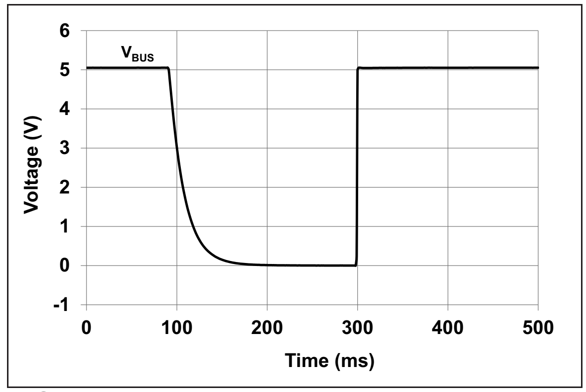


FIGURE 2-4: V_{BUS} Discharge Behavior.

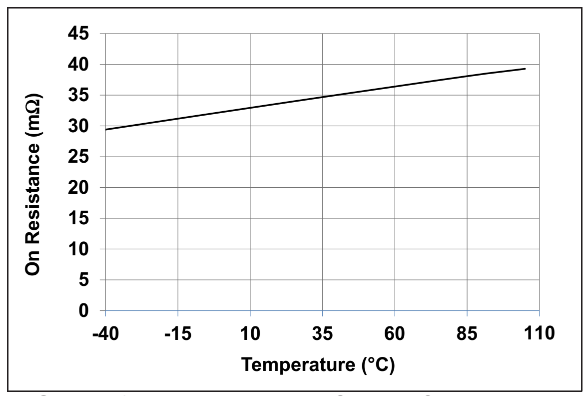


FIGURE 2-5: Power Switch On Resistance vs. Temperature.

Note: Unless otherwise indicated, $V_{DD} = V_S = 5V$, $T_A = +27°C$.

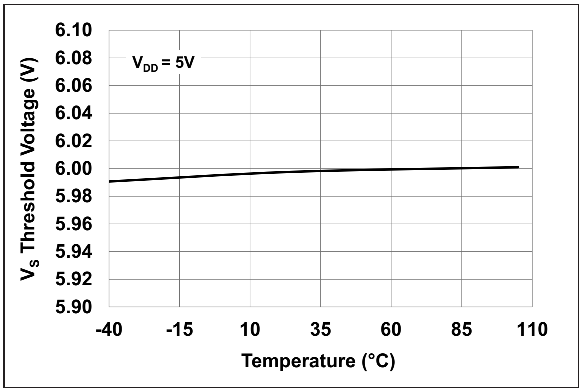


FIGURE 2-6: *V_S Overvoltage Threshold vs. Temperature.*

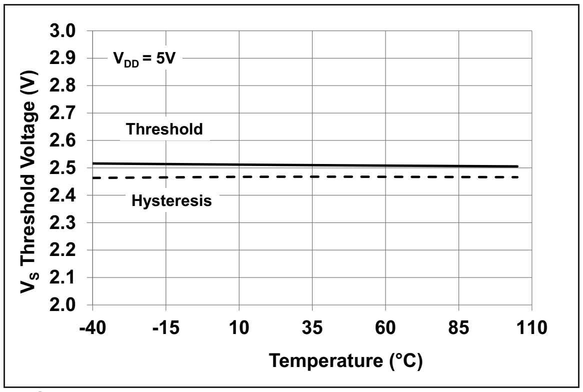


FIGURE 2-7: *V_S Undervoltage Threshold vs. Temperature.*

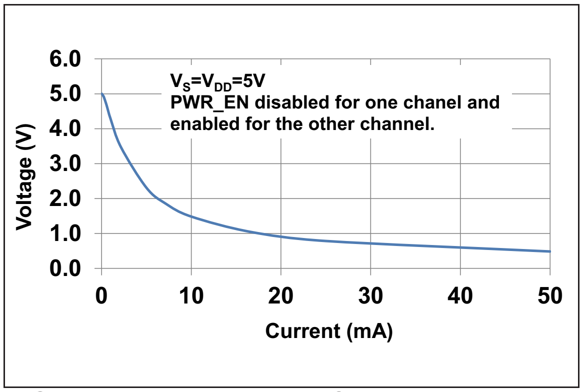


FIGURE 2-8: *Detect State V_{BUS} vs. I_{BUS}.*

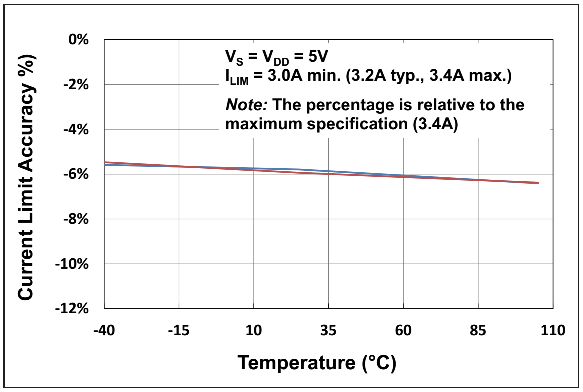


FIGURE 2-9: *Trip Current Limit Operation vs. Temperature.*

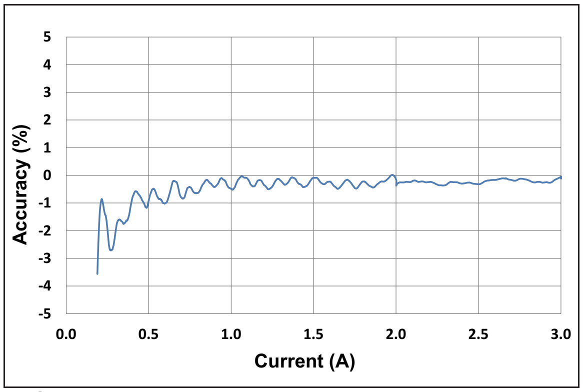


FIGURE 2-10: *I_{BUS} Measurement Accuracy.*

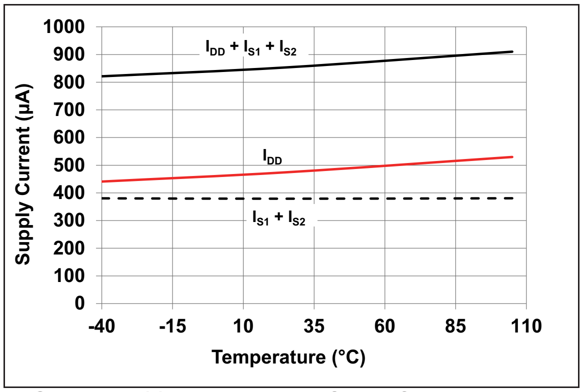


FIGURE 2-11: *Active State Current vs. Temperature (both channels on, PWR_EN1 = PWR_EN2 = 1).*

Note: Unless otherwise indicated, $V_{DD} = V_S = 5V$, $T_A = +27°C$.

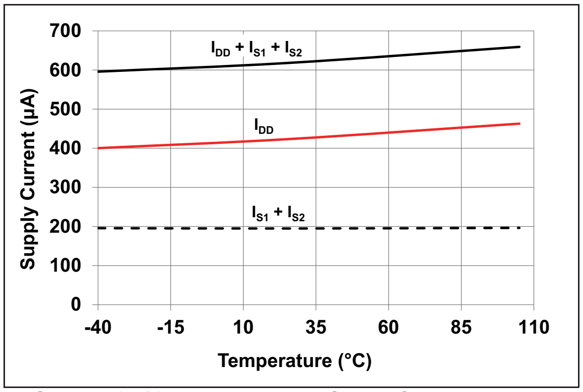


FIGURE 2-12: *Active State Current vs. Temperature (only one channel on, PWR_EN1 = 1, PWR_EN2 = 0).*

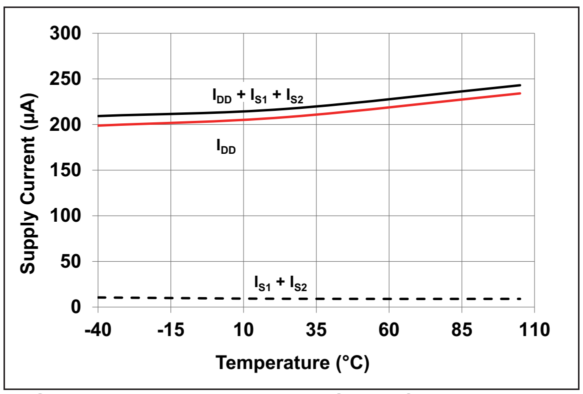


FIGURE 2-13: *Detect State Current vs. Temperature.*

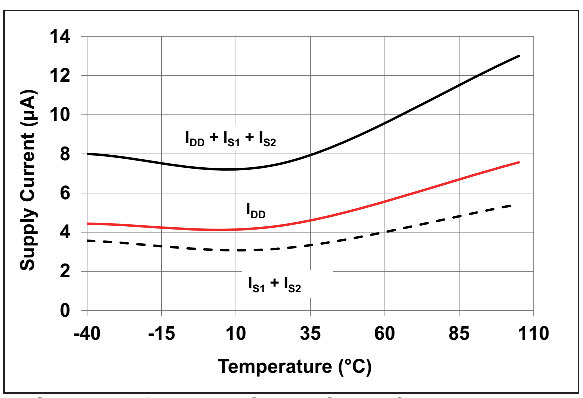


FIGURE 2-14: *Sleep State Current vs. Temperature.*

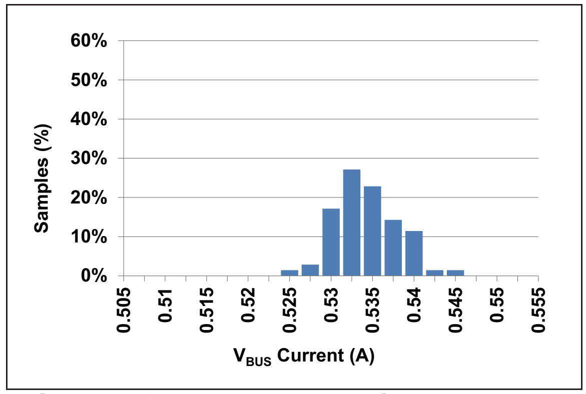


FIGURE 2-15: *ILIM1 Trip Current Distribution.*

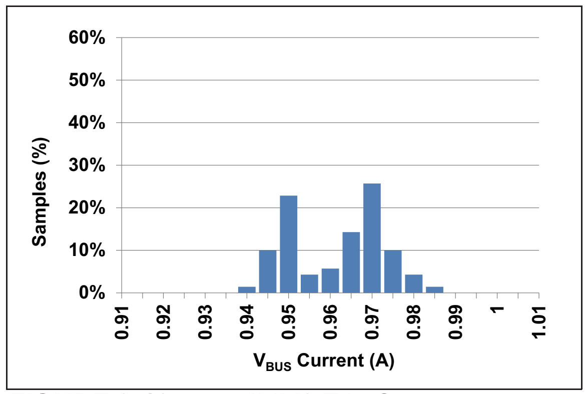


FIGURE 2-16: *ILIM2 Trip Current Distribution[(1)].*

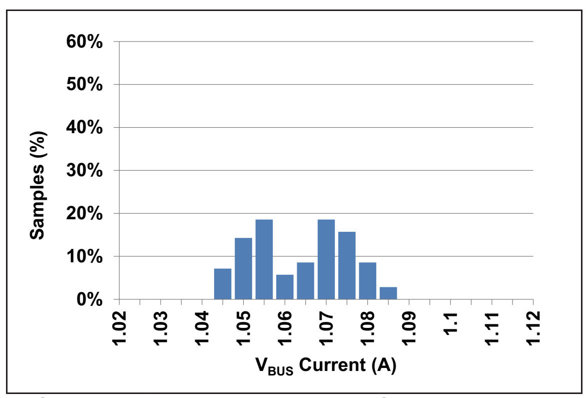


FIGURE 2-17: *ILIM3 Trip Current Distribution[(1)].*

Note 1: The histogram aspect is caused by a mixture of two normal distributions, corresponding to the two V_{BUS} channels.

Note: Unless otherwise indicated, $V_{DD} = V_S = 5V$, $T_A = +27°C$.

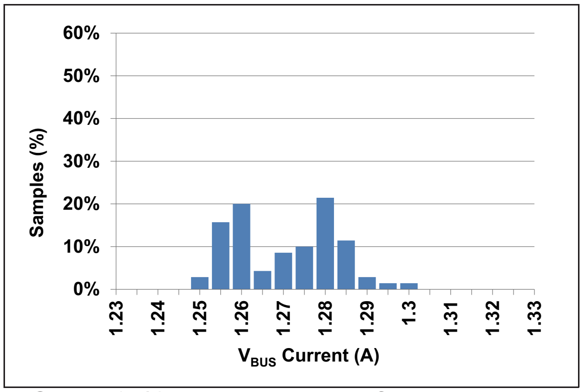


FIGURE 2-18: *ILIM4 Trip Current Distribution[1].*

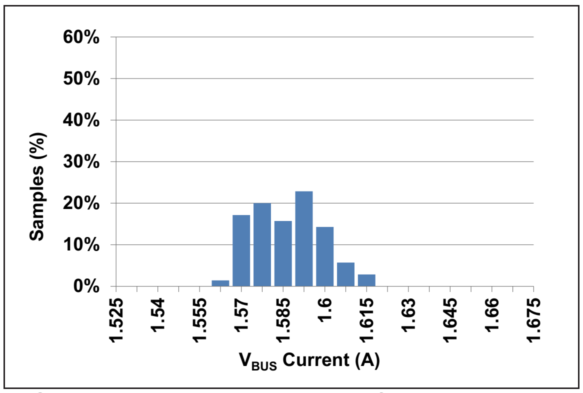


FIGURE 2-19: *ILIM5 Trip Current Distribution[1].*

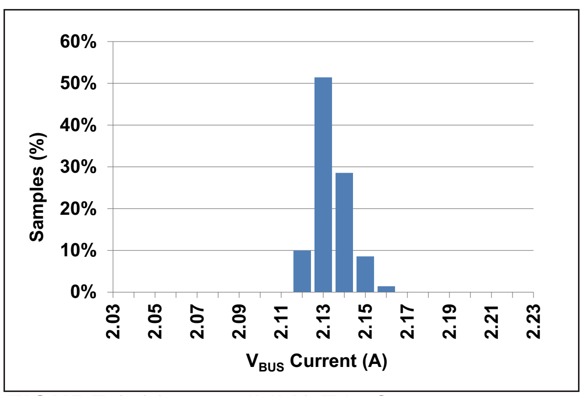


FIGURE 2-20: *ILIM6 Trip Current Distribution.*

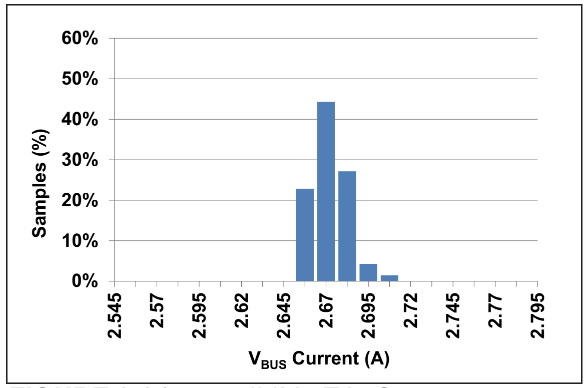


FIGURE 2-21: *ILIM7 Trip Current Distribution.*

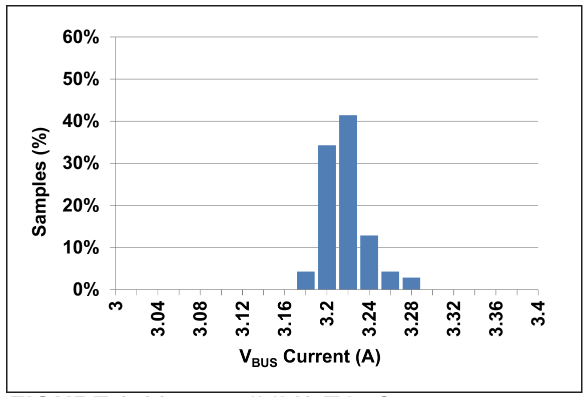


FIGURE 2-22: *ILIM8 Trip Current Distribution.*

Note 1: The histogram aspect is caused by a mixture of two normal distributions, corresponding to the two V_{BUS} channels.

3.0 PIN DESCRIPTION

Descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

UCS2112 4x4 QFN	Symbol	Function	Pin Type	Connection Type if Pin Not Used
1	PWR_EN1	Port power switch enable #1	DI	Connect to ground or V_{DD} (depending on the polarity decoded via COMM_ILIM pin)
2	A_DET#1	Open-drain output for Attach Detection on V_{BUS1} (requires pull-up resistor)	OD	Connect to ground
3	BOOST#	Logic output for DC-DC converter voltage increase (requires pull-up resistor)	OD	Connect to ground
4, 5	V_{BUS1}	Port power switch #1 output (requires both pins tied together)	High Power, AIO	Leave open
6, 7	V_S	Voltage input to port power switch V_{BUS1} (requires both pins tied together)	High Power, AIO	Connect to ground
8	V_{DD}	Common supply voltage	Power	N/A
9, 10	V_S	Voltage input to port power switch V_{BUS2} (requires both pins tied together)	High Power, AIO	Connect to ground
11, 12	V_{BUS2}	Port power switch #2 output (requires both pins tied together)	High Power, AIO	Leave open
13	COMM_ILIM	Enables SMBus or Stand-Alone mode at power-up. Hardware strap for maximum current limit	AIO	N/A
14	A_DET#2	Open-drain output for Attach Detection on V_{BUS2} (requires Pull Up)	OD	Connect to ground
15	PWR_EN2	Port power switch enable #2	DI	Connect to ground or V_{DD} (depending on the polarity decoded via COMM_ILIM pin)
16	ALERT#2	Output fault ALERT for V_{BUS2} (requires pull-up resistor)	OD	Connect to ground
17	SMCLK	SMCLK - SMBus clock input (requires pull-up resistor)	DI	Connect to V_{PULLUP} (or to ground in Stand-alone mode)
18	SMDATA	SMDATA - SMBus data input/output (requires pull-up resistor)	DIOD	Connect to V_{PULLUP} (or to ground in Stand-alone mode)
19	GND	Ground	Power	N/A
20	ALERT#1	Output fault ALERT for V_{BUS1} (requires pull-up resistor)	OD	Connect to ground
21	EP	Exposed thermal pad. Must be connected to electrical ground.	EP	N/A

TABLE 3-2: PIN TYPES

Pin Type	Description
Power	This pin is used to supply power or ground to the device.
Hi-Power	This pin is a high-current pin.
AIO	Analog Input/Output – this pin is used as an I/O for analog signals.
DI	Digital Input – this pin is used as a digital input.
DIOD	Open-Drain Digital Input/Output – this pin is bidirectional. It is open-drain and requires a pull-up resistor.
OD	Open-Drain Digital Output – used as a digital output. It is open-drain and requires a pull-up resistor.
EP	Exposed thermal pad

4.0 TERMS AND ABBREVIATIONS

> **Note:** The PWR_EN1 and PWR_EN2 pins each have Configuration bits ("<pin name>_S" in General Configuration 1 register (Address 11h) and General Configuration 2 register (Address 12h)) that may be used to perform the same function as the external pin state. These bits are accessed via the SMBus/I^{2}C and are OR'd with the respective pin. This OR'd combination of pin state and register bit is referenced as the <pin name> control.

TABLE 4-1: TERMS AND ABBREVIATIONS

Term/Abbreviation	Description
Attach Detection	An Attach Detection event occurs when the current drawn by a portable device is greater than I_{DET_QUAL} for longer than t_{DET_QUAL}.
Attachment	The physical insertion of a portable device into a USB port that UCS2112 is controlling.
CC	Constant Current
CDM	Charged Device Model. JEDEC model for characterizing susceptibility of a device to damage from ESD.
Current Limiting Mode	Determines the action that is performed when the I_{BUS} current reaches the I_{LIM} threshold. Trip opens the port power switch. Constant Current (variable slope) allows V_{BUS} to be dropped by the portable device.
Disconnection	USB-IF term which refers to the loss of active USB communications between a USB host and a USB device.
Dynamic Thermal Management	The UCS2112 automatically adjusts port power switch limits and modes to lower internal power dissipation when the thermal regulation temperature value is approached.
HBM	Human Body Model
I_{BUS_R2MIN}	Current limiter mode boundary
I_{LIM}	The I_{BUS} current threshold used in current limiting. In Trip mode, when I_{LIM} is reached, the port power switch is opened. In Constant Current mode, when the current exceeds I_{LIM}, operation continues at a reduced voltage and increased current; if V_{BUS} voltage drops below V_{BUS_MIN}, the port power switch is opened.
OCL	Overcurrent limit
POR	Power-on Reset
Portable Device	USB device attached to the USB port.
Removal Detection	A Removal Detection event occurs when the current load on the V_{BUS} pin drops to less than I_{REM_QUAL} for longer than t_{REM_QUAL}.
Removal	The physical removal of a portable device from a USB port that the UCS2112 is controlling.
Stand-Alone Mode	Indicates that the communications protocol is not active and all communications between the UCS2112 and a controller are done via the external pins only (PWR_EN1 and PWR_EN2 as inputs, and ALERT1#, ALERT2#, A_DET1# and A_DET2# as outputs).

NOTES:

5.0 GENERAL DESCRIPTION

The UCS2112 is a dual-port power switch. Two USB power ports are supported with current limits up to 3.0A continuous current (3.4A maximum) each. Selectable and programmable current limiting configurations are also available to the application. A typical block diagram is shown in Figure 5-1.

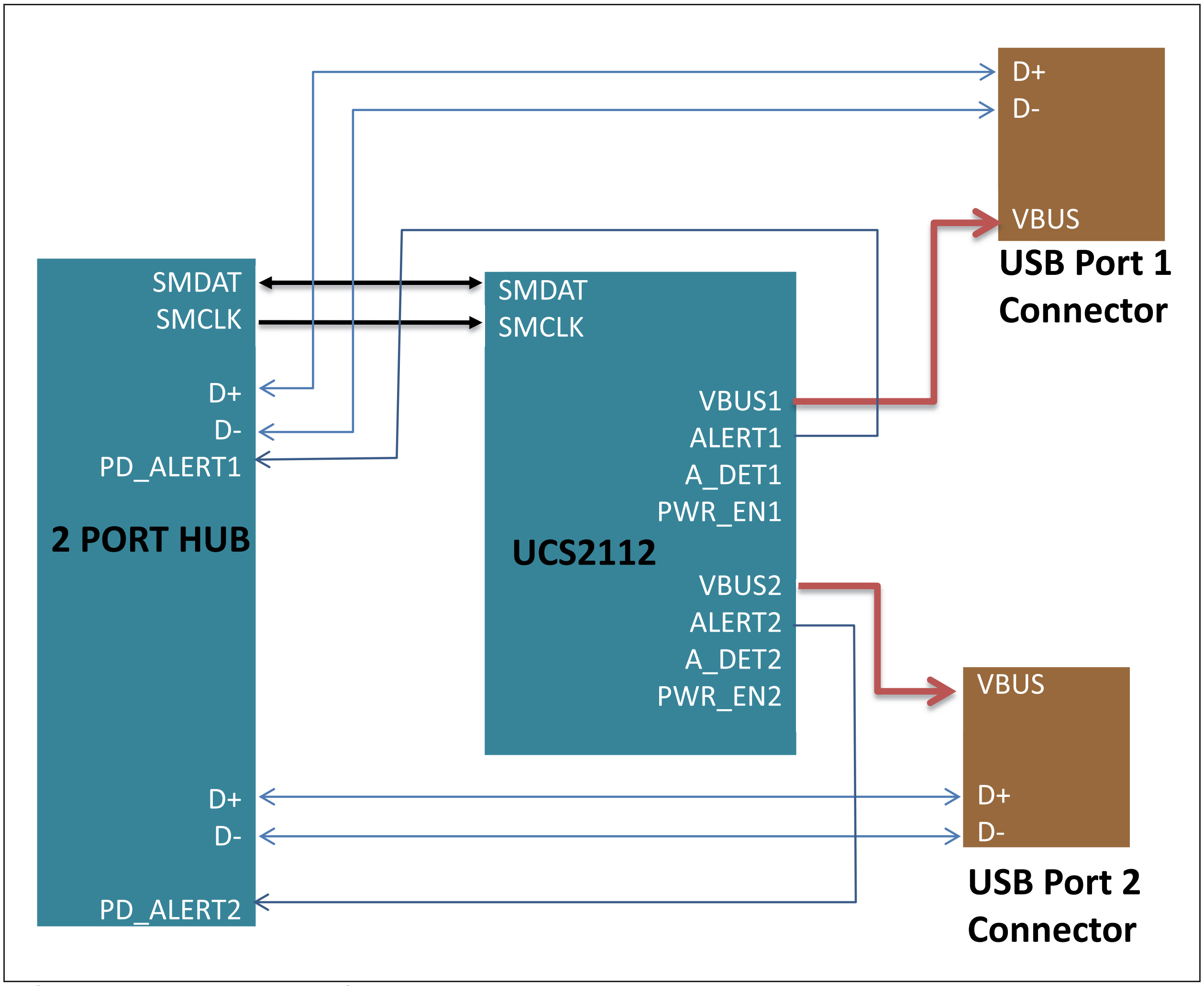


FIGURE 5-1: *Typical USB Application.*

5.1 UCS2112 Power States

Power states are indicators of the device's current consumption in the System and the functionality of the Digital Logic. Table 5-1 details the UCS2112 power states.

TABLE 5-1: POWER STATES DESCRIPTION

State	Description
Off	This power state is entered when the voltage at the V_{DD} pin voltage is < V_{DD_TH}. In this state, the device is considered "off". The UCS2112 will not retain its digital states and register contents nor respond to SMBus/I^2C communications. The port power switch and bypass switch will be off. See **Section 5.1.1 "Off State Operation"**.
Sleep	This is the lowest power state available. While in this state, the UCS2112 will retain digital functionality and wake to respond to SMBus/I^2C communications. See **Section 5.1.2 "Sleep State Operation"**.
Detect	The Detect power state should not be confused with the actual Attach / Removal Detection feature. Detect power state is both channels awaiting attachment. This is a lower-current power state. In this state, the device is actively looking for a portable device to be attached. While in this state, the UCS2112 will retain the configuration and charge rationing data, but it will not monitor the bus current. SMBus/I^2C communications will be fully functional. See **Section 5.1.3 "Detect State Operation"**.
Error	This power state is entered when a Fault condition exists. Error power state is one or both channels in Fault Handling. This state is updated as Priority One. The Interrupt Status registers for each channel will update the fault detected per channel. Only the channel that has detected a fault will be affected since the other channel can remain active if no fault is detected. See **Section 5.1.5 "Error State Operation"**.
Active	Active power state is one, or both channels active and sourcing current to the V_{BUS} Port. This state is updated as Priority Two. None of the channels have detected fault. This power state provides full functionality. While in this state, operations include activation of the port power switch, current limiting, and charge rationing. See **Section 5.1.4 "Active State Operation"**.

Table 5-2 shows the settings for the various power states, except Off and Error. If V_{DD} < V_{DD_TH}, the UCS2112 is in the Off state.

TABLE 5-2: POWER STATES CONTROL SETTINGS

Power State	PWR_EN1	PWR_EN2	ATT_DET	Portable Device Attached	Behavior
Sleep	disabled	disabled	N/A	N/A	• All switches disabled. • V_{BUS} will be near ground potential. • The UCS2112 wakes to respond to SMBus communications.
Detect	enabled	disabled	enabled	No	• Automatic transition to Active state when conditions met for V_{BUS1} (see **Section 5.1.3.1 "Automatic Transition from Detect to Active"**). • V_{BUS2} pins have very low current delivery capability.
	disabled	enabled	enabled	No	• Automatic transition to Active state when conditions met for V_{BUS2} (see **Section 5.1.3.1 "Automatic Transition from Detect to Active"**). • V_{BUS1} pins have very low current delivery capability.
	enabled	enabled	enabled	No	• Automatic transition to Active state when conditions met for both V_{BUS1} and V_{BUS2} (see **Section 5.1.3.1 "Automatic Transition from Detect to Active"**).

TABLE 5-2: POWER STATES CONTROL SETTINGS (CONTINUED)

Power State	PWR_EN1	PWR_EN2	ATT_DET	Portable Device Attached	Behavior
Active	enabled	disabled	N/A	Yes	• Port power switch is on during A_DET1=1 for V_{BUS1}. • V_{BUS2} pins have very low current delivery capability.
	disabled	enabled	N/A	Yes	• Port power switch is on during A_DET2=1 for V_{BUS2}. • V_{BUS1} pins have very low current delivery capability.
	enabled	enabled	N/A	Yes	• Port power switch is on during A_DET1=A_DET2=1 for V_{BUS1} and V_{BUS2}.
	enabled	disabled	disabled	N/A	• Forced ACTIVE Power State: Port power switch is on at all times for V_{BUS1}. • V_{BUS2} pins have very low current delivery capability.
	disabled	enabled	disabled	N/A	• Forced ACTIVE Power State: Port power switch is on at all times for V_{BUS2}. • V_{BUS1} pins have very low current delivery capability.
	enabled	enabled	disabled	N/A	• Forced ACTIVE Power State: Port power switch is on at all times for V_{BUS1} and V_{BUS2}.

5.1.1 OFF STATE OPERATION

The device will be in the Off state if V_{DD} is less than V_{DD_TH}. When the UCS2112 is in the Off state, it will do nothing and all circuitry will be disabled. Digital register values are not stored and the device will not respond to SMBus commands.

5.1.2 SLEEP STATE OPERATION

The PWR_EN1 and PWR_EN2 pins may be used to cause the UCS2112 to enter/exit Sleep. These pins are AND'ed for Sleep mode.

When the UCS2112 is in the Sleep state, the device will be in its lowest-power state. The bypass switch and the port power switch will be disabled. The Attach and Removal Detection feature will be disabled. V_{BUS1} and V_{BUS2} will be near ground potential. The ALERT#1 and ALERT#2 pins will not be asserted. If asserted prior to entering the Sleep state, the ALERT# pin will be released. SMBus activity is limited to single byte read or write.

The first data byte read from the UCS2112 when it is in the Sleep state will wake it; however, the data to be read will return all 0's and should be considered invalid. This is a "dummy" read byte meant to wake the UCS2112. Subsequent read or write bytes will be accepted normally. After the dummy read, the UCS2112 will be in a higher-power state (see Figure 5-2). After communication has not occurred for t_{IDLE_SLEEP}, the UCS2112 will return to Sleep.

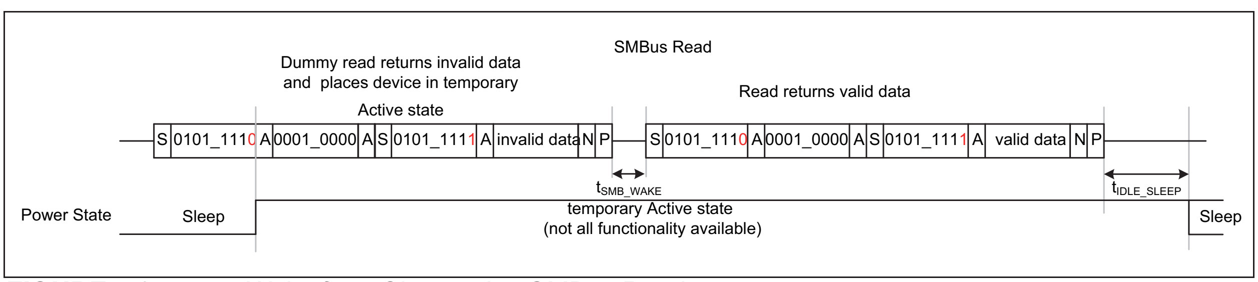


FIGURE 5-2: *Wake from Sleep using SMBus Read.*

5.1.3 DETECT STATE OPERATION

When the UCS2112 is in the Detect state, the port power switch will be disabled. The V_{BUS} output will be connected to the V_{DD} voltage by a secondary bypass switch.

There are two methods for transitioning from the Detect state to the Active state: automatic and host-controlled.

5.1.3.1 Automatic Transition from Detect to Active

For the Detect state, enable PWR_EN1 and/or PWR_EN2, and supply $V_{DD} \geq V_{DD\_TH}$. When a portable device is attached and an Attach Detection event occurs, the UCS2112 will automatically transition to the Active state.

5.1.3.2 State Change from Detect to Active

When conditions cause the UCS2112 to transition from the Detect state to the Active state, the following occurs:

- The Attach Detection feature will be disabled; the Removal Detection feature remains enabled.
- The bypass switch will be turned off.
- The discharge switch will be turned on briefly for $t_{DISCHARGE}$.
- The port power switch will be turned on.

5.1.4 ACTIVE STATE OPERATION

Every time the UCS2112 enters the Active state, the port power switches are closed. The UCS2112 cannot be in the Active state (and therefore, the port power switch cannot be turned on) if any of the following conditions exist:

- $V_S < V_{S\_UVLO}$
- PWR_EN1 and PWR_EN2 are disabled.

5.1.5 ERROR STATE OPERATION

The UCS2112 will enter the Error state from the Active state when any of the following events are detected:

- The maximum allowable internal die temperature (T_{TSD}) has been exceeded.
- An overcurrent condition has been detected.
- An undervoltage condition on either V_{BUS} pin has been detected (see **Section 5.3.4 "Undervoltage Lockout on VS"**).
- A back-drive condition has been detected (see **Section 5.3.2 "Back-voltage Detection"**).
- A discharge error has been detected.
- An overvoltage condition on the V_S pin.

The UCS2112 will enter the Error state from the Detect state when a back-drive condition has been detected on either port, or when the maximum allowable internal die temperature has been exceeded.

The UCS2112 will enter the Error state from the Sleep state when a back-drive condition has been detected.

When the UCS2112 enters the Error state, the port power switch and the V_{BUS} bypass switch will be disabled while the ALERT# pin is asserted (by default). They will remain off while in this power state. The UCS2112 will leave this state as determined by the fault handling selection.

With the auto-recovery fault handler, after the t_{CYCLE} time period, the UCS2112 will check that all of the error conditions have been removed.

If all of the error conditions have been removed, the UCS2112 will return to the Active state or Detect state, as applicable.

If the device is in the Error state and a Removal Detection event occurs, it will check the error conditions and then return to the power state defined.

5.2 Communication

The UCS2112 can operate in SMBus mode (see **Section 8.0 "System Management Bus Protocol"**) or Stand-alone mode. The resistor connected to the COMM_ILIM pin determines the operating mode and the hardware-set I_{LIM} setting, as shown in Table 5-3. Unless connected to GND or V_{DD}, the resistors in Table 5-3 are external pull-down resistors.

The SMBus address is specified in **Section 8.2 "SMBus Address and RD/WR Bit"**.

TABLE 5-3: COMMUNICATION DECODE

COMM_ILIM Pull Down Resistor (±1%)	PWR_EN1 and PWR_EN2 Polarity	I_{LIM} (A)	Total I_{LIM} (A) (Note 1)	Communication Mode
GND	Active-High	0.53	0.53 + 0.53	SMBus
10 kΩ	Active-High	0.96	0.96 + 0.96	SMBus
12 kΩ	Active-High	1.07	1.07 + 1.07	SMBus
15 kΩ	Active-High	1.28	1.28 + 1.28	SMBus
18 kΩ	Active-High	1.6	1.6 + 1.6	SMBus

Note 1: The total maximum current depends on power dissipation characteristics of the design (see Table 1-1).

TABLE 5-3: COMMUNICATION DECODE (CONTINUED)

COMM_ILIM Pull Down Resistor (±1%)	PWR_EN1 and PWR_EN2 Polarity	I_{LIM} (A)	Total I_{LIM} (A) (Note 1)	Communication Mode
22 kΩ	Active-High	2.13	2.13 + 2.13	SMBus
27 kΩ	Active-High	2.67	2.67 + 2.67	SMBus
33 kΩ	Active-High	3.2	3.2 + 3.2	SMBus
47 kΩ	Active-Low	0.53	0.53 + 0.53	Stand-Alone
56 kΩ	Active-Low	0.96	0.96 + 0.96	Stand-Alone
68 kΩ	Active-Low	1.07	1.07 + 1.07	Stand-Alone
82 kΩ	Active-Low	1.28	1.28 + 1.28	Stand-Alone
100 kΩ	Active-Low	1.6	1.6 + 1.6	Stand-Alone
120 kΩ	Active-Low	2.13	2.13 + 2.13	Stand-Alone
150 kΩ	Active-Low	2.67	2.67 + 2.67	Stand-Alone
V_{DD}	Active-Low	3.2	3.2 + 3.2	Stand-Alone

Note 1: The total maximum current depends on power dissipation characteristics of the design (see Table 1-1).

5.3 Supply Voltages

5.3.1 V_{DD} SUPPLY VOLTAGE

The UCS2112 requires 4.5V to 5.5V present on the V_{DD} pin for core device functionality. Core device functionality consists of maintaining register states, wake-up upon SMBus/I^{2}C query and Attach Detection.

5.3.2 BACK-VOLTAGE DETECTION

The back drive detector is functional in all power states (Sleep, Detect, and Active).

When in Sleep, the UCS2112 will enter the Error state from Sleep if a Back Drive condition was detected.

Whenever the following condition is true for either port, the port power switch will be disabled, the V_{BUS} bypass switch will be disabled and a back-voltage event will be flagged. This will cause the UCS2112 to enter the Error power state (see **Section 5.1.5 "Error State Operation"**).

Note:	The V_{BUS} voltage exceeds the V_S and/or the V_{DD} pin voltage by V_{BV_TH} and the port power switch is closed. The port power switch will be opened immediately. If the condition lasts for longer than t_{MASK}, then the UCS2112 will enter the Error state. Otherwise, the port power switch will be turned on as soon as the condition is removed.

5.3.3 BACK-DRIVE CURRENT PROTECTION

If a portable device is attached that is self-powered, it may drive the V_{BUS} port to its power supply voltage level; however, the UCS2112 is designed such that leakage current from the V_{BUS} pins to the V_{DD} and/or the V_S pin shall not exceed I_{BD_1} (if the V_{DD} and/or V_S voltage is zero) or I_{BD_2} (if the V_{DD} and/or V_S voltage exceeds V_{DD_TH}).

5.3.4 UNDERVOLTAGE LOCKOUT ON V_S

The UCS2112 requires a minimum voltage (V_{S_UVLO}) be present on the V_S pin for Active power state.

5.3.5 OVERVOLTAGE DETECTION AND LOCKOUT ON V_S/V_{DD}

The UCS2112 port power switch will be disabled if the voltage on the V_S pin exceeds a voltage (V_{S_OV}) for longer than the specified time (t_{MASK}). This will cause the device to enter the Error state.

5.3.6 PWR_EN1 AND PWR_EN2 INPUT

The PWR_EN control affects the power state and enables the port power switch to be turned on if conditions are met (see Table 5-2). The port power switch cannot be closed if PWR_EN is disabled. However, if PWR_EN is enabled, the port power switch is not necessarily closed (see **Section 5.1.4 "Active State Operation"**). In SMBus mode, the PWR_EN1 and PWR_EN2 pins states will be ignored by the UCS2112 if the PIN_IGN Configuration bit is set; otherwise, the PWR_EN1S and PWR_EN2S Configuration bits are checked along with the pins.

5.4 Discrete Output Pins

5.4.1 ALERT#1 AND ALERT#2 OUTPUT PINS

The UCS2112 has two independent ALERT# out pins. ALERT#1 is tied to the status of the V_{BUS1} pin. ALERT#2 is tied to the status of the V_{BUS2} pin.

The ALERT# pin is an active-low open-drain interrupt to the host controller. The ALERT# pin is asserted when an error occurs. The ALERT# pin can also be asserted when the LOW_CUR (portable device is pulling less current and may be finished charging) or TREG (thermal regulation temperature exceeded) bits are set and linked. Also, when charge rationing is enabled, the ALERT# pin is asserted by default when the current rationing threshold is reached (as determined by RTN_BEH<1:0>). The ALERT# pin is released when all error conditions that may assert the ALERT# pin (such as an error condition, charge rationing, and TREG and LOW_CUR if linked) have been removed or reset as necessary.

5.4.2 BOOST# OUTPUT PIN

The UCS2112 provides a BOOST# output pin to compensate for voltage drops during high loads. The BOOST# pin is an active-low, open-drain output that would be connected to a resistor in the DC-DC Converter's feedback error voltage loop (see Figure 5-3).

The BOOST# pin is asserted when V_{BUS} Current > I_{BOOST}. I_{BOOST} typical value is 1.9A. The BOOST# is OR'ed for both V_{BUS1} and V_{BUS2} ports. When the BOOST# pin is asserted, it will remain in this state for at least t_{BOOST_MAT} (minimum assertion time).

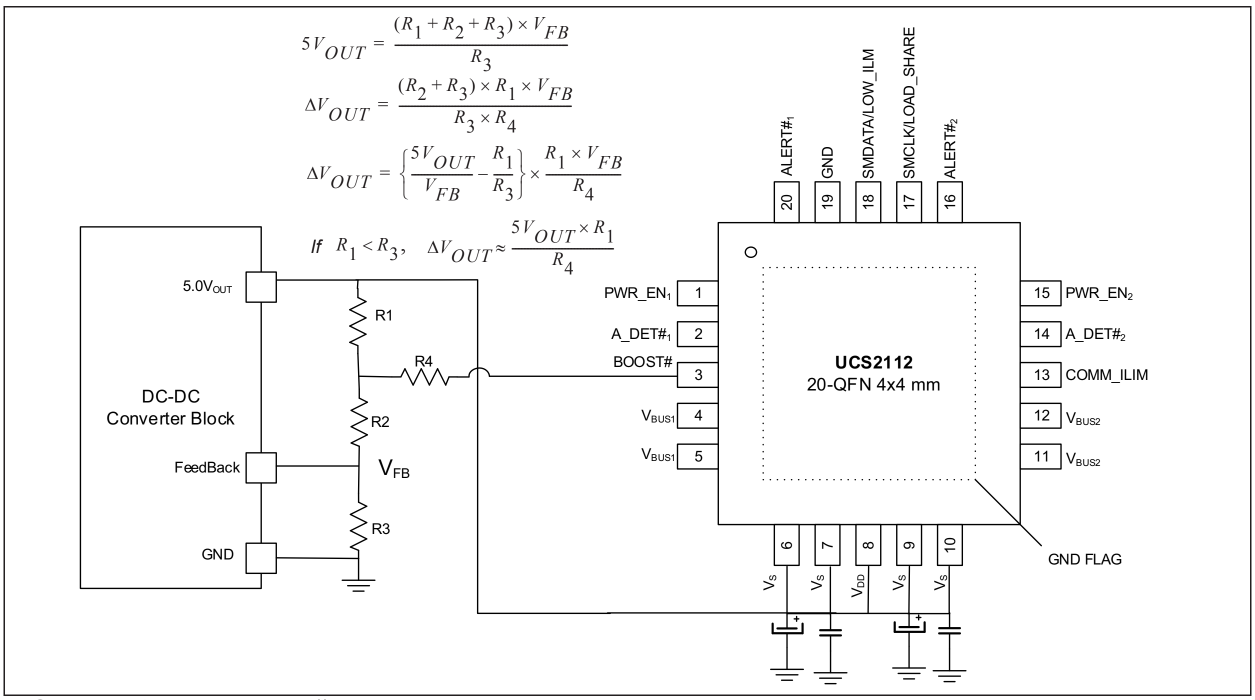


FIGURE 5-3: *Boost# Pin Usage.*

5.5 Discrete Input Pins

5.5.1 COMM_ILIM INPUT

The COMM_ILIM input determines the communications mode, as shown in Table 7-1. This is also the hardware strap for MAX Current Limit.

5.5.2 SMCLK

When operated in Stand-Alone mode, this pin should be tied to ground. When the UCS2112 is configured for SMBus communications, the SMCLK is the clock input.

5.5.3 SMDATA

When used in Stand-Alone, this pin should be tied to ground.

When the UCS2112 is configured for SMBus communications, the SMDATA is the data input/output.

6.0 DETECT STATE

6.1 Device Attach / Removal Detection

The UCS2112 can detect the attachment and removal of a portable device on the V_{BUS1} or V_{BUS2} ports.

Note: By default, device attach / removal detection feature is disabled. It can be enabled by clearing ATT_DISABLE bit 6 in Register 9-9.

6.1.1 V_{BUS} BYPASS SWITCH

The UCS2112 contains circuitry to provide V_{BUS} current as shown in Figure 6-1. In the Detect state, V_{DD} is the voltage source; in the Active state, V_S is the voltage source. The bypass switch and the port power switch are never both on at the same time.

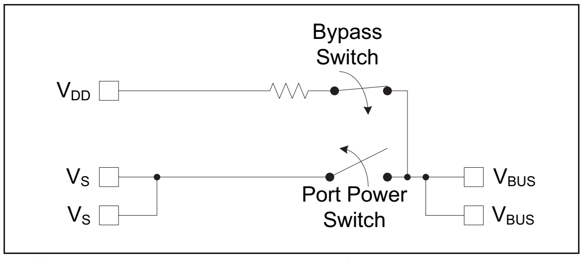


FIGURE 6-1: Bypass Switch.

While the V_{BUS} bypass switch is active, the current available to a portable device will be limited to I_{BUS_BYP} and the Attach Detection feature will be active.

6.1.2 ATTACH DETECTION

The primary Attach Detection feature is only active in the Detect power state. When active, this feature constantly monitors the current load on the V_{BUS1} or V_{BUS2} pins. If the current drawn by a portable device is greater than I_{DET_QUAL} for longer than t_{DET_QUAL}, an Attach Detection event occurs. This will cause the A_DET# Status bits to be set.

Until the port power switch is enabled, the current available to a portable device will be limited to that used to detect device attachment (I_{DET_QUAL}). Once an Attach Detection event occurs, the UCS2112 will wait for the PWR_EN control to be enabled (if not already). When PWR_EN is enabled and V_S is above the threshold, the UCS2112 will activate the V_{BUS} port power switch and operate in Active state.

6.1.3 REMOVAL DETECTION

The Removal Detection feature will be active in the Active and Detect power states. This feature monitors the current load on the V_{BUS1} and V_{BUS2} pins. If this load drops to less than $I_{REM\_QUAL\_DET}$ for longer than t_{REM_QUAL}, a Removal Detection event is flagged.

When a Removal Detection event is flagged, the following will be done:

1. Disable the port power switch and the bypass switch.
2. Set the REM Status register bit.
3. Enable an internal discharging device that will discharge the V_{BUS} line within $t_{DISCHARGE}$.
4. Once the V_{BUS} pin has been discharged, the device will return to the Detect state regardless of the PWR_EN control state.

NOTES:

7.0 USB PORT POWER SWITCH

To assure compliance to various charging specifications, the UCS2112 contains a USB port power switch that supports two current-limiting modes: Trip and Constant current (variable slope). The current limit (I_{LIM}) is pin selectable (and may be updated via the register set). The switch also includes soft start circuitry and a separate short-circuit current limit.

The port power switch is on in the Active state (except when V_{BUS} is discharging).

Note: If a load that draws between 2 mA and 7 mA is connected to the port power switch, a voltage ripple between 40-90 mV_{PP} is observed at the V_{BUS} output. This behavior is normal and it does not affect the charging process when a portable device is connected.

7.1 Current Limiting

7.1.1 CURRENT LIMIT SETTING

The UCS2112 hardware set current limit, I_{LIM}, can be one of eight values. This resistor value is read once upon UCS2112 power-up. The current limit can be changed via the SMBus/I^2C after power-up; however, the programmed current limit cannot exceed the hardware set current limit. Unless connected to V_{DD}, the resistors in Table 7-1 are pull-down resistors.

At power-up, the communication mode (Stand-alone or SMBus/I^2C) and hardware current limit (I_{LIM}) are determined via the pull-down resistor (or pull-up resistor if connected to V_{DD}) on the COMM_ILIM pin, as shown in Table 7-1.

7.1.2 SHORT-CIRCUIT OUTPUT CURRENT LIMITING

Short-circuit current limiting occurs when the output current is above the selectable current limit (I_{LIMx}). This event will be detected and the current will immediately be limited (within t_{SHORT_LIM} time). If the condition remains, the port power switch will flag an Error condition and enter the Error state.

7.1.3 SOFT START

When the PWR_EN control changes states to enable the port power switch, or an Attach Detection event occurs in the Detect power state and the PWR_EN control is already enabled, the UCS2112 invokes a soft start routine for the duration of the V_{BUS} rise time (t_{R_BUS}). This soft start routine will limit current flow from V_S into V_{BUS} while it is active. This circuitry will prevent current spikes due to a step in the portable device current draw.

In the case when a portable device is attached while the PWR_EN pin is already enabled, if the bus current exceeds I_{LIM}, the UCS2112 current limiter will respond within a specified time (t_{SHORT_LIM}) and will operate normally at this point. The C_{BUS} capacitor will deliver the extra current, if any, as required by the load change.

TABLE 7-1: I_{LIM} DECODE

COMM_ILIM Pull Down Resistor (±1%)	PWR_EN1 and PWR_EN2 Polarity	I_{LIM} (A)	Total I_{LIM} (A) (Note 1)
GND	Active-High	0.53	0.53 + 0.53
10 kΩ	Active-High	0.96	0.96 + 096
12 kΩ	Active-High	1.07	1.07 + 1.07
15 kΩ	Active-High	1.28	1.28 + 1.28
18 kΩ	Active-High	1.6	1.6 + 1.6
22 kΩ	Active-High	2.13	2.13 + 2.13
27 kΩ	Active-High	2.67	2.67 + 2.67
33 kΩ	Active-High	3.2	3.2 + 3.2
47 kΩ	Active-Low	0.53	0.53 + 0.53
56 kΩ	Active-Low	0.96	0.96 + 0.96
68 kΩ	Active-Low	1.07	1.07 + 1.07
82 kΩ	Active-Low	1.28	1.28 + 1.28
100 kΩ	Active-Low	1.6	1.6 + 1.6
120 kΩ	Active-Low	2.13	2.13 + 2.13
150 kΩ	Active-Low	2.67	2.67 + 2.67
V_{DD}	Active-Low	3.2	3.2 + 3.2

Note 1: The total maximum current depends on power dissipation characteristics of the design (see Table 1-1).

7.1.4 CURRENT LIMITING MODES

The UCS2112 current limiting has two modes: trip and constant current (variable slope). Either mode functions at all times when the port power switch is closed. When operating in the Detect power state, the current capacity at V_{BUS} is limited to I_{BUS_BYP} as described in **Section 6.1.1 "VBUS Bypass Switch"**.

7.1.4.1 Trip Mode

When using trip current limiting, the UCS2112 USB port power switch functions as a low resistance switch and rapidly turns off if the current limit is exceeded. While operating using trip current limiting, the V_{BUS} output voltage will be held relatively constant (equal to the V_S voltage minus the R_{ON} x I_{BUS} current) for all current values up to the I_{LIM}.

If the current drawn by a portable device exceeds I_{LIM}, the following occurs:

1. The port power switch will be turned off (Trip action).
2. The UCS2112 will enter the Error state and assert the ALERT# pin.
3. The fault handling circuitry will then determine subsequent actions.

Figure 7-1 shows operation of current limits in trip mode with the shaded area representing the USB 2.0 specified V_{BUS} range. Dashed lines indicate the port power switch output will go to zero (e.g., trip) when I_{LIM} is exceeded. Note that operation at all possible values of I_{LIM} are shown in Figure 7-1 for illustrative purposes only; in actual operation only one I_{LIM} can be active at any time.

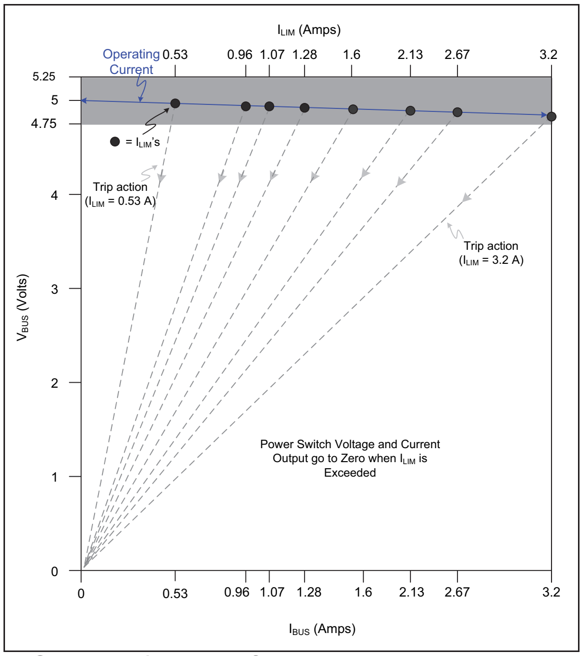


FIGURE 7-1: *Current Limiting in Trip Mode.*

7.1.4.2 Constant Current Limiting (Variable Slope)

Constant current limiting is used when the current drawn is greater than I_{LIM} (and $I_{LIM} \leq 1.6A$). In CC mode, the port power switch allows the attached portable device to reduce V_{BUS} output voltage to less than the input V_S voltage while maintaining current delivery. The V/I slope depends on the user set $_{ILIM}$ value. This slope is held constant for a given I_{LIM} value.

This mode is specifically provided for devices that rely on resistive means to reduce V_{BUS} voltage for direct battery charging or to allow portable devices a means to "test" charger capacity. See Figure 7-2.

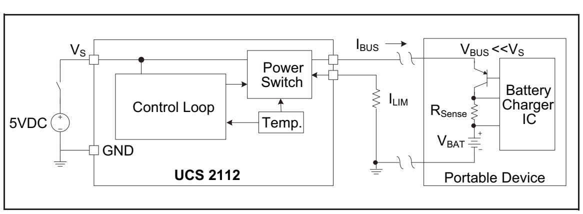


FIGURE 7-2: *Constant Current Example.*

Figure 7-3 shows operation of current limits while using CC mode. Unlike trip mode, once I_{BUS} current exceeds I_{LIM}, operation continues at a reduced voltage and increased current. Note that the shaded area representing the USB 2.0 specified V_{BUS} range is now restricted to an upper current limit of I_{BUS_R2MIN}. Note that the UCS2112 will heat up along each load line as voltage decreases. If the internal temperature exceeds the T_{REG} or T_{TSD} thresholds, the port power switch will open. Also note that when the V_{BUS} voltage is brought low enough (below V_{BUS_MIN}), the port power switch will open.

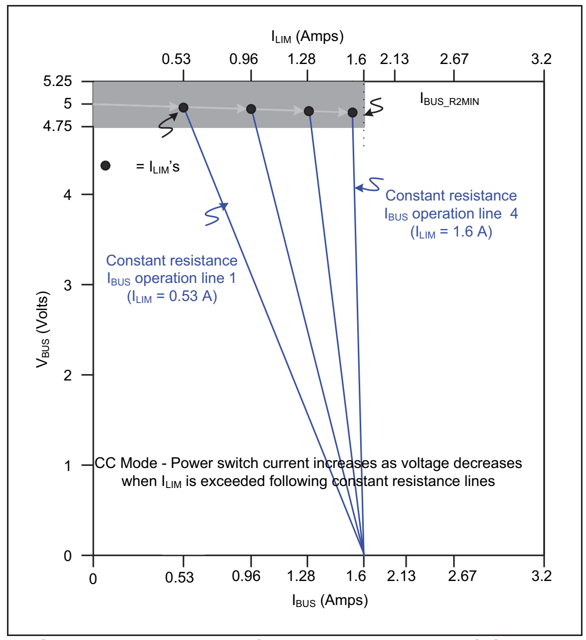


FIGURE 7-3: *Current Limiting in CC Mode.*

7.2 USB Port Power Profiles

The UCS2112 combines the qualities of traditional USB port power switches with USB port power profiles set forth in the USB-IF BC1.2 specification. USB port power profiles consist of distinct voltage-current operation regions defined by "keep-out" and "operation" regions.

While operating in CC mode, the UCS2112 provides voltage-current output operating profiles that are specified by two keep-out regions.

If the current reaches the I_{BUS_R2MIN} setting for longer than t_{MASK}, the UCS2112 enters the Error state and an Overcurrent event is flagged.

If the V_{BUS} voltage ever goes below the no operation lower-voltage keep-out (V_{BUS_MIN}) value for longer than t_{MASK}, the port power switch is disabled and a keep-out violation is flagged (by setting the MIN_KEEP_OUT Status bit). This will cause the device to enter the Error state.

Figure 7-4 illustrates the relationship between these USB port power profile parameters.

7.2.1 OPERATION WITHIN A USB PORT POWER PROFILE

An attached device may be constrained to operate within the boundaries of a USB port power profile by setting the value of I_{LIM} less than the USB port power profile I_{BUS_R2MIN} value. In this case, the port power switch will be in Trip mode up until I_{LIM} is exceeded. At which point, the switch will transition into CC mode. If the attached device reduces the output voltage to less than V_{BUS_MIN}, the switch will trip and terminate charging.

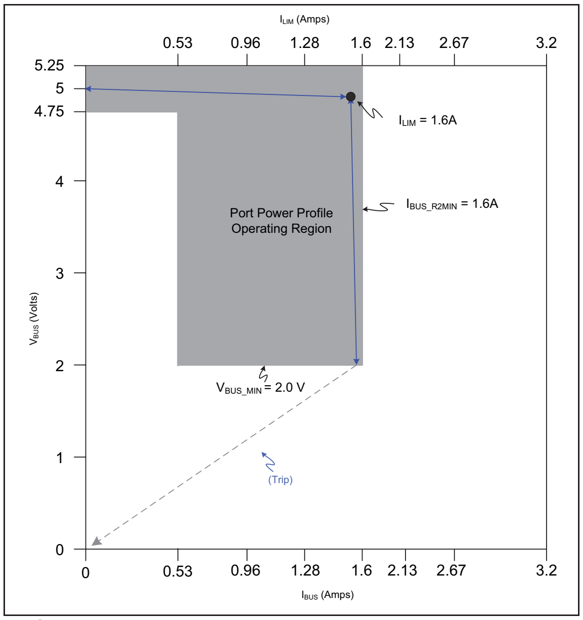


FIGURE 7-4: *$I_{LIM} < I_{BUS\_R2MIN}$ Example.*

> **Note:** The CC mode of operation is possible only up to 1.6A. As long as the value of I_{LIM} is less than the fixed port power profile I_{BUS_R2MIN} value, CC mode is possible. Otherwise, the USB port power switch will operate in trip mode operation.

7.2.2 OPERATION OUTSIDE OF A USB PORT POWER PROFILE

An attached device may be allowed to operate outside of the boundaries of a USB port power profile by setting the value of I_{LIM} greater than the USB port power profile I_{BUS_R2MIN} value. This is the default operation for all portable devices. In this case, the USB port power switch will operate in Trip mode until the bus current reaches the I_{LIM} value. Once the I_{LIM} value has been exceeded, the port power switch will open and terminate charging. Figure 7-5 illustrates an example of current limiting in this configuration.

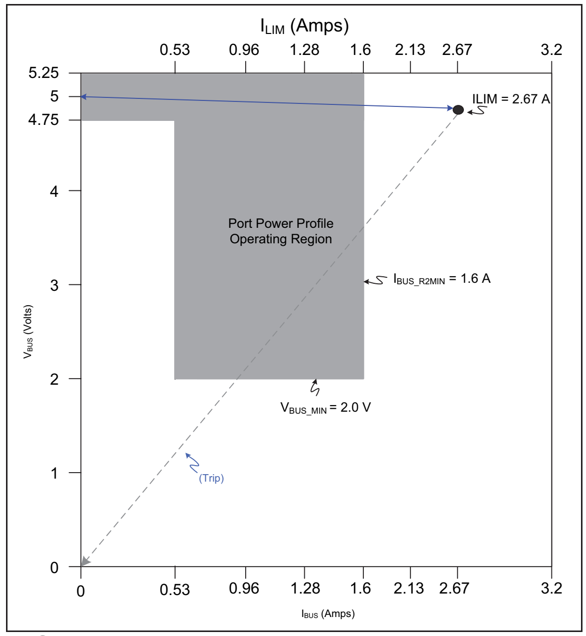


FIGURE 7-5: *$I_{LIM} > I_{BUS\_R2MIN}$ Example.*

7.3 Thermal Management and Voltage Protection

7.3.1 THERMAL MANAGEMENT

The UCS2112 utilizes two-stage internal thermal management. The first stage is Dynamic Thermal Management, and the second stage is Fixed Thermal Shutdown.

7.3.1.1 Dynamic Thermal Management

For the first stage (active in both current-limiting modes), referred to as Dynamic Thermal Management, the UCS2112 automatically adjusts port power switch limits and modes to lower power dissipation when the thermal regulation temperature value is approached, as described in this section.

If the internal temperature exceeds the T_{REG} value, the port power switch is opened, the current limit (I_{LIM}) will be lowered by one step and a timer is started (t_{DC_TEMP}). When this timer expires, the port power switch is closed and the internal temperature will be checked again. If it remains above the T_{REG} threshold, the UCS2112 will repeat this cycle (open port power switch and reduce the I_{LIM} setting by one step) until I_{LIM} reaches its minimum value.

If the UCS2112 is operating using Constant Current Limiting (variable slope) and the I_{LIM} setting has been reduced to its minimum set point and the temperature is still above T_{REG}, the UCS2112 will switch to operating using trip current limiting. This will be done by reducing the I_{BUS_R2MIN} setting to 100 mA and restoring the I_{LIM} setting to the value immediately below the programmed setting (e.g., if the programmed I_{LIM} is 2.13A, the value will be set to 1.6A). If the temperature continues to remain above T_{REG}, the UCS2112 will continue this cycle (open the port power switch and reduce the I_{LIM} setting by one step).

If the UCS2112 internal temperature drops below T_{REG} - T_{REG_HYST}, the UCS2112 will take action based on the following:

1. If the Current Limit mode changed from CC mode to Trip mode, then a timer is started. When this timer expires, the UCS2112 will reset the port power switch operation to its original configuration, allowing it to operate using Constant Current Limiting (variable slope).
2. If the Current Limit mode did not change from CC mode to Trip mode, or was already operating in Trip mode, the UCS2112 will reset the port power switch operation to its original configuration.

If the UCS2112 is operating using Trip Current Limiting and the I_{LIM} setting has been reduced to its minimum set point and the temperature is above T_{REG}, the port power switch will be closed and the current limit will be held at its minimum setting until the temperature drops below T_{REG} - T_{REG_HYST}.

7.3.1.2 Thermal Shutdown

The second stage of thermal management consists of a hardware implemented thermal shutdown corresponding to the maximum allowable internal die temperature (T_{TSD}). If the internal temperature exceeds this value, the port power switches (both ports) will immediately be turned off until the temperature is below T_{TSD} - T_{TSD_HYST}.

7.4 V_{BUS} Discharge

The UCS2112 will discharge V_{BUS} through an internal 100Ω resistor when at least one of the following conditions occurs:

- The PWR_EN control is disabled (triggered on the inactive edge of the PWR_EN control).
- A portable device Removal Detection event is flagged if the Attach/Removal Detect feature is enabled (by default it is disabled).
- The V_S voltage drops below a specified threshold (V_{S_UVLO}) that causes the port power switch to be disabled.
- When commanded into the Sleep power state.
- Upon recovery from the Error state.
- When commanded via the SMBus in the Active state.
- Any time the port power switch is activated after the V_{BUS} bypass switch has been on (i.e., whenever V_{BUS} voltage transitions from being driven from V_{DD} to being driven from V_S, such as going from Detect to Active power state) if the Attach/Removal Detect feature is enabled (by default it is disabled).
- Any time the V_{BUS} bypass switch is activated after the port power switch has been on (i.e., going from Active to Detect power state) if the Attach/Removal Detect feature is enabled (by default it is disabled).

When the V_{BUS} discharge circuitry is activated at the end of the $t_{DISCHARGE}$ time, the UCS2112 will confirm that V_{BUS} was discharged. If the V_{BUS} voltage is not below the V_{TEST} level, a discharge error will be flagged (by setting the DISCH_ERR(1/2) Status bit) and the UCS2112 will enter the Error state.

7.5 Charge Rationing Interactions

When charge rationing is active, regardless of the specified behavior, the UCS2112 will function normally until the charge rationing threshold is reached. Note that charge rationing is only active when the UCS2112 is in the Active state, and it does not automatically reset when a Removal or Attach Detection event occurs. This allows charging of sequential portable devices while charge is being rationed, which means that the accumulated power given to several portable devices will still be held to the stated rationing limit.

Changing the charge rationing behavior will have no effect on the charge rationing data registers. If the behavior is changed prior to reaching the charge rationing threshold, this change will occur and be transparent to the user. When the charge rationing threshold is reached, the UCS2112 will take action as shown in Table 7-2. If the behavior is changed after the charge rationing threshold has been reached, the UCS2112 will immediately adopt the newly programmed behavior, clearing the ALERT# pin and restoring switch operation respectively (see Table 7-4).

TABLE 7-2: CHARGE RATIONING BEHAVIOR

RTN_BEH (1 or 2) <1:0>		Behavior	Actions taken	Notes
1	0			
0	0	Report	ALERT# pin asserted.	
0	1	Report and Disconnect (default)	1. ALERT# pin asserted. 2. Port power switch disconnected.	All bus monitoring is still active. Toggling the PWR_EN control will cause the device to change power states as defined by the registers; however, the port power switch will remain off until the rationing circuitry is reset. Furthermore, the bypass switch will not be turned on if enabled via the Attach Detection.
1	0	Disconnect and Go to Sleep	1. Port power switch disconnected. 2. Device will enter the Sleep state.	All V_{BUS} and V_S monitoring will be stopped. Toggling the PWR_EN control will have no effect on the power state until the rationing circuitry is reset.
1	1	Ignore	Take no further action.	

TABLE 7-3: CHARGE RATIONING RESET BEHAVIOR

Behavior	Reset Actions
Report	1. Reset the Total Accumulated Charge registers. 2. Clear the RATION Status bit. 3. Release the ALERT# pin.
Report and Disconnect	1. Reset the Total Accumulated Charge registers. 2. Clear the RATION Status bit. 3. Release the ALERT# pin. 4. Check the PWR_EN controls and enter the indicated power state if the controls changed.
Disconnect and Go to Sleep	1. Reset the Total Accumulated Charge registers. 2. Clear the RATION Status bit. 3. Check the PWR_EN controls and enter the indicated power state if the controls changed.
Ignore	1. Reset the Total Accumulated Charge registers. 2. Clear the RATION Status bit.

TABLE 7-4: EFFECTS OF CHANGING RATIONING BEHAVIOR AFTER THRESHOLD REACHED

Previous Behavior	New Behavior	Actions Taken
Ignore	Report	Assert ALERT# pin.
	Report and Disconnect	1. Assert ALERT# pin. 2. Open port power switch. See the Report and Disconnect (default) in Table 7-2.
	Disconnect and Go to Sleep	1. Open port power switch. 2. Enter the Sleep state. See the Disconnect and Go to Sleep in Table 7-2.
Report	Ignore	Release ALERT# pin.
	Report and Disconnect	Open port power switch. See the Report and Disconnect (default) in Table 7-2.
	Disconnect and Go to Sleep	1. Release the ALERT# pin. 2. Open the port power switch. 3. Enter the Sleep state. See the Disconnect and Go to Sleep in Table 7-2.
Report and Disconnect	Ignore	1. Release the ALERT# pin. 2. Check the PWR_EN controls and enter the indicated power state if the controls changed.
	Report	Check the PWR_EN controls and enter the indicated power state if the controls changed.
	Disconnect and Go to Sleep	1. Release the ALERT# pin. 2. Enter the Sleep state. See the Disconnect and Go to Sleep in Table 7-2.
Disconnect and go to Sleep	Ignore	Check the PWR_EN controls and enter the indicated power state if the controls changed.
	Report	1. Assert the ALERT# pin. 2. Check the PWR_EN controls and enter the indicated power state if the controls changed.
	Report and Disconnect	1. Assert the ALERT# pin. 2. Check the PWR_EN controls to determine the power state then enter that state except that the port power switch and bypass switch will not be closed.

If the RTN_EN control is set to '0' prior to reaching the charge rationing threshold, rationing will be disabled and the Total Accumulated Charge registers will be cleared. If the RTN_EN control is set to '0' after the charge rationing threshold has been reached, the following additional steps occur:

1. RATION Status bit will be cleared.
2. The ALERT# pin will be released if asserted by the rationing circuitry and no other conditions are present.
3. The PWR_EN controls are checked to determine the power state.

Setting the RTN_RST control to '1' will automatically reset the Total Accumulated Charge registers to 00_00h. If this is done prior to reaching the charge rationing threshold, the data will continue to be accumulated restarting from 00_00h. If this is done after the charge rationing threshold is reached, the UCS2112 will take action as shown in Table 7-3.

7.6 Fault Handling Mechanism

The UCS2112 has two modes for handling faults:

- Latch (latch-upon-fault)
- Auto-recovery (automatically attempt to restore the Active power state after a fault occurs).

If the SMBus is actively utilized, auto-recovery fault handling is the default error handler as determined by the LATCH_SET bit. Faults include overcurrent, overvoltage (on V_S), undervoltage (on V_{BUS}), back-voltage (V_{BUS} to V_S or V_{BUS} to V_{DD}), discharge error, and maximum allowable internal die temperature (T_{TSD}) exceeded. Faults do not include keep-out violations except V_{BUS_MIN}.

7.6.1 AUTO-RECOVERY FAULT HANDLING

When the LATCH_SET bit is low, auto-recovery fault handling is used. When an error condition is detected, the UCS2112 will immediately enter the Error state and assert the ALERT# pin. Independently from the host controller, the UCS2112 will wait a preset time (t_{CYCLE}), check error conditions (t_{TST}), and restore Active operation if the error condition(s) no longer exist. If all other conditions that may cause the ALERT# pin to be asserted have been removed, the ALERT# pin will be released. A short-circuit auto-recovery example is provided in Figure 7-6.

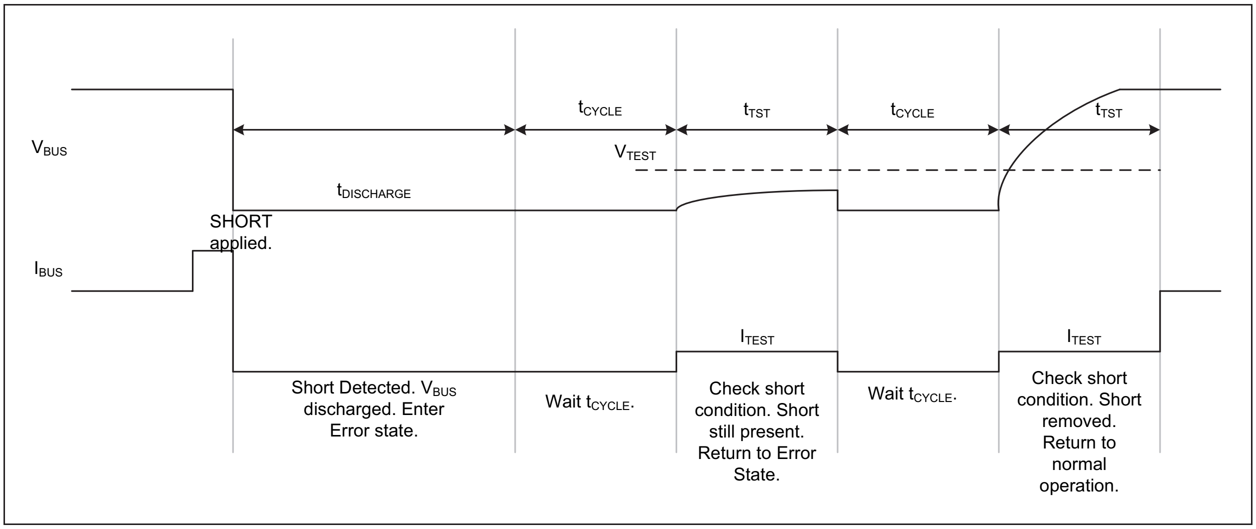


FIGURE 7-6: *Error Recovery.*

7.6.2 LATCHED FAULT HANDLING

When the LATCH_SET bit is high, latch fault handling is used. When an error condition is detected, the UCS2112 will enter the Error power state and assert the ALERT# (1 or 2) pin. Upon command from the host controller (by toggling the PWR_EN (1, or 2) pin control from enabled to disabled or by clearing the ERR bit via SMBus), the UCS2112 will check error conditions once and restore Active operation if error conditions no longer exist. If an error condition still exists, the host controller is required to issue the command again to check error conditions.

If the ALERT# pin is asserted and the Interrupt Status registers (addresses 03h or 04h) are not read, the corresponding ALERT# pin remains asserted until the corresponding PWR_EN pin is toggled.

If the ALERT# pin is asserted and the Interrupt Status registers are read, the ALERT# pin will deassert, but the UCS will remain in error state until the ERR bit is cleared via SMBus or the PWR_EN pin is toggled.

8.0 SYSTEM MANAGEMENT BUS PROTOCOL

In SMBus mode, the UCS2112 communicates with a host controller, such as an Microchip PIC® microcontroller or hub, through the SMBus. The SMBus is a two-wire serial communication protocol between a computer host and its peripheral devices. A detailed timing diagram is shown in Figure 1-1. Stretching of the SMCLK signal is supported; however, the UCS2112 will not stretch the clock signal.

8.1 SMBus Start Bit

The SMBus Start bit is defined as a transition of the SMBus Data line from a logic '1' state to a logic '0' state while the SMBus Clock line is in a logic '1' state.

8.2 SMBus Address and RD/$\overline{WR}$ Bit

The SMBus Address Byte consists of the 7-bit client address followed by the RD/$\overline{WR}$ indicator bit. If this RD/$\overline{WR}$ bit is a logic '0', the SMBus Host is writing data to the client device. If this RD/$\overline{WR}$ bit is a logic '1', the SMBus Host is reading data from the client device.

The UCS2112 with the order code UCS2112-1-V/G4 has the SMBus address 57h - 1010_111(r/$\overline{w}$).

Customers should contact their distributor, representatives or field application engineer (FAE) for additional SMBus addresses. Local sales offices are also available to help customers. A list of sales offices and locations is included in the back of this document.

8.3 SMBus Data Bytes

All SMBus Data bytes are sent Most Significant bit first and composed of 8 bits of information.

8.4 SMBus ACK and NACK Bits

The SMBus client will acknowledge all data bytes that it receives. This is done by the client device pulling the SMBus Data line low after the 8th bit of each byte that is transmitted. This applies to both the Write Byte and Block Write protocols.

The Host will NACK (not acknowledge) the last data byte to be received from the client by holding the SMBus data line high after the 8th data bit has been sent. For the Block Read protocol, the Host will ACK (acknowledge) each data byte that it receives except the last data byte.

8.5 SMBus Stop Bit

The SMBus Stop bit is defined as a transition of the SMBus Data line from a logic '0' state to a logic '1' state while the SMBus clock line is in a logic '1' state. When the UCS2112 detects an SMBus Stop bit and it has been communicating with the SMBus protocol, it will reset its client interface and prepare to receive further communications.

8.6 SMBus Time-out

The UCS2112 includes an SMBus time-out feature. If the clock is held at logic '0' for $t_{TIMEOUT}$, the device can time out and reset the SMBus interface. The SMBus interface can also reset if both the clock and data lines are held at a logic '1' for t_{IDLE_RESET}. Communication is restored with a Start condition.

The time-out function defaults to disabled. It can be enabled by clearing the DIS_TO bit in the General Configuration 3 register (see Register 9-9).

8.7 SMBus and I²C Compliance

The major difference between SMBus and I²C devices is highlighted in this section. For complete compliance information, refer to the SMBus 2.0 specification and Application Note AN14.0 "*Microchip Dedicated Slave Devices in I²C Systems*" (DS00001853).

- UCS2112 supports I²C fast mode at 400 kHz. This covers the SMBus maximum time of 100 kHz.
- The minimum frequency for SMBus communications is 10 kHz.
- The client protocol will reset if the clock is held low longer than 30 ms. This time-out functionality is disabled by default in the UCS2112 and can be enabled by clearing the DIS_TO bit. I²C does not have a time out.
- Except when operating in Sleep, the client protocol will reset if both the clock and the data line are logic '1' for longer than 200 µs (Idle condition). This function is disabled by default in the UCS2112 and can be enabled by clearing the DIS_TO bit. I²C does not have an Idle condition.
- I²C devices do not support the Alert Response Address functionality (which is optional for SMBus).
- I²C devices support block read and write differently. I²C protocol allows for unlimited number of bytes to be sent in either direction. The SMBus protocol requires that an additional data byte indicating number of bytes to read/write is transmitted. The UCS2112 supports I²C formatting only.

8.8 SMBus Protocols

The UCS2112 is SMBus 2.0-compatible and supports Send Byte, Read Byte, Block Read, Receive Byte as valid protocols as shown below. The UCS2112 also supports the I²C block read and block write protocols. The device supports Write Byte, Read Byte, and Block Read/Block Write. All of the below protocols use the convention in Table 8-1.

TABLE 8-1: SMBUS PROTOCOL

Data Sent to Device	Data Sent to the Host
Data sent	Data sent

8.9 SMBus Write Byte

The Write Byte is used to write one byte of data to a specific register as shown in Table 8-2.

TABLE 8-2: WRITE BYTE PROTOCOL

START	Slave Address	WR	ACK	Reg. Addr.	ACK	Register Data	ACK	STOP
1 → 0	YYYY_YYY	0	0	XXh	0	XXh	0	0 → 1

8.10 SMBus Read Byte

The Read Byte protocol is used to read one byte of data from the registers as shown in Table 8-3.

TABLE 8-3: READ BYTE PROTOCOL

START	Slave Address	WR	ACK	Register Address	ACK	
1 → 0	YYYY_YYY	0	0	XXh	0	
START	**Slave Address**	**RD**	**ACK**	**Register Data**	**NACK**	**STOP**
1 → 0	YYYY_YYY	1	0	XXh	1	0 → 1

8.11 Block Write

The Block Write is used to write multiple data bytes to a group of contiguous registers, as shown in Table 8-4. It is an extension of the Write Byte Protocol.

Note: The Block Write and Block Read protocols require that the Address Pointer be automatically incremented. For a write command, the Address Pointer will be automatically incremented when the ACK is sent to the host. There are no over or under bound limit checking and the Address Pointer will wrap around from FFh to 00h if necessary.

TABLE 8-4: BLOCK WRITE PROTOCOL

START	Slave Address	WR	ACK	Register Address	ACK	Repeat N Times		STOP
						Register Data	ACK	
1 → 0	YYYY_YYY	0	0	XXh	0	XXh	0	0 → 1

8.12 Block Read

The Block Read is used to read multiple data bytes from a group of contiguous registers, as shown in Table 8-5. It is an extension of the Read Byte Protocol.

TABLE 8-5: BLOCK READ PROTOCOL

START	Slave Address	WR	ACK	Register Address	ACK			
1 → 0	YYYY_YYY	0	0	XXh	0			
START	**Slave Address**	**RD**	**ACK**	**Repeat N Times**		**Register Data**	**NACK**	**STOP**
				Register Data	**ACK**			
1 → 0	YYYY_YYY	1	0	XXh	0	XXh	1	0 → 1

8.13 SMBus Send Byte

The Send Byte protocol is used to set the internal address register pointer to the correct address location. No data is transferred during the Send Byte protocol as shown in Table 8-6.

> **Note 1:** The SMBus Send Byte command is expected to be followed by the SMBus Receive Byte command. When two SMbus Send Byte commands are sent in a row, the first command receives an ACK and will be processed by the UCS2112, but the second command receives a NACK, and will be ignored.

TABLE 8-6: SEND BYTE PROTOCOL

START	Slave Address	WR	ACK	Register Address	ACK	STOP
1 → 0	YYYY_YYY	0	0	XXh	0	0 → 1

8.14 SMBus Receive Byte

The Receive Byte protocol is used to read data from a register when the internal register Address Pointer is known to be at the right location (e.g., set via Send Byte). This is used for consecutive reads of the same register as shown in Table 8-7.

TABLE 8-7: RECEIVE BYTE PROTOCOL

START	Slave Address	RD	ACK	Register Data	NACK	STOP
1 → 0	YYYY_YYY	1	0	XXh	1	0 → 1

8.14.1 STAND-ALONE OPERATING MODE

Stand-alone mode allows the UCS2112 to operate without active SMBus/I^{2}C communications. Stand-alone mode can be enabled by connecting a pull-down resistor greater or equal to 47 kΩ on the COMM_ILIM pin as shown in Table 5-3.The SMCLK pin should be tied to ground in this mode.

9.0 REGISTER DESCRIPTION

The registers shown in Table 9-1 are accessible through the SMBus or I^2C. An entry of '—' indicates that the bit is not used. Writing to these bits will have no effect and reading these bits will return '0'. Writing to a reserved bit may cause unexpected results and reading from a reserved bit will return either '1' or '0' as indicated in the bit description. While in the Sleep state, the UCS2112 will retain configuration and charge rationing data as indicated in the text. If a register does not indicate that data will be retained in the Sleep power state, this information will be lost when the UCS2112 enters the Sleep power state.

TABLE 9-1: REGISTER SET IN HEXADECIMAL ORDER

Register Address	Register Name	R/W	Function	Default Value	Page No.
00h	Port 1 Current Measurement	R	Stores the current measurement for port 1	00h	38
01h	Port 2 Current Measurement	R	Stores the current measurement for port 2	00h	38
02h	V_{BUS} Port Status	R	Indicates Load Share V_{BUS} Port and general status	00h	39
03h	Interrupt Status1	See Text	Indicates why ALERT# pin asserted for port 1	00h	40
04h	Interrupt Status2	See Text	Indicates why ALERT# pin asserted for port 2	00h	42
0Fh	General Status1	R/R-C	Indicates General Status for port 1	00h	44
10h	General Status2	R/R-C	Indicates General Status for port 2	00h	45
11h	General Configuration1	R/W	Controls basic functionality for port 1	06h	46
12h	General Configuration2	R/W	Controls basic functionality for port 2	02h	47
13h	General Configuration3	R/W	Controls other functionality	60h	48
14h	Current Limit	R/W	Controls/Displays MAX Current Limit per port	00h	49
15h	Auto-Recovery Configuration	R/W	Controls the auto-recovery functionality	2Ah	50
16h	Port 1 Total Accumulated Charge High Byte	R	Stores the total accumulated charge delivered high byte, Port 1	00h	51
17h	Port 1 Total Accumulated Charge Middle High Byte	R	Stores the total accumulated charge delivered middle high byte, Port 1	00h	51
18h	Port 1 Total Accumulated Charge Middle Low Byte	R	Stores the total accumulated charge delivered middle low byte, Port 1	00h	51
19h	Port 1 Total Accumulated Charge Low Byte	R	Stores the total accumulated charge delivered low byte, Port 1	00h	51
1Ah	Port 2 Total Accumulated Charge High Byte	R	Stores the total accumulated charge delivered high byte, Port 2	00h	52
1Bh	Port 2 Total Accumulated Charge Middle High Byte	R	Stores the total accumulated charge delivered middle high byte, Port 2	00h	52
1Ch	Port 2 Total Accumulated Charge Middle Low Byte	R	Stores the total accumulated charge delivered middle low byte, Port 2	00h	52
1Dh	Port 2 Total Accumulated Charge Low Byte	R	Stores the total accumulated charge delivered low byte, Port 2	00h	52
1Eh	Port 1 Charge Rationing Threshold High Byte	R/W	Sets the maximum allowed charge that will be delivered to Port 1	FFh	53
1Fh	Port 1 Charge Rationing Threshold Low Byte	R/W	Sets the maximum allowed charge that will be delivered to Port 1	FFh	53
20h	Port 2 Charge Rationing Threshold High Byte	R/W	Sets the maximum allowed charge that will be delivered to Port 2	FFh	53

TABLE 9-1: REGISTER SET IN HEXADECIMAL ORDER (CONTINUED)

Register Address	Register Name	R/W	Function	Default Value	Page No.
21h	Port 2 Charge Rationing Threshold Low Byte	R/W	Sets the maximum allowed charge that will be delivered to Port 2	FFh	53
22h	Ration Configuration	R/W	Controls Charge Ration Functionality	11h	54
23h	Port 1 Current Limit Behavior	R/W	Controls the Current Limiting Behavior (CC Mode Region 2) for Port 1	96h	55
24h	Port 2 Current Limit Behavior	R/W	Controls the Current Limiting Behavior (CC Mode Region 2) for Port 2	96h	55
FDh	Product ID	R	Stores a fixed value that identifies each product	E1h	56
FEh	Manufacturer ID	R	Stores a fixed value that identifies Microchip	5Dh	56
FFh	Revision	R	Stores a fixed value that represents the revision number	81h	56

9.1 Current Measurement Register

The Current Measurement register stores the measured current value delivered to the portable device (I_{BUS}). This value is updated continuously while the device is in the Active power state.

REGISTER 9-1: PORTS 1 AND 2 CURRENT MEASUREMENT REGISTERS (ADDRESSES 00H, 01H)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
CM(x)<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7:0 **CM(x)<7:0>:** Port X Current Measurement, where x = 1 or 2 (address 00h for Port 1 and address 01h for Port 2) (1) (2).

Note 1: The bit weights are in mA,1 LSB = 13.3 mA (maximum value is 255 LSB corresponding to 3.4A).

2: This data will be cleared when the device enters the Sleep or Detect states. This data will also be cleared whenever the port power switch is turned off (or any time that V_{BUS} is discharged).

9.2 Status Registers

The Status registers store bits that indicate error conditions as well as Attach Detection and Removal Detection.

REGISTER 9-2: V_{BUS} PORT STATUS REGISTER (ADDRESS 02H)

R-0	R-0	R-0	R-0	U-0	U-0	R-0	R-0
ALERT2_PIN	ALERT1_PIN	CC_MODE2	CC_MODE1	—	—	ADET2_PIN	ADET1_PIN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **ALERT2_PIN:** Reflects the status of the ALERT#2 pin. This bit is set and cleared as the ALERT#2 pin changes states.

1 = ALERT#2 Pin asserted (logic low)
0 = ALERT#2 Pin not asserted

bit 6 **ALERT1_PIN:** Reflects the status of the ALERT#1 pin. This bit is set and cleared as the ALERT#1 pin changes states.

1 = ALERT#1 Pin asserted (logic low)
0 = ALERT#1 Pin not asserted

bit 5 **CC_MODE2:** Port2 Constant Current Mode State

1 = Port 2 in Constant Current mode
0 = Port 2 operating normally

bit 4 **CC_MODE1:** Port1 Constant Current Mode State

1 = Port 1 in Constant Current mode
0 = Port 1 operating normally

bit 3-2 **Unimplemented**

bit 1 **ADET2:_PIN** Reflects the status of the A_DET#2 pin. When set, indicates that the A_DET#2 pin is asserted low. This bit is set and cleared as the A_DET#2 pin changes states.

1 = A_DET#2 pin is asserted (logic low)
0 = A_DET#2 pin is not asserted

bit 0 **ADET1_PIN:** Reflects the status of the A_DET#1 pin. When set, indicates that the A_DET#1 pin is asserted low. This bit is set and cleared as the A_DET#1 pin changes states.

1 = A_DET#1 pin is asserted (logic low)
0 = A_DET#1 pin is not asserted

REGISTER 9-3: INTERRUPT STATUS 1 REGISTER (ADDRESS 03H)

R/W-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
ERR1 (1)	DISCH_ERR1	RESET	KEEP_OUT1	TSD	OV_VOLT	BACK_V1	OV_LIM1
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	C = Clear on Read
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **ERR1:** Error Port 1 - Indicates that an error was detected on the V_{BUS1} pin and the device entered the Error state. Writing this bit to ‘0’ will clear the Error state and allows the device to be returned to the Active state. When written to ‘0’, all error conditions are checked. If all error conditions have been removed, the UCS2112 returns to the Active state. This bit is set automatically by the UCS2112 when the Error state is entered. If any other bit is set in the Interrupt Status register (03h), the device will not leave the Error state.

This bit is cleared automatically by the UCS2112 if the auto-recovery fault handling functionality is active and no error conditions are detected. Likewise, this bit is cleared when the PWR_EN1 control is disabled (Note 1).

1 = Port 1 in Error State.
0 = Port 1 in Active State (no errors detected).

bit 6 **DISCH_ERR1:** Discharge Error Port 1 – indicates the device was unable to discharge Port1. This bit will be cleared when read if the error condition has been removed or if the ERR bit is cleared. This bit will cause the ALERT#1 pin to be asserted and the device to enter the Error state.

1 = UCS2112 was unable to discharge V_{BUS1}.
0 = No V_{BUS1} discharge error.

bit 5 **RESET:** Indicates that the UCS2112 has just been reset and should be re-programmed. This bit will be set at power-up. This bit is cleared when read or when the PWR_EN control is toggled. The ALERT# pins are not asserted when this bit is set. This data is retained in the Sleep state.

1 = UCS2112 has just been reset.
0 = Reset did not occur.

bit 4 **KEEP_OUT1:** Port 1 Minimum Keep-out region – Indicates that the V-I output on the V_{BUS1} pin has dropped below V_{BUS_MIN}. This bit will be cleared when read if the error condition has been removed or if the ERR1 bit is cleared. This bit will cause the ALERT#1 pin to be asserted and the device to enter the Error state.

1 = $V_{BUS1} < V_{BUS\_MIN}$
0 = $V_{BUS1} > V_{BUS\_MIN}$

bit 3 **TSD:** Thermal Shutdown – Indicates that the internal temperature has exceeded T_{TSD} threshold and the device has entered the Error state. This bit will be cleared when read if the error condition has been removed or if the ERR1 bit is cleared. This bit will cause the ALERT#1and ALERT#2 pins to be asserted and the device to enter the Error state.

1 = Thermal Shutdown Temperature reached.
0 = Internal temperature < T_{TSD}

bit 2 **OV_VOLT:** V_S Overvoltage Indicates that the V_S voltage has exceeded the V_{S_OV} threshold, and the device has entered the Error state. This bit will be cleared when read if the error condition has been removed or if the ERR1 bit is cleared. This bit will cause the ALERT#1 and ALERT#2 pins to be asserted and the device to enter the Error state.

1 = $V_S > V_{S\_OV}$
0 = $V_S < V_{S\_OV}$

REGISTER 9-3: INTERRUPT STATUS 1 REGISTER (ADDRESS 03H) (CONTINUED)

bit 1 **BACK_V1:** Back-Bias Voltage Port 1 – Indicates that the V_{BUS1} voltage has exceeded the V_S or V_{DD} voltages by more than 150 mV. This bit will be cleared when read if the error condition has been removed or if the ERR1 bit is cleared. This bit will cause the ALERT#1 pin to be asserted and the device to enter the Error state.

1 = $V_{BUS1} > V_S$, or $V_{BUS1} > V_{DD}$ by more than 150 mV.
0 = V_{BUS1} voltage has not exceeded the V_S and V_{DD} voltages by more than 150 mV.

bit 0 **OV_LIM1:** Overcurrent Limit Port 1 – Indicates that the I_{BUS} current has exceeded both the I_{LIM} threshold and the I_{BUS_R2MIN} threshold settings for V_{BUS1}. This bit will be cleared when read if the error condition has been removed or if the ERR1 bit is cleared. This bit will cause the ALERT#1 pin to be asserted and the device to enter the Error state.

1 = Current Limit for Port 1 exceeded
0 = Current Limit for Port 1 not exceeded

Note 1: Note that the ERR1 bit does not necessarily reflect the ALERT#1 pin status. The ALERT#1 pin may be cleared or asserted without the ERR1 bit changing states.

REGISTER 9-4: INTERRUPT STATUS 2 REGISTER (ADDRESS 04H)

R/W-0	R/C-0	R-0	R/C-0	R/C-0	U-0	R/C-0	R/C-0
ERR2 [(1)]	DISCH_ERR2	VS_LOW	KEEP_OUT2	TREG	—	BACK_V2	OV_LIM2
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	C = Clear on Read
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **ERR2:** Error Port 2 – Indicates that an error was detected on the V_{BUS1} pin and the device entered the Error state. Writing this bit to a '0' will clear the Error state and allows the device to be returned to the Active state. When written to '0', all error conditions are checked. If all error conditions have been removed, the UCS2112 returns to the Active state. This bit is set automatically by the UCS2112 when the Error state is entered. If any other bit is set in the Interrupt Status register (04h), the device will not leave the Error state. This bit is cleared automatically by the UCS2112 if the auto-recovery fault handling functionality is active and no error conditions are detected. Likewise, this bit is cleared when the PWR_EN2 control is disabled (Note 1).

1 = Port 2 in Error State.

0 = Port 2 in Active State (no errors detected).

bit 6 **DISCH_ERR2:** Discharge Error Port 2 – indicates the device was unable to discharge Port2. This bit will be cleared when read if the error condition has been removed or if the ERR bit is cleared. This bit will cause the ALERT#2 pin to be asserted and the device to enter the Error state.

1 = Device was unable to discharge V_{BUS2}.

0 = No V_{BUS2} discharge error.

bit 5 **VS_LOW:** Indicates that the V_S voltage has fallen below the V_{S_UVLO} threshold and both V_{BUS1} and V_{BUS2} port power switches are held off. This bit is cleared automatically when the V_S voltage is above the V_{S_UVLO} threshold.

1 = V_S voltage has fallen below the V_{S_UVLO}.

0 = V_S voltage is above V_{S_UVLO}.

bit 4 **KEEP_OUT2:** Port 2 Minimum Keep-out region – Indicates that the V-I output on the V_{BUS2} pin has dropped below V_{BUS_MIN}. This bit will be cleared when read if the error condition has been removed or if the ERR2 bit is cleared. This bit will cause the ALERT#2 pin to be asserted and the device to enter the Error state.

1 = $V_{BUS2} < V_{BUS\_MIN}$

0 = $V_{BUS2} > V_{BUS\_MIN}$

bit 3 **TREG:** Thermal Regulation – Indicates that the internal temperature has exceeded T_{REG} and that the current limit has been reduced. This bit is cleared when read and will not cause the ALERT#1 and ALERT#2 pins to be asserted unless the ALERT_LINK bit is set.

1 = Internal temperature > T_{REG}

0 = Internal temperature < T_{REG}

bit 2 **Unimplemented:** Read as '0'

bit 1 **BACK_V2:** Back-Bias Voltage Port 2 – Indicates that the V_{BUS2} voltage has exceeded the V_S or V_{DD} voltages by more than 150 mV. This bit will be cleared when read if the error condition has been removed or if the ERR2 bit is cleared. This bit will cause the ALERT#2 pin to be asserted and the device to enter the Error state.

1 = $V_{BUS2} > V_S$, or $V_{BUS2} > V_{DD}$ by more than 150 mV.

0 = V_{BUS2} voltage has not exceeded the V_S and V_{DD} voltages by more than 150 mV.

REGISTER 9-4: INTERRUPT STATUS 2 REGISTER (ADDRESS 04H) (CONTINUED)

bit 0 **OV_LIM2:** Overcurrent Limit Port 2 – Indicates that the I_{BUS} current has exceeded both the I_{LIM} threshold and the I_{BUS_R2MIN} threshold settings for V_{BUS2}. This bit will be cleared when read if the error condition has been removed or if the ERR2 bit is cleared. This bit will cause the ALERT#2 pin to be asserted and the device to enter the Error state.

1 = Current Limit for Port 2 exceeded
0 = Current Limit for Port 2 not exceeded.

Note 1: Note that the ERR2 bit does not necessarily reflect the ALERT#2 pin status. The ALERT#2 pin may be cleared or asserted without the ERR2 bit changing states.

REGISTER 9-5: GENERAL STATUS 1 REGISTER (ADDRESS 0FH)

R/C-0	U-x	U-x	R-0	R-0	R/C-0	R/C-0	R-0
RATION1	—	—	CC_MODE1	PWR_EN1_CON	LOW_CUR1	REM1	ADET1
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	C = Clear on Read
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **RATION1:** Indicates the state of Port 1 Rationing. This bit is cleared when read, or cleared automatically when the RTN_RST1 bit is set or the RTN_EN1 bit is cleared.
1 = Port 1 has delivered the programmed mAh of current
0 = Port 1 has not delivered the programmed mAh of current

bit 6-5 **Unimplemented**

bit 4 **CC_MODE1:** Indicates whether Port 1 has entered CC mode.
1 = Port 1 is in CC mode
0 = Port 1 not in CC mode

bit 3 **PWR_EN1_CON:** Reflects the PWR_EN control state. This bit is set and cleared automatically with the logic expression: (PWR_EN1 pin OR PWR_EN1S).
1 = Port 1 Power Enable is set
0 = Port 1 Power Enable is clear

bit 2 **LOW_CUR1:** Indicates if the portable device charge current is below the 13.3 mA threshold on the V_{BUS1} and may have finished charging. This bit is cleared when read and will cause the ALERT#1 pin to be asserted if the ALERT_LINK1 bit is set.
1 = Port 1 charging current less than threshold
0 = Port 1 charging current above threshold

bit 1 **REM1:** Removal Detection Port1 – Indicates if a Removal Detection event has occurred and there is no longer a portable device present on the V_{BUS1} pin. This bit is cleared when read and will not cause the ALERT#1 pin to be asserted.
1 = Removal Detection occurred
0 = No Removal Detection

bit 0 **ADET1:** Attach Detection Port1 – Indicates that an Attach Detection event has occurred on the V_{BUS1} pins and there is a new portable device present. Asserts the A_DET#1 pin. This bit is set and cleared as the A_DET#1 pin changes.
1 = Attach Detection event has occurred. A_DET#1 pin asserted
0 = No Attach Detection event

REGISTER 9-6: GENERAL STATUS 2 REGISTER (ADDRESS 10H)

R/C-0	U-x	U-x	R-0	R-0	R/C-0	R/C-0	R-0
RATION2	—	—	CC_MODE2	PWR_EN2_CON	LOW_CUR2	REM2	ADET2
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	C = Clear on Read
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **RATION2:** Indicates the state of Port 2 Rationing. This bit is cleared when read, or cleared automatically when the RTN_RST2 bit is set or the RTN_EN2 bit is cleared.
1 = Port 2 has delivered the programmed mAh of current
0 = Port 2 has not delivered the programmed mAh of current

bit 6-5 **Unimplemented**

bit 4 **CC_MODE2:** Indicates whether Port 2 has entered CC mode.
1 = Port 2 is in CC mode
0 = Port 2 not in CC mode

bit 3 **PWR_EN2_CON:** Reflects the PWR_EN control state. This bit is set and cleared automatically with the logic expression: (PWR_EN2 pin OR. PWR_EN2S).
1 = Port 2 Power Enable is set
0 = Port 2 Power Enable is clear

bit 2 **LOW_CUR2:** Indicates if the portable device charge current is below the 13.3 mA threshold on the V_{BUS2} and may have finished charging. This bit is cleared when read and will cause the ALERT#2 pin to be asserted if the ALERT_LINK2 bit is set.
1 = Port 2 charging current less than threshold
0 = Port 2 charging current above threshold

bit 1 **REM2:** Removal Detection Port2 - Indicates if a Removal Detection event has occurred and there is no longer a portable device present on the V_{BUS1} pin. This bit is cleared when read and will not cause the ALERT#2 pin to be asserted.
1 = Removal Detection occurred
0 = No Removal Detection

bit 0 **ADET2:** Attach Detection Port2 - indicates that an Attach Detection event has occurred on the V_{BUS2} pins and there is a new portable device present. Asserts the A_DET#2 pin. This bit is set and cleared as the A_DET#2 pin changes.
1 = Attach Detection event has occurred. A_DET#2 pin asserted
0 = No Attach Detection event

9.3 Configuration Registers

The Configuration registers control basic device functionality. The contents of these registers are retained in Sleep.

REGISTER 9-7: GENERAL CONFIGURATION 1 REGISTER (ADDRESS 11H)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-0
ALERT1_MASK	ALERT1_LINK	DSCHG1	PWR_EN1S	DISCHG_TIME<1:0>		ATT_TH1<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	C = Clear on Read
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **ALERT1_MASK:** Mask errors for all interrupts in Register 9-3 except OV_LIM1 and TSD.
1 = The ALERT#1 pin will only assert if a OV_LIM1 or TSD is detected.
0 = The ALERT#1 pin will be asserted if an error condition or indicator event is detected.

bit 6 **ALERT1_LINK:** Links the ALERT#1 pin to be asserted when the LOW_CUR1 bit is set.
1 = The ALERT#1 pin will be asserted if the LOW_CUR1 indicator bit is set.
0 = The ALERT#1 pin will not be asserted if the LOW_CUR1 indicator bit is set.

bit 5 **DSCHG1:** Forces the V_{BUS1} to be reset and discharged when the UCS2112 is in the Active state. Writing this bit to a logic '1' will cause the port power switch to be opened and the discharge circuitry to activate and discharge V_{BUS}. Actual discharge time is controlled by DISCHG_TIME<1:0>. This bit is self-clearing.
1 = V_{BUS1} discharge initiated.
0 = Port 1 not in discharge

bit 4 **PWR_EN1S:** Power Enable Port 1 override – This bit is OR'ed with the PWR_EN1 pin. Thus, if the polarity is set to active-high, either the PWR_EN1 pin or this bit must be '1' to enable the port power switch.

bit 3-2 **DISCHG_TIME<1:0>:** Discharge time Port 1 – sets $t_{DISCHARGE}$. The discharge time value is the same for both ports.
00 = 100 ms
01 = 200 ms
10 = 300 ms
11 = 400 ms

bit 1-0 **ATT_TH1<1:0>:** Attach Detection Threshold Port 1 – determines the current draw needed to determine an Attach event has occurred. It also controls the Removal Detection current level (Note 1).
00 = 200 µA Attach/100 µA Removal
01 = 400 µA Attach/300 µA Removal
10 = 800 µA Attach/700 µA Removal
11 = 1000 µA Attach/900 µA Removal

Note 1: The removal threshold is different when operating in the Active power state versus when operating in the Detect power state.

REGISTER 9-8: GENERAL CONFIGURATION 2 REGISTER (ADDRESS 12H)

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-1	R/W-0
ALERT2_MASK	ALERT2_LINK	DSCHG2	PWR_EN2S	—	—	ATT_TH2<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	C = Clear on Read
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **ALERT2_MASK:** Mask errors for all interrupts in Register 9-4 except OV_LIM2 and TSD.
1 = The ALERT#2 pin will only assert if a OV_LIM2 or TSD is detected.
0 = The ALERT#2 pin will be asserted if an error condition or indicator event is detected.

bit 6 **ALERT2_LINK:** Links the ALERT#2 pin to be asserted when the LOW_CUR2 or TREG bits are set.
1 = The ALERT#2 pin will be asserted if the LOW_CUR2 or TREG indicator bit is set.
0 = The ALERT#2 pin will not be asserted if the LOW_CUR2 or TREG indicator bit is set.

bit 5 **DSCHG2:** Forces the V_{BUS2} to be reset and discharged when the UCS2112 is in the Active state. Writing this bit to a logic ‘1' will cause the port power switch to be opened and the discharge circuitry to activate to discharge V_{BUS}. Actual discharge time is controlled by DISCHG_TIME<1:0>. This bit is self-clearing.
1 = V_{BUS2} discharge initiated.
0 = Port 2 not in discharge

bit 4 **PWR_EN2S:** Power Enable Port 2 override – This bit is OR’ed with the PWR_EN2 pin. Thus, if the polarity is set to active-high, either the PWR_EN2 pin or this bit must be ‘1’ to enable the port power switch.

bit 3-2 **Unimplemented**

bit 1-0 **ATT_TH2<1:0>:** Attach Detection Threshold Port 2 – determines the current draw needed to determine an Attach event has occurred. It also controls the Removal Detection current level (Note 1).
00 = 200 µA Attach/100 µA Removal
01 = 400 µA Attach/300 µA Removal
10 = 800 µA Attach/700 µA Removal
11 = 1000 µA Attach/900 µA Removal

Note 1: The removal threshold is different when operating in the Active power state versus when operating in the Detect power state.

REGISTER 9-9: GENERAL CONFIGURATION 3 REGISTER (ADDRESS 13H)

R/W-0	R/W-1	R/W-1	R-0	R-0	R/W-0	U-0	U-0
PIN_IGN	ATT_DIS	DIS_TO	PWR_STATE<1:0> (1)		BOOST	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	C = Clear on Read
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **PIN_IGN:** Ignores the PWR_EN1 and PWR_EN2 pin states when determining the power state. This bit is retained in Sleep.
1 = PWR_EN1 and PWR_EN2 pin states are ignored.
0 = Power state is determined by the OR’d combination of the PWR_EN1 and PWR_EN2 pins states and the corresponding PWR_EN1S and PWR_EN2S bit states.

bit 6 **ATT_DIS:** Attach Detect Disable – Disables the Attach and Removal Detection feature and affects the power state (see Table 5-2). Setting this bit to 1 forces Active state provided the PWR_EN 1/2 control is enabled.
1 = Attach/Removal Detection disabled.
0 = Attach/Removal Detection enabled.

bit 5 **DIS_TO:** Disable Time Out – Disables the SMBus time out feature.
1 = Time out disabled
0 = Time out enabled

bit 4-3 **PWR_STATE<1:0>:** Current Power State – These bits indicate the current power state. See Note 1
00 = SLEEP
01 = DETECT
10 = ACTIVE
11 = ERROR

bit 2 **BOOST:** Indicates that the I_{BUS} current is higher than I_{BOOST} on V_{BUS1} or V_{BUS2} (bit is OR’ed).
1 = I_{BUS} has exceeded I_{BOOST} on either or both ports
0 = I_{BUS} is less than I_{BOOST} on either port individually

bit 1-0 **Unimplemented**

Note 1: Accessing the SMBus/I²C causes the UCS2112 to leave the Sleep state. As a result, the PWR_STATE<1:0> bits will never read as 00b.

9.4 Current Limit Register

The Current Limit register controls the I_{LIM} used by the port power switch. The default setting is based on the resistor on the COMM_ILIM pin and this value cannot be changed to be higher than hardware set value. The contents of this register are retained in Sleep.

REGISTER 9-10: CURRENT LIMIT REGISTER (ADDRESS 14H)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	ILIM_PORT2<2:0>			ILIM_PORT1<2:0>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5-3 **ILIM_PORT2<2:0>:** Sets the I_{LIM} value for port 2.

000 = 0.53A
001 = 0.96A
010 = 1.07A
011 = 1.28A
100 = 1.6A
101 = 2.13A
110 = 2.67A
111 = 3.2A

bit 2-0 **ILIM_SW<2:0>:** Sets the I_{LIM} value for port 1.

000 = 0.53A
001 = 0.96A
010 = 1.07A
011 = 1.28A
100 = 1.6A
101 = 2.13A
110 = 2.67A
111 = 3.2A

9.5 Auto-Recovery Register

The contents of this register are retained in Sleep.

The Auto-Recovery Configuration register sets the parameters used when the auto-recovery fault handling algorithm is invoked. Once the auto-recovery fault handling algorithm has checked the overtemperature and back-drive conditions, it will set the I_{LIM} value to I_{TEST} and then turn on the port power switch and start the t_{TST} timer. If, after the timer has expired, the V_{BUS} voltage is less than V_{TEST}, then it is assumed that a short-circuit condition is present and the Error state is restarted for auto recovery.

REGISTER 9-11: AUTO RECOVERY CONFIGURATION REGISTER (ADDRESS 15H)

R/W-0	R/W-0	R/W-1	R/W-0	R/W-1	R/W-0	R/W-1	R/W-0
LATCHS	TCYCLE<2:0>			TTST<1:0>		VTST_SW<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **LATCHS:** Latch Set – Controls the fault-handling routine that is used in the case that an error is detected.

1 = Error state will be latched. In order for the UCS2112 to return to normal Active state, the ERR bit must be cleared by the user.
0 = The UCS2112 will automatically retry when an error condition is detected.

bit 6-4 **TCYCLE<2:0>:** Defines the delay (t_{CYCLE}) after the Error state is entered before the auto-recovery fault handling algorithm is started as shown below.

000 = 15 ms
001 = 20 ms
010 = 25 ms
011 = 30 ms
100 = 35 ms
101 = 40 ms
110 = 45 ms
111 = 50 ms

bit 3-2 **TTST<1:0>:** Retry Duration timer – Sets the t_{TST} as shown below.

00 = 10 ms
01 = 15 ms
10 = 20 ms
11 = 25 ms

bit 1-0 **VTST_SW:** Short-circuit Voltage Threshold V_{TEST} voltage threshold that must be crossed during retries to declare the short removed.

00 = 250 mV
01 = 500 mV
10 = 750 mV
11 = 1000 mV

9.6 Total Accumulated Charge Registers

The Total Accumulated Charge registers store the total accumulated charge delivered from the V_S source to a portable device. The bit weighting of the registers is given in mA-hrs. The register value is reset to `00_00h` only when the RTN_RST bit is set or if the RTN_EN bit is cleared (see Register 9-16). This value will be retained when the device transitions out of the Active state and resumes accumulation if the device returns to the Active state and charge rationing is still enabled.

These registers are updated every one (1) second while the UCS2112 is in the Active power state. Every time the value is updated, it is compared against the target value in the Charge Rationing Threshold registers. This data is retained in the Sleep state.

REGISTER 9-12: PORT1 TOTAL ACCUMULATED CHARGE REGISTERS (ADDRESS 16H, 17H, 18H, 19H)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
TAC1<25:18>							
bit 31							bit 24

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
TAC1<17:10>							
bit 23							bit 16

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
TAC1<9:2>							
bit 15							bit 8

R-0	R-0	U-0	U-0	U-0	U-0	U-0	U-0
TAC1<1:0>		—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-6	**TAC1<25:0>:** Total Accumulated Charge Port 1 – Each LSB of this 26-bit value equals 0.00367 mAh.
bit 5-0	**Unimplemented:** Read as '0'

REGISTER 9-13: PORT2 TOTAL ACCUMULATED CHARGE REGISTER (ADDRESS 1AH,1BH,1CH,1DH)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
TAC2<25:18>							
bit 31							bit 24

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
TAC2<17:10>							
bit 23							bit 16

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
TAC2<9:2>							
bit 15							bit 8

R-0	R-0	U-0	U-0	U-0	U-0	U-0	U-0
TAC2<1:0>		—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-6	**TAC2<25:0>:** Total Accumulated Charge Port 2 – Each LSB of this 26-bit value equals 0.00367 mAh.
bit 5-0	**Unimplemented:** Read as ‘0’

9.7 Charge Rationing Threshold Registers

The Charge Rationing Threshold registers set the maximum allowed charge that will be delivered to a portable device. Every time the Total Accumulated Charge registers are updated, the value is checked against this limit. If the value meets or exceeds this limit, the RATION1/RATION2 bit is set and action taken according to the RTN_BEH1<1:0> and RTN_BEH2<1:0> bits in Register 9-16: Ration Configuration Register (Address 22h).

REGISTER 9-14: PORT 1 CHARGE RATIONING THRESHOLD REGISTERS (ADDRESS 1EH,1FH)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
CT1<15:8>							
bit 15							bit 8

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
CT1<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **CT1<15:0>:** Charge Rationing Threshold Port 1 – Each LSB of this 16-bit value equals 3.76 mAh.

REGISTER 9-15: PORT 2 CHARGE RATIONING THRESHOLD REGISTERS (ADDRESS 20H, 21H)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
CT2<15:8>							
bit 15							bit 8

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
CT2<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **CT2:** Charge Rationing Threshold Port 2 – Each LSB of this 16-bit value equals 3.76 mAh.

REGISTER 9-16: RATION CONFIGURATION REGISTER (ADDRESS 22H)

R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-1
RTN_EN2	RTN_RST2	RTN_BEH2<1:0>		RTN_EN1	RTN_RST1	RTN_BEH1<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **RTN_EN2:** Charge Ration Enable Port 2 – Enables Charge Rationing for Port 2.

1 = Charge Rationing enabled

0 = Charge Rationing disabled. The Total Accumulated Charge registers for port 2 will be cleared to 00_00h and current data will no longer be accumulated. If the Total Accumulated Charge registers have already reached the Charge Rationing Threshold, the applied response will be removed as if the charge rationing had been reset. This will also clear the RATION2 Status bit (if set).

bit 6 **RTN_RST2:** Port 2 Ration Reset – Resets the charge rationing functionality for port 2.

1 = Total Accumulated Charge registers are reset to 00_00h. In addition, when this bit is set, the RATION2 Status bit will be cleared and, if there are no other errors or active indicators, the ALERT#2 pin will be released.

0 = Normal operation. This bit must be cleared to enable charge rationing.

bit 5-4 **RTN_BEH2<1:0>:** Ration Behavior Control bits – Controls how the UCS2112 responds when the Ration Threshold has been exceeded (as shown in Table 7-2).

00 = Report
01 = Report and Disconnect
10 = Disconnect and SLEEP
11 = Ignore

bit 3 **RTN_EN1:** Charge Ration Enable Port 1 – Enables Charge Rationing for Port 1.

1 = Charge Rationing enabled

0 = Charge Rationing disabled. The Total Accumulated Charge registers for port 1 will be cleared to 00_00h and current data will no longer be accumulated. If the Total Accumulated Charge registers have already reached the Charge Rationing Threshold, the applied response will be removed as if the charge rationing had been reset. This will also clear the RATION1 Status bit (if set).

bit 2 **RTN_RST1:** Port 1 Ration Reset – Resets the charge rationing functionality for port 1.

1 = Total Accumulated Charge registers are reset to 00_00h. In addition, when this bit is set, the RATION1 Status bit will be cleared and, if there are no other errors or active indicators, the ALERT#1 pin will be released.

0 = Normal operation. This bit must be cleared to enable charge rationing.

bit 1-0 **RTN_BEH1<1:0>:** Ration Behavior Control bits – Controls how the UCS2112 responds when the Ration Threshold has been exceeded (as shown in Table 7-2).

00 = Report
01 = Report and Disconnect
10 = Disconnect and SLEEP
11 = Ignore

9.8 Current Limit Behavior Registers

The Current Limit Behavior register stores the values used by the applied current limiting mode (trip or CC). The contents of this register are not retained in Sleep.

REGISTER 9-17: PORT 1 CURRENT LIMIT BEHAVIOR REGISTER (ADDRESS 23H)

R/W-1	R/W-0	U-0	R/W-1	R/W-0	R/W-1	R/W-1	R/W-0
SEL_VBUS1_MIN<1:0>		—	SEL_R2_IMIN1<2:0>			Reserved	Reserved
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **SEL_VBUS1_MIN<1:0>:** Define the V_{BUS_MIN} voltage for port 1 as follows:
00 = 1.50V
01 = 1.75V
10 = 2.0V
11 = 2.25V

bit 5 **Unimplemented**

bit 4-2 **SEL_R2_IMIN1<2:0>:** Defines the I_{BUS_R2MIN} current.
000 = 100 mA
001 = 530 mA
010 = 960 mA
011 = 1280 mA
100 = 1600 mA
101 = 2130 mA

bit 1-0 **Reserved:** Do not change.

REGISTER 9-18: PORT 2 CURRENT LIMIT BEHAVIOR REGISTER (ADDRESS 24H)

R/W-1	R/W-0	U-0	R/W-1	R/W-0	R/W-1	R/W-1	R/W-0
SEL_VBUS2_MIN<1:0>		—	SEL_R2_IMIN2<2:0>			Reserved	Reserved
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **SEL_VBUS2_MIN<1:0>:** Define the V_{BUS_MIN} voltage for port 2 as follows:
00 = 1.50V
01 = 1.75V
10 = 2.0V
11 = 2.25V

bit 5 **Unimplemented**

bit 4-2 **SEL_R2_IMIN2<2:0>:** Defines the I_{BUS_R2MIN} current.
000 = 100 mA
001 = 530 mA
010 = 960 mA
011 = 1280 mA
100 = 1600 mA
101 = 2130 mA

bit 1-0 **Reserved**: Do not change.

9.9 Product ID Register

The Product ID register stores a unique 8-bit value that identifies the UCS device family.

REGISTER 9-19: PRODUCT ID REGISTER (ADDRESS FDH)

R-1	R-1	R-1	R-0	R-0	R-0	R-0	R-1
PID<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **PID<7:0>:** Product ID for the UCS2112.

9.10 Manufacturer ID Register

The Manufacturer ID register stores a unique 8-bit value that identifies Microchip Technology Inc.

REGISTER 9-20: MANUFACTURER ID REGISTER (ADDRESS FEH)

R-0	R-1	R-0	R-1	R-1	R-1	R-0	R-1
MID<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **MID<7:0>:** Manufacturer ID for Microchip.

9.11 Revision Register

The Revision register stores an 8-bit value that represents the part revision.

REGISTER 9-21: REVISION REGISTER (ADDRESS FFH)

R-1	R-0	R-0	R-0	R-0	R-0	R-0	R-1
REV<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

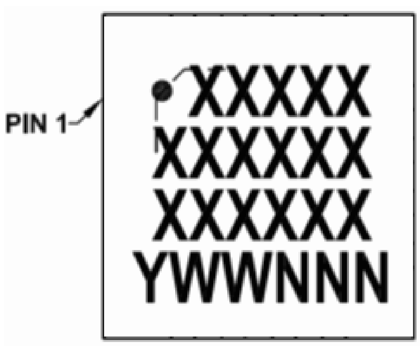
bit 7-0 **REV<7:0>:** Part Revision.

NOTES:

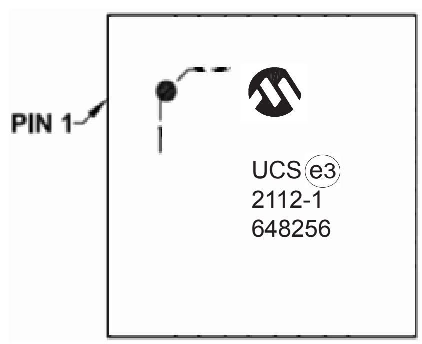
10.0 PACKAGING INFORMATION

10.1 Package Marking Information

4x4 mm QFN, 20-lead

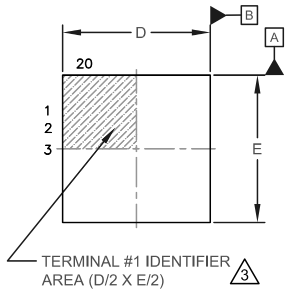


Example

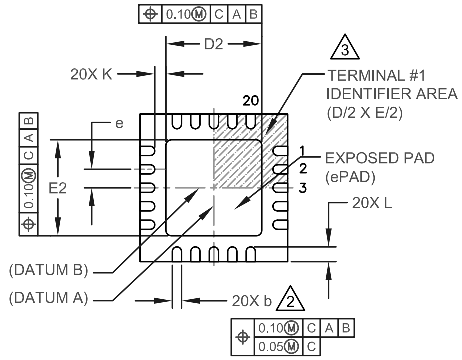


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

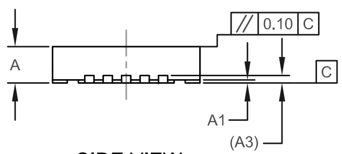


TOP VIEW

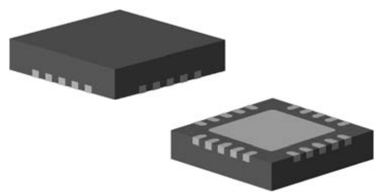


BOTTOM VIEW

REVISION HISTORY			
REVISION	DESCRIPTION	DATE	RELEASED BY
A	INITIAL PRELIMINARY RELEASE	3/18/07	S.K.ILIEV
B	INITIAL PRODUCTION RELEASE	12/5/07	S.K.ILIEV
C	L from 0.4±0.05 to 0.4±0.1mm. Y from 0.65 to 0.69mm. GD/GE from 3.01 to 3.00. K(min) from 0.2 to 0.25	4/21/08	S.K.ILIEV
D	ADDED GD/GE MAX. Y=0.69 from NOM to MIN	3/8/10	S.K.ILIEV
E	ADDED Y (MAX) = 0.80	3/15/10	S.K.ILIEV
F	ADDED Y CENTER PCB PAD VIA INFORMATION	2/17/12	S.K.ILIEV



SIDE VIEW

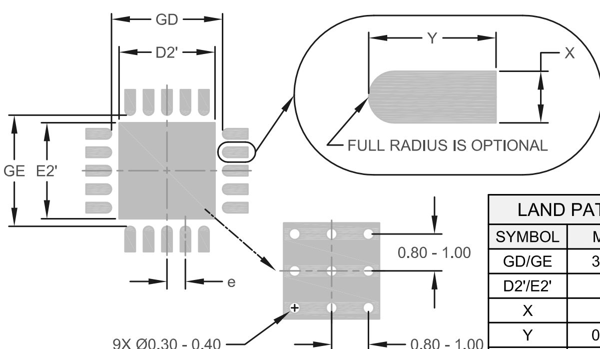


3-D VIEWS

COMMON DIMENSIONS					
SYMBOL	MIN	NOM	MAX	NOTE	REMARK
A	0.80	0.85	0.90	-	OVERALL PACKAGE HEIGHT
A1	0	0.02	0.05	-	STANDOFF
A3	0.20 REF			-	LEAD-FRAME THICKNESS
D/E	3.90	4.00	4.10	-	X/Y BODY SIZE
D2/E2	2.50	2.60	2.70	-	X/Y EXPOSED PAD SIZE
L	0.30	0.40	0.50	-	TERMINAL LENGTH
b	0.18	0.25	0.30	2	TERMINAL WIDTH
K	0.25	0.30	-	-	TERMINAL TO PAD DISTANCE
e	0.50 BSC			-	TERMINAL PITCH

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS "b" APPLIES TO PLATED TERMINALS AND IT IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
3. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE AREA INDICATED.



LAND PATTERN DIMENSIONS			
SYMBOL	MIN	NOM	MAX
GD/GE	3.00	-	3.10
D2'/E2'	-	2.60	2.60
X	-	0.28	0.28
Y	0.69	-	0.80
e	0.50		

THE USER MAY MODIFY THE PCB LAND PATTERN DIMENSIONS BASED ON THEIR EXPERIENCE AND/OR PROCESS CAPABILITY

PCB LAND PATTERN

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLIMETERS AND TOLERANCES ARE:
DECIMAL X.X ±0.1 X.XX ±0.05 X.XXX ±0.025 — ANGULAR ±1°
INTERPRET DIM AND TOL PER ASME Y14.5M - 1994

THIRD ANGLE PROJECTION

Note: For the most current package drawings, see the Microchip Packaging Specification at http://www.microchip.com/packaging

	NAME	DATE
DRAWN	-	3/14/07
CHECKED	S.K.ILIEV	3/15/07
APPROVED	S.K.ILIEV	3/18/07

MATERIAL: -
FINISH: -
PRINT WITH "SCALE TO FIT" DO NOT SCALE DRAWING

TITLE: PACKAGE OUTLINE
20 PINS SQFN, 4x4mm BODY, 0.5mm PITCH
(SAWN QFN, FULL LEAD TERMINATION)

DWG NUMBER	REV
20SQFN-4x4B-0.5P	F

SCALE	STD COMPLIANCE	SHEET
1:1	JEDEC: MO-220	1 OF 1

NOTES:

APPENDIX A: REVISION HISTORY

Revision C (February 2017)

The following is the list of modifications:

- Added minimum and maximum values for the ILIM7 parameter in Table 1-2: Electrical Specifications.
- Added “Operating Junction Temperature” parameter in Table 1-3: Temperature Specifications.
- Added a note in Section 8.13, SMBus Send Byte detailing the behavior of the UCS2112 when two commands are sent in a row.
- Added maximum value for the VDD_TH_HYST parameter and maximum value for the R_{ON_PSW} parameter in Table 1-2 Electrical Specifications.
- Updated Figure 2-8 “Detect State VBUS vs. IBUS”.
- Minor typographical corrections

Revision B (October 2015)

- Updated Features to indicate EN/IEC 60950-1 (CB) certification.

Revision A (August 2015)

- Original release of this document

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X] (1)	–X	–X	/XX
Device	Tape and Reel Option	Version	Temperature Range	Package

Device:	UCS2112: USB Dual-Port Power Switch and Current Monitor
Tape and Reel Option:	Blank = Tube T = Tape and Reel
Version:	1 = SMBus address 57h
Temperature Range:	V = -40°C to +105°C (Various)
Package:	G4 = Plastic Quad Flat No Lead Package - 4x4 mm Body with 0.40 mm Contact Length, Saw Singulated, QFN, 20-lead

Examples:

a) UCS2112-1-V/G4: Various Temperature
20-pin 4x4 QFN package

b) UCS2112T-1-V/G4: Tape and Reel
Various Temperature
20-pin 4x4 QFN Package

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip’s Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

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QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
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ISBN: 978-1-5224-1382-0

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11/07/16