

---

---

## Full-Featured, Low Pin Count Microcontrollers with XLP Product Brief

---

---

### Description

PIC16(L)F183XX microcontrollers feature Analog, Core Independent Peripherals and communication peripherals, combined with eXtreme Low Power (XLP) for a wide range of general purpose and low-power applications. The Peripheral Pin Select (PPS) functionality enables pin mapping when using the digital peripherals (CLC, CWG, CCP, PWM and communications) to add flexibility to the application design.

### Core Features

- C Compiler Optimized RISC Architecture
- Only 49 Instructions
- Operating Speed:
  - DC – 32 MHz clock input
  - 125 ns minimum instruction cycle
- Interrupt Capability
- 16-Level Deep Hardware Stack
- Up to Four 8-Bit Timers
- Up to Three 16-Bit Timers
- Low-Current Power-on Reset (POR)
- Configurable Power-up Timer (PWRTE)
- Brown-out Reset (BOR) with Fast Recovery
- Low-Power BOR (LPBOR) Option
- Extended Watchdog Timer (WDT) with Dedicated On-Chip Oscillator for Reliable Operation
- Programmable Code Protection

### Memory

- Up to 14KB Program Flash Memory (PFM)
- Up to 1KB Data SRAM Memory
- 256B of EEPROM Data Flash Memory (DFM)
- Direct, Indirect and Relative Addressing modes

### Operating Characteristics

- Operating Voltage Range:
  - 1.8V to 3.6V (PIC16LF183XX)
  - 2.3V to 5.5V (PIC16F183XX)
- Temperature Range:
  - Industrial: -40°C to 85°C
  - Extended: -40°C to 125°C

### eXtreme Low-Power (XLP) Features

- Sleep mode: 50 nA @ 1.8V, typical
- Watchdog Timer: 500 nA @ 1.8V, typical
- Secondary Oscillator: 500 nA @ 32 kHz
- Operating Current:
  - 8 uA @ 32 kHz, 1.8V, typical
  - 32 uA/MHz @ 1.8V, typical

### Power-Saving Functionality

- Doze mode: Ability to run the CPU core slower than the system clock used by the internal peripherals
- Idle mode: Ability to put the CPU core to sleep while internal peripherals continue operating from the system clock
- Sleep mode: Lowest Power Consumption
- Peripheral Module Disable: Peripheral power disable hardware module to minimize power consumption of unused peripherals

### Digital Peripherals

- Configurable Logic Cell (CLC):
  - Up to four CLCs
  - Integrated combinational and sequential logic
- Complementary Waveform Generator (CWG):
  - Rising and falling edge dead-band control
  - Full-bridge, half-bridge, 1-channel drive
  - Up to two CWGs
  - Multiple signal sources
- Up to Four Capture/Compare/PWM (CCP) modules
- PWM: Two 10-bit Pulse-Width Modulators
- Numerically Controlled Oscillator (NCO):
  - Precision linear frequency generator (@50% duty cycle) with 0.0001% step size of source input clock
  - Input Clock: 0 Hz < F<sub>NCO</sub> < 32 MHz
  - Resolution: F<sub>NCO</sub>/2<sup>20</sup>
- Serial Communications:
  - SPI, I<sup>2</sup>C™, EUSART
  - RS-232, RS-485, LIN compatible
- Data Signal Modulator (DSM):
  - Modulates a carrier signal with digital data to create custom carrier synchronized output waveforms.

# PIC16(L)F183XX

---

- Peripheral Pin Select (PPS):
  - I/O pin remapping of digital peripherals
- Up to 18 I/O Pins:
  - Individually programmable pull-ups
  - Slew rate control
  - Interrupt-on-change with edge-select

## Analog Peripherals

- 10-Bit Analog-to-Digital Converter (ADC):
  - Up to 17 external channels
  - Conversion available during Sleep
- Comparator:
  - Up to two comparators
  - Low and High-Speed modes
  - Fixed Voltage Reference at inverting/non-inverting input(s)
  - Comparator outputs externally accessible
- 5-Bit Digital-to-Analog Converter (DAC):
  - 5-bit resolution, rail-to-rail
  - Positive Reference Selection
  - Unbuffered I/O pin output
  - Internal connections to ADCs and comparators
- Voltage Reference:
  - Fixed Voltage Reference with 1.024V, 2.048V and 4.096V output levels

## Clocking Structure

- High-Precision Internal Oscillator:
  - Selectable frequency range up to 32 MHz
- x2/x4 PLL with Internal and External Sources
- Low-Power Internal 32 kHz Oscillator (LFINTOSC)
- External 32 kHz Crystal Oscillator (SOCS)
- External High-Speed Crystal Oscillators

**TABLE 1: PIC16(L)F183XX Family Types**

Device	Data Sheet Index	Program Flash Memory (K words)	Program Memory Flash (K bytes)	Data Memory (bytes)	Data SRAM (bytes)	I/Os <sup>(1)</sup>	10-bit ADC (ch)	5-bit DAC	Comparators	CWG	Clock Ref	Timers (8/16-bit)	CCP	PWM	NCO	EUSART	MSSP (I <sup>2</sup> C™/SPI)	CLC	DSM	PPS	XLP	PMD	Idle & Doze	Debug <sup>(2)</sup>
PIC16(L)F18313	(A)	2	3.5	256	256	6	9	1	1	1	1	2/1	2	2	1	1	1	2	1	Y	Y	Y	Y	I/E
PIC16(L)F18323	(A)	2	3.5	256	256	12	15	1	2	1	1	2/1	2	2	1	1	1	2	1	Y	Y	Y	Y	I/E
PIC16(L)F18324	(B)	4	7	256	512	12	15	1	2	2	1	4/3	4	2	1	1	1	4	1	Y	Y	Y	Y	I/E
PIC16(L)F18325	(C)	8	14	256	1K	12	15	1	2	2	1	4/3	4	2	1	1	2	4	1	Y	Y	Y	Y	I/E
PIC16(L)F18344	(B)	4	7	256	512	18	21	1	2	2	1	4/3	4	2	1	1	1	4	1	Y	Y	Y	Y	I/E
PIC16(L)F18345	(C)	8	14	256	1K	18	21	1	2	2	1	4/3	4	2	1	1	2	4	1	Y	Y	Y	Y	I/E

**Note 1:** One pin is input-only.

**Note 2:** Debugging Methods: (I) – Integrated on Chip; E – using Emulation Header.

**Data Sheet Index:** (Unshaded devices are described in this document.)

**Note A:** Future Release [PIC16\(L\)F18313/18323 Data Sheet](#), [Full-Featured, Low Pin Count Microcontrollers with XLP](#)  
**Note B:** Future Release [PIC16\(L\)F18324/18344 Data Sheet](#), [Full-Featured, Low Pin Count Microcontrollers with XLP](#)  
**Note C:** Future Release [PIC16\(L\)F18325/18345 Data Sheet](#), [Full-Featured, Low Pin Count Microcontrollers with XLP](#)

**Note:** For other small form-factor package availability and marking information, please visit <http://www.microchip.com/packaging> or contact your local sales office.

# PIC16(L)F183XX

---

---

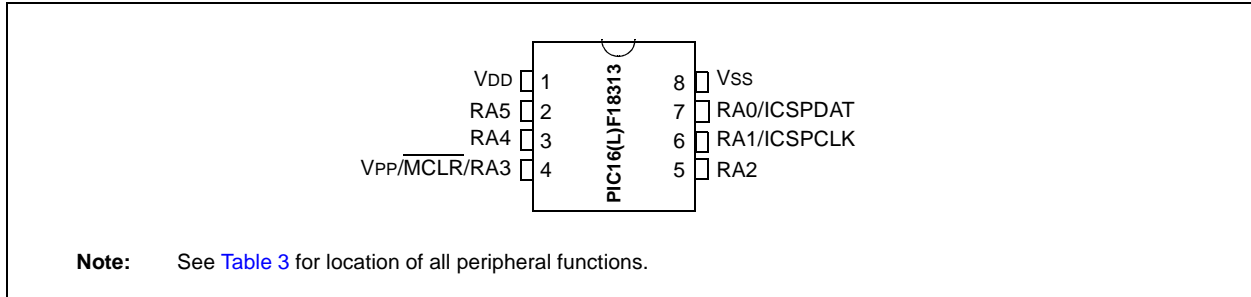
**TABLE 2: PACKAGES**

Packages	PDIP	SOIC	DFN/UDFN	TSSOP	QFN/UQFN	SSOP
PIC16(L)F18313	X	X	X			
PIC16(L)F18323	X	X		X	X	
PIC16(L)F18324	X	X		X	X	
PIC16(L)F18325	X	X		X	X	
PIC16(L)F18344	X	X			X	X
PIC16(L)F18345	X	X			X	X

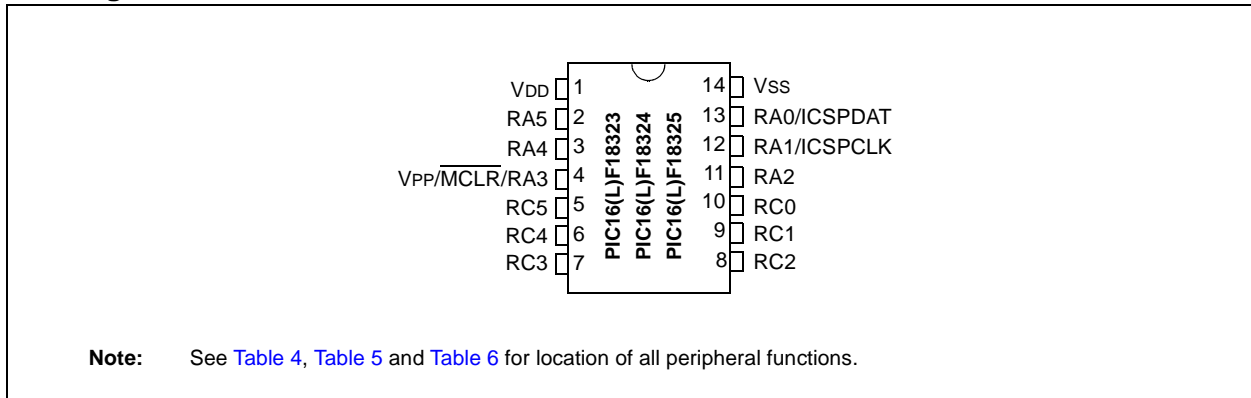
**Note:** Pin details are subject to change.

## PIN DIAGRAMS

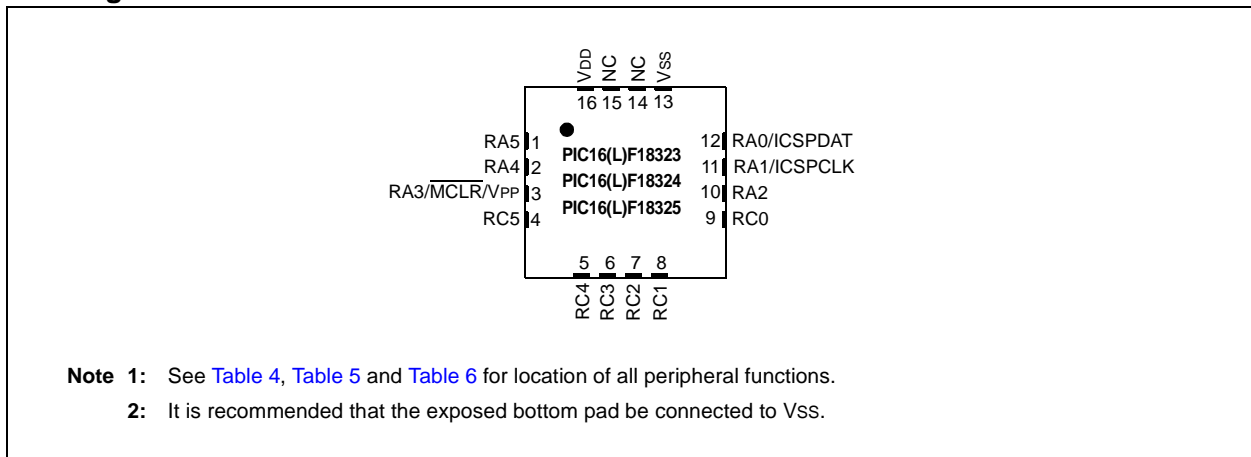
### Pin Diagram – 8-Pin PDIP, SOIC, DFN/UDFN



### Pin Diagram – 14-Pin PDIP, SOIC, TSSOP

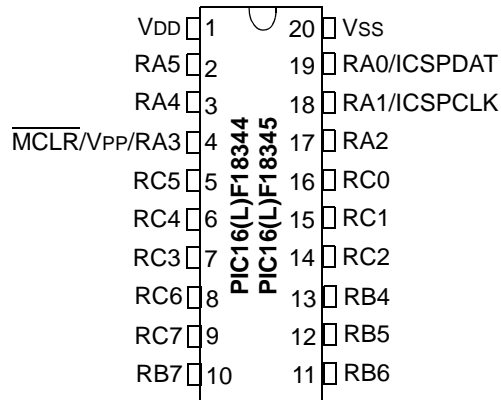


### Pin Diagram – 16-Pin QFN/UQFN



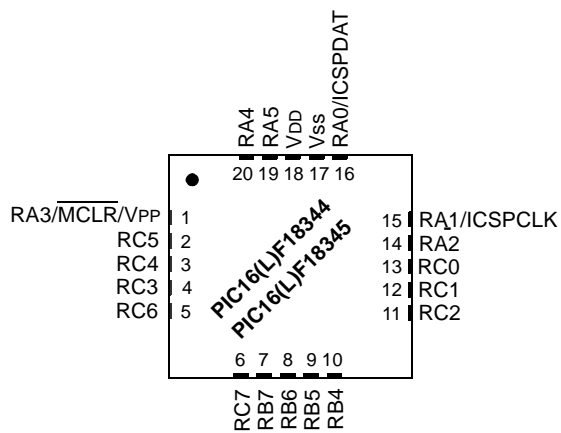
# PIC16(L)F183XX

## Pin Diagram – 20-Pin PDIP, SOIC, SSOP



**Note:** See [Table 7](#) and [Table 8](#) for location of all peripheral functions.

## Pin Diagram – 20-Pin QFN/UQFN (4x4)



- Note 1:** See [Table 7](#) and [Table 8](#) for location of all peripheral functions.
- 2:** It is recommended that the exposed bottom pad be connected to VSS.

## PIN ALLOCATION TABLES

TABLE 3: 8-PIN ALLOCATION TABLE (PIC16(L)F18313)

I/O <sup>(2)</sup>	8-Pin PDIP/SOIC/DFN/UDFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	EUSART	CLC	CLKR	Interrupt	Pull-up	Basic
RA0	7	ANA0	—	C1IN0+	—	DAC1OUT	MDCIN1 <sup>(1)</sup>	—	—	—	—	—	TX <sup>(1)</sup> CK <sup>(1)</sup>	CLCIN3 <sup>(1)</sup>	—	IOCA0	Y	ICDDAT/ ICSPDAT
RA1	6	ANA1	VREF+	C1IN0-	—	DAC1REF+	MDMIN <sup>(1)</sup>	—	—	—	—	SCK <sup>(1)</sup> SCL <sup>(1,3,4)</sup>	RX <sup>(1)</sup> DT <sup>(1,3)</sup>	CLCIN2 <sup>(1)</sup>	—	IOCA1	Y	ICDCLK/ ICSPCLK
RA2	5	ANA2	VREF-	—	—	DAC1REF-	—	T0CKI <sup>(1)</sup>	—	—	CWG1 <sup>(1)</sup>	SDA <sup>(1,3,4)</sup> SDO <sup>(1)</sup>	—	—	—	INT <sup>(1)</sup> IOCA2	Y	—
RA3	4	—	—	—	—	—	—	—	—	—	—	SS <sup>(1)</sup>	—	CLCIN0 <sup>(1)</sup>	—	IOCA3	Y	MCLR VPP
RA4	3	ANA4	—	C1IN1-	—	—	—	T1G <sup>(1)</sup> SOSCO	—	—	—	—	—	—	—	IOCA4	Y	CLKOUT OSC2
RA5	2	ANA5	—	—	—	—	MDCIN2 <sup>(1)</sup>	T1CKI <sup>(1)</sup> SOSCIN SOSCI	CCP1 <sup>(1)</sup> CCP2 <sup>(1)</sup>	—	—	—	—	CLCIN1 <sup>(1)</sup>	—	IOCA5	Y	CLKIN OSC1
VDD	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD
VSS	8	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS
OUT <sup>(2)</sup>	—	—	—	C1OUT	NCO	—	DSM	TMR0	CCP1	PWM5	CWG1A	SDA <sup>(3)</sup>	CK	CLC1OUT	CLKR	—	—	—
	—	—	—	—	—	—	—	—	CCP2	PWM6	CWG1B	SCL <sup>(3)</sup>	DT <sup>(3)</sup>	CLC2OUT	—	—	—	—
	—	—	—	—	—	—	—	—	—	—	CWG1C	SDO	TX	—	—	—	—	—
	—	—	—	—	—	—	—	—	—	—	CWG1D	SCK	—	—	—	—	—	—

- Note**
- 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.
  - 2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.
  - 3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.
  - 4: These pins are configured for I<sup>2</sup>C™ logic levels; clock and data signals may be assigned to any of these pins. Assignments to the other pins (e.g., RA5) will operate, but logic levels will be standard TTL/ST as selected by the INLVL register.

**TABLE 4: 14/16-PIN ALLOCATION TABLE (PIC16(L)F18323)**

I/O <sup>(2)</sup>	14/16-Pin PDIP/SOIC/TSSOP	16-Pin QFN/JUQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	EUSART	CLC	CLKR	Interrupt	Pull-up	Basic
RA0	13	12	ANA0	—	C1IN0+	—	DAC1OUT	—	—	—	—	—	—	—	—	—	IOCA0	Y	ICDDAT/ ICSPDAT
RA1	12	11	ANA1	VREF+	C1IN0- C2IN0-	—	DAC1REF+	—	—	—	—	—	—	—	—	—	IOCA1	Y	ICDCLK/ ICSPCLK
RA2	11	10	ANA2	VREF-	—	—	DAC1REF-	—	TOCKI <sup>(1)</sup>	—	—	CWG1 <sup>(1)</sup>	—	—	—	—	INT <sup>(1)</sup> IOCA2	Y	—
RA3	4	3	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCA3	Y	MCLR VPP
RA4	3	2	ANA4	—	—	—	—	—	T1G <sup>(1)</sup> SOSCO	—	—	—	—	—	—	—	IOCA4	Y	CLKOUT OSC2
RA5	2	1	ANA5	—	—	—	—	—	T1CKI <sup>(1)</sup> SOSCIN SOSCI	—	—	—	—	—	CLCIN3 <sup>(1)</sup>	—	IOCA5	Y	CLKIN OSC1
RC0	10	9	ANC0	—	C2IN0+	—	—	—	—	—	—	—	SCK <sup>(1)</sup> SCL <sup>(1,3,4)</sup>	—	—	—	IOCC0	Y	—
RC1	9	8	ANC1	—	C1IN1- C2IN1-	—	—	—	—	—	—	—	SDI <sup>(1)</sup> SDA <sup>(1,3,4)</sup>	—	CLCIN2 <sup>(1)</sup>	—	IOCC1	Y	—
RC2	8	7	ANC2	—	C1IN2- C2IN2-	—	—	MDCIN1 <sup>(1)</sup>	—	—	—	—	—	—	—	—	IOCC2	Y	—
RC3	7	6	ANC3	—	C1IN3- C2IN3-	—	—	MDMIN <sup>(1)</sup>	—	CCP2 <sup>(1)</sup>	—	—	SS <sup>(1)</sup>	—	CLCIN0 <sup>(1)</sup>	—	IOCC3	Y	—
RC4	6	5	ANC4	—	—	—	—	—	—	—	—	—	—	TX <sup>(1)</sup> CK <sup>(1)</sup>	CLCIN1 <sup>(1)</sup>	—	IOCC4	Y	—
RC5	5	4	ANC5	—	—	—	—	MDCIN2 <sup>(1)</sup>	—	CCP1 <sup>(1)</sup>	—	—	—	RX <sup>(1)</sup> DT <sup>(1,3)</sup>	—	—	IOCC5	Y	—
VDD	1	16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD
VSS	14	13	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS

- Note**
- 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.
  - 2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.
  - 3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.
  - 4: These pins are configured for I<sup>2</sup>C™ logic levels; clock and data signals may be assigned to any of these pins. Assignments to other pins (e.g. RA5) will operate, but logic levels will be standard TTL/ST as selected by the INLVL register.



**TABLE 4: 14/16-PIN ALLOCATION TABLE (PIC16(L)F18323)**

I/O <sup>(2)</sup>	14/16-Pin PDIP/SOIC/TSSOP	16-Pin QFN/UQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	EUSART	CLC	CLKR	Interrupt	Pull-up	Basic
OUT <sup>(2)</sup>	—	—	—	—	C1OUT	NCO	—	DSM	TMR0	CCP1	PWM5	CWG1A	SDA <sup>(3)</sup>	CK	CLC1OUT	CLKR	—	—	—
	—	—	—	—	C2OUT	—	—	—	—	CCP2	PWM6	CWG1B	SCL <sup>(3)</sup>	DT <sup>(3)</sup>	CLC2OUT	—	—	—	—
	—	—	—	—	—	—	—	—	—	—	—	CWG1C	SDO	TX	—	—	—	—	—
	—	—	—	—	—	—	—	—	—	—	—	CWG1D	SCK	—	—	—	—	—	—

- Note**
- 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.
  - 2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.
  - 3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.
  - 4: These pins are configured for I<sup>2</sup>C™ logic levels; clock and data signals may be assigned to any of these pins. Assignments to other pins (e.g. RA5) will operate, but logic levels will be standard TTL/ST as selected by the INLVL register.

TABLE 5: 14/16-PIN ALLOCATION TABLE (PIC16(L)F18324)

I/O <sup>(2)</sup>	14/16-Pin PDIP/SOIC/TSSOP	16-Pin QFN/UFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	EUSART	CLC	CLKR	Interrupt	Pull-up	Basic	
RA0	13	12	ANA0	—	C1IN0+	—	DAC1OUT	—	—	—	—	—	—	—	—	—	IOCA0	Y	ICDDAT/ ICSPDAT	
RA1	12	11	ANA1	VREF+	C1IN0- C2IN0-	—	DAC1REF+	—	—	—	—	—	—	—	—	—	IOCA1	Y	ICDCLK/ ICSPCLK	
RA2	11	10	ANA2	VREF-	—	—	DAC1REF-	—	T0CKI <sup>(1)</sup>	CCP3 <sup>(1)</sup>	—	CWG1 <sup>(1)</sup> CWG2 <sup>(1)</sup>	—	—	—	—	INT <sup>(1)</sup> IOCA2	Y	—	
RA3	4	3	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCA3	Y	MCLR V <sub>PP</sub>	
RA4	3	2	ANA4	—	—	—	—	—	T1G <sup>(1)</sup> SOSCO	—	—	—	—	—	—	—	IOCA4	Y	CLKOUT OSC2	
RA5	2	1	ANA5	—	—	—	—	—	T1CKI <sup>(1)</sup> SOSCIN SOSCI	—	—	—	—	—	CLCIN3 <sup>(1)</sup>	—	IOCA5	Y	CLKIN OSC1	
RC0	10	9	ANC0	—	C2IN0+	—	—	—	T5CKI <sup>(1)</sup>	—	—	—	SCK <sup>(1)</sup> SCL <sup>(1,3,4)</sup>	—	—	—	IOCC0	Y	—	
RC1	9	8	ANC1	—	C1IN1- C2IN1-	—	—	—	—	CCP4 <sup>(1)</sup>	—	—	SDI <sup>(1)</sup> SDA <sup>(1,3,4)</sup>	—	CLCIN2 <sup>(1)</sup>	—	IOCC1	Y	—	
RC2	8	7	ANC2	—	C1IN2- C2IN2-	—	—	MDCIN1 <sup>(1)</sup>	—	—	—	—	—	—	—	—	IOCC2	Y	—	
RC3	7	6	ANC3	—	C1IN3- C2IN3-	—	—	MDMIN <sup>(1)</sup>	T5G <sup>(1)</sup>	CCP2 <sup>(1)</sup>	—	—	SS <sup>(1)</sup>	—	CLCIN0 <sup>(1)</sup>	—	IOCC3	Y	—	
RC4	6	5	ANC4	—	—	—	—	—	T3G <sup>(1)</sup>	—	—	—	—	TX <sup>(1)</sup> CK <sup>(1)</sup>	CLCIN1 <sup>(1)</sup>	—	IOCC4	Y	—	
RC5	5	4	ANC5	—	—	—	—	MDCIN2 <sup>(1)</sup>	T3CKI <sup>(1)</sup>	CCP1 <sup>(1)</sup>	—	—	—	RX <sup>(1)</sup> DT <sup>(1,3)</sup>	—	—	IOCC5	Y	—	
V <sub>DD</sub>	1	16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	V <sub>DD</sub>	
V <sub>SS</sub>	14	13	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	V <sub>SS</sub>

- Note**
- 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.
  - 2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.
  - 3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.
  - 4: These pins are configured for I<sup>2</sup>C™ logic levels; clock and data signals may be assigned to any of these pins. Assignments to other pins (e.g. RA5) will operate, but logic levels will be standard TTL/ST as selected by the INLVL register.

**TABLE 5: 14/16-PIN ALLOCATION TABLE (PIC16(L)F18324) (CONTINUED)**

I/O <sup>(2)</sup>	14/16-Pin PDIP/SOIC/TSSOP	16-Pin QFN/UQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	EUSART	CLC	CLKR	Interrupt	Pull-up	Basic
OUT <sup>(2)</sup>	—	—	—	—	C1OUT	NCO	—	DSM	TMR0	CCP1	PWM5	CWG1A CWG2A	SDA <sup>(3)</sup>	CK	CLC1OUT	CLKR	—	—	—
	—	—	—	—	C2OUT	—	—	—	—	CCP2	PWM6	CWG1B CWG2B	SCL <sup>(3)</sup>	DT <sup>(3)</sup>	CLC2OUT	—	—	—	—
	—	—	—	—	—	—	—	—	—	CCP3	—	CWG1C CWG2C	SDO	TX	CLC3OUT	—	—	—	—
	—	—	—	—	—	—	—	—	—	CCP4	—	CWG1D CWG2D	SCK	—	CLC4OUT	—	—	—	—

- Note**
- 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.
  - 2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.
  - 3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.
  - 4: These pins are configured for I<sup>2</sup>C™ logic levels; clock and data signals may be assigned to any of these pins. Assignments to other pins (e.g. RA5) will operate, but logic levels will be standard TTL/ST as selected by the INLVL register.

TABLE 6: 14/16-PIN ALLOCATION TABLE (PIC16(L)F18325)

(2) I/O	14/16-Pin PDIP/SOIC/TSSOP	16-Pin QFN/QFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	EUSART	CLC	CLKR	Interrupt	Pull-up	Basic	
RA0	13	12	ANA0	—	C1IN0+	—	DAC1OUT	—	—	—	—	—	SS2 <sup>(1)</sup>	—	—	—	IOCA0	Y	ICDDAT/ ICSPDAT	
RA1	12	11	ANA1	VREF+	C1IN0- C2IN0-	—	DAC1REF+	—	—	—	—	—	—	—	—	—	IOCA1	Y	ICDCLK/ ICSPCLK	
RA2	11	10	ANA2	VREF-	—	—	DAC1REF-	—	T0CKI <sup>(1)</sup>	CCP3 <sup>(1)</sup>	—	CWG1 <sup>(1)</sup> CWG2 <sup>(1)</sup>	—	—	—	—	INT <sup>(1)</sup> IOCA2	Y	—	
RA3	4	3	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCA3	Y	MCLR VPP	
RA4	3	2	ANA4	—	—	—	—	—	T1G <sup>(1)</sup> SOSCO	—	—	—	—	—	—	—	IOCA4	Y	CLKOUT OSC2	
RA5	2	1	ANA5	—	—	—	—	—	T1CKI <sup>(1)</sup> SOSCIN SOSCI	—	—	—	—	—	CLCIN3 <sup>(1)</sup>	—	IOCA5	Y	CLKIN OSC1	
RC0	10	9	ANC0	—	C2IN0+	—	—	—	T5CKI <sup>(1)</sup>	—	—	—	SCK1 <sup>(1)</sup> SCL1 <sup>(1,3,4)</sup>	—	—	—	IOCC0	Y	—	
RC1	9	8	ANC1	—	C1IN1- C2IN1-	—	—	—	—	CCP4 <sup>(1)</sup>	—	—	SDI1 <sup>(1)</sup> SDA1 <sup>(1,3,4)</sup>	—	CLCIN2 <sup>(1)</sup>	—	IOCC1	Y	—	
RC2	8	7	ANC2	—	C1IN2- C2IN2-	—	—	MDCIN1 <sup>(1)</sup>	—	—	—	—	—	—	—	—	IOCC2	Y	—	
RC3	7	6	ANC3	—	C1IN3- C2IN3-	—	—	MDMIN <sup>(1)</sup>	T5G <sup>(1)</sup>	CCP2 <sup>(1)</sup>	—	—	SS1 <sup>(1)</sup>	—	CLCIN0 <sup>(1)</sup>	—	IOCC3	Y	—	
RC4	6	5	ANC4	—	—	—	—	—	T3G <sup>(1)</sup>	—	—	—	SCK2 <sup>(1)</sup> SCL2 <sup>(1,3,4)</sup>	TX <sup>(1)</sup> CK <sup>(1)</sup>	CLCIN1 <sup>(1)</sup>	—	IOCC4	Y	—	
RC5	5	4	ANC5	—	—	—	—	MDCIN2 <sup>(1)</sup>	T3CKI <sup>(1)</sup>	CCP1 <sup>(1)</sup>	—	—	SDI2 <sup>(1)</sup> SDA2 <sup>(1,3,4)</sup>	RX <sup>(1)</sup> DT <sup>(1,3)</sup>	—	—	IOCC5	Y	—	
VDD	1	16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD	
VSS	14	13	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS

- Note**
- 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.
  - 2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.
  - 3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.
  - 4: These pins are configured for I<sup>2</sup>C™ logic levels; clock and data signals may be assigned to any of these pins. Assignments to other pins (e.g. RA5) will operate, but logic levels will be standard TTL/ST as selected by the INLVL register.

**TABLE 6: 14/16-PIN ALLOCATION TABLE (PIC16(L)F18325) (Continued)**

I/O <sup>(2)</sup>	14/16-Pin PDIP/SOIC/TSSOP	16-Pin QFN/UQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	EUSART	CLC	CLKR	Interrupt	Pull-up	Basic
OUT <sup>(2)</sup>	—	—	—	—	C1OUT	DDS	—	DSM	TMR0	CCP1	PWM5	CWG1A CWG2A	SDA1 <sup>(3)</sup> SDA2 <sup>(3)</sup>	CK	CLC1OUT	CLKR	—	—	—
	—	—	—	—	C2OUT	—	—	—	—	CCP2	PWM6	CWG1B CWG2B	SCL1 <sup>(3)</sup> SCL2 <sup>(3)</sup>	DT <sup>(3)</sup>	CLC2OUT	—	—	—	—
	—	—	—	—	—	—	—	—	—	CCP3	—	CWG1C CWG2C	SDO1 SDO2	TX	CLC3OUT	—	—	—	—
	—	—	—	—	—	—	—	—	—	CCP4	—	CWG1D CWG2D	SCK1 SCK2	—	CLC4OUT	—	—	—	—

- Note**
- 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.
  - 2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.
  - 3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.
  - 4: These pins are configured for I<sup>2</sup>C™ logic levels; clock and data signals may be assigned to any of these pins. Assignments to other pins (e.g. RA5) will operate, but logic levels will be standard TTL/ST as selected by the INLVL register.

TABLE 7: 20-PIN ALLOCATION TABLE (PIC16(L)F18344)

I/O/I	20-Pin PDIP/SOIC/SSOP	20-Pin QFN/UQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	EUSART	CLC	CLKR	Interrupt	Pull-up	Basic
RA0	19	16	ANA0	—	C1IN0+	—	DAC1OUT	—	—	—	—	—	—	—	—	—	IOCA0	Y	ICDDAT/ ICSPDAT
RA1	18	15	ANA1	VREF+	C1IN0- C2IN0-	—	DAC1REF+	—	—	—	—	—	—	—	—	—	IOCA1	Y	ICDCLK/ ICSPCLK
RA2	17	14	ANA2	VREF-	—	—	DAC1REF-	—	T0CKI <sup>(1)</sup>	CCP3 <sup>(1)</sup>	—	CWG1 <sup>(1)</sup> CWG2 <sup>(1)</sup>	—	—	CLCIN0 <sup>(1)</sup>	—	INT <sup>(1)</sup> IOCA2	Y	—
RA3	4	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCA3	Y	MCLR VPP
RA4	3	20	ANA4	—	—	—	—	—	T1G <sup>(1)</sup> T3G <sup>(1)</sup> T5G <sup>(1)</sup> SOSCO	CCP4 <sup>(1)</sup>	—	—	—	—	—	—	IOCA4	Y	CLKOUT OSC2
RA5	2	19	ANA5	—	—	—	—	—	T1CKI <sup>(1)</sup> T3CKI <sup>(1)</sup> T5CKI <sup>(1)</sup> SOSCIN SOSCI	—	—	—	—	—	—	—	IOCA5	Y	CLKIN OSC1
RB4	13	10	ANB4	—	—	—	—	—	—	—	—	—	SDI <sup>(1)</sup> SDA <sup>(1,3,4)</sup>	—	CLCIN2 <sup>(1)</sup>	—	IOCB4	Y	—
RB5	12	9	ANB5	—	—	—	—	—	—	—	—	—	—	RX <sup>(1)</sup> DT <sup>(1)</sup>	CLCIN3 <sup>(1)</sup>	—	IOCB5	Y	—
RB6	11	8	ANB6	—	—	—	—	—	—	—	—	—	SCK <sup>(1)</sup> SCL <sup>(1,3,4)</sup>	—	—	—	IOCB6	Y	—
RB7	10	7	ANB7	—	—	—	—	—	—	—	—	—	—	TX <sup>(1)</sup> CK <sup>(1)</sup>	—	—	IOCB7	Y	—
RC0	16	13	ANC0	—	C2IN0+	—	—	—	—	—	—	—	—	—	—	—	IOCC0	Y	—
RC1	15	12	ANC1	—	C1IN1- C2IN1-	—	—	—	—	—	—	—	—	—	—	—	IOCC1	Y	—
RC2	14	11	ANC2	—	C1IN2- C2IN2-	—	—	MDCIN1 <sup>(1)</sup>	—	—	—	—	—	—	—	—	IOCC2	Y	—

- Note**
- 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.
  - 2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.
  - 3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.
  - 4: These pins are configured for I<sup>2</sup>C™ logic levels; clock and data signals may be assigned to any of these pins. Assignments to other pins (e.g., RA5) will operate, but logic levels will be standard TTL/ST as selected by the INLVL register.

**TABLE 7: 20-PIN ALLOCATION TABLE (PIC16(L)F18344) (Continued)**

I/O <sup>(2)</sup>	20-Pin PDIP/SSOP	20-Pin QFN/UQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	EUSART	CLC	CLKR	Interrupt	Pull-up	Basic
RC3	7	4	ANC3	—	C1IN3- C2IN3-	—	—	MDMIN <sup>(1)</sup>	—	CCP2 <sup>(1)</sup>	—	—	—	—	CLCIN1 <sup>(1)</sup>	—	IOCC3	Y	—
RC4	6	3	ANC4	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCC4	Y	—
RC5	5	2	ANC5	—	—	—	—	MDCIN2 <sup>(1)</sup>	—	CCP1 <sup>(1)</sup>	—	—	—	—	—	—	IOCC5	Y	—
RC6	8	5	ANC6	—	—	—	—	—	—	—	—	—	SS <sup>(1)</sup>	—	—	—	IOCC6	Y	—
RC7	9	6	ANC7	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCC7	Y	—
VDD	1	18	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD
VSS	20	17	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS
OUT <sup>(2)</sup>	—	—	—	—	C1OUT	NCO	—	DSM	TMR0	CCP1	PWM5	CWG1A CWG2A	SDO	DT <sup>(3)</sup>	CLC1OUT	CLKR	—	—	—
	—	—	—	—	C2OUT	—	—	—	—	CCP2	PWM6	CWG1B CWG2B	SCK	CK	CLC2OUT	—	—	—	—
	—	—	—	—	—	—	—	—	—	CCP3	—	CWG1C CWG2C	SCL <sup>(3)</sup>	TX	CLC3OUT	—	—	—	—
	—	—	—	—	—	—	—	—	—	CCP4	—	CWG1D CWG2D	SDA <sup>(3)</sup>	—	CLC4OUT	—	—	—	—

- Note**
- 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.
  - 2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.
  - 3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.
  - 4: These pins are configured for I<sup>2</sup>C™ logic levels; clock and data signals may be assigned to any of these pins. Assignments to other pins (e.g., RA5) will operate, but logic levels will be standard TTL/ST as selected by the INLVL register.

TABLE 8: 20-PIN ALLOCATION TABLE (PIC16(L)F18345)

I/O <sup>(2)</sup>	20-Pin PDIP/SOIC/SSOP	20-Pin QFN/UQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	EUSART	CLC	CLKR	Interrupt	Pull-up	Basic
RA0	19	16	ANA0	—	C1IN0+	—	DAC1OUT	—	—	—	—	—	—	—	—	—	IOCA0	Y	ICDDAT/ ICSPDAT
RA1	18	15	ANA1	VREF+	C1IN0- C2IN0-	—	DAC1REF+	—	—	—	—	—	SS2 <sup>(1)</sup>	—	—	—	IOCA1	Y	ICDCLK/ ICSPCLK
RA2	17	14	ANA2	VREF-	—	—	DAC1REF-	—	T0CKI <sup>(1)</sup>	CCP3 <sup>(1)</sup>	—	CWG1 <sup>(1)</sup> CWG2 <sup>(1)</sup>	—	—	CLCIN0 <sup>(1)</sup>	—	INT <sup>(1)</sup> IOCA2	Y	—
RA3	4	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCA3	Y	MCLR VPP
RA4	3	20	ANA4	—	—	—	—	—	T1G <sup>(1)</sup> T3G <sup>(1)</sup> T5G <sup>(1)</sup> SOSCO	CCP4 <sup>(1)</sup>	—	—	—	—	—	—	IOCA4	Y	CLKOUT OSC2
RA5	2	19	ANA5	—	—	—	—	—	T1CKI <sup>(1)</sup> T3CKI <sup>(1)</sup> T5CKI <sup>(1)</sup> SOSCIN SOSCI	—	—	—	—	—	—	—	IOCA5	Y	CLKIN OSC1
RB4	13	10	ANB4	—	—	—	—	—	—	—	—	—	SDI1 <sup>(1)</sup> SDA1 <sup>(1,3,4)</sup>	—	CLCIN2 <sup>(1)</sup>	—	IOCB4	Y	—
RB5	12	9	ANB5	—	—	—	—	—	—	—	—	—	SDI2 <sup>(1)</sup> SDA2 <sup>(1,3,4)</sup>	RX <sup>(1)</sup> DT <sup>(1)</sup>	CLCIN3 <sup>(1)</sup>	—	IOCB5	Y	—
RB6	11	8	ANB6	—	—	—	—	—	—	—	—	—	SCK1 <sup>(1)</sup> SCL1 <sup>(1,3,4)</sup>	—	—	—	IOCB6	Y	—
RB7	10	7	ANB7	—	—	—	—	—	—	—	—	—	SCK2 <sup>(1)</sup> SCL2 <sup>(1,3,4)</sup>	TX <sup>(1)</sup> CK <sup>(1)</sup>	—	—	IOCB7	Y	—
RC0	16	13	ANC0	—	C2IN0+	—	—	—	—	—	—	—	—	—	—	—	IOCC0	Y	—
RC1	15	12	ANC1	—	C1IN1- C2IN1-	—	—	—	—	—	—	—	—	—	—	—	IOCC1	Y	—
RC2	14	11	ANC2	—	C1IN2- C2IN2-	—	—	MDCIN1 <sup>(1)</sup>	—	—	—	—	—	—	—	—	IOCC2	Y	—

- Note**
- 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.
  - 2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.
  - 3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.
  - 4: These pins are configured for I<sup>2</sup>C™ logic levels; clock and data signals may be assigned to any of these pins. Assignments to other pins (e.g., RA5) will operate, but logic levels will be standard TTL/ST as selected by the INLVL register.



**TABLE 8: 20-PIN ALLOCATION TABLE (PIC16(L)F18345)**

I/O <sup>(2)</sup>	20-Pin PDIP/SOIC/SSOP	20-Pin QFN/UQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	EUSART	CLC	CLKR	Interrupt	Pull-up	Basic
RC3	7	4	ANC3	—	C1IN3- C2IN3-	—	—	MDMIN <sup>(1)</sup>	—	CCP2 <sup>(1)</sup>	—	—	—	—	CLCIN1 <sup>(1)</sup>	—	IOCC3	Y	—
RC4	6	3	ANC4	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCC4	Y	—
RC5	5	2	ANC5	—	—	—	—	MDCIN2 <sup>(1)</sup>	—	CCP1 <sup>(1)</sup>	—	—	—	—	—	—	IOCC5	Y	—
RC6	8	5	ANC6	—	—	—	—	—	—	—	—	—	SS <sup>(1)</sup>	—	—	—	IOCC6	Y	—
RC7	9	6	ANC7	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCC7	Y	—
VDD	1	18	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD
VSS	20	17	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS
OUT <sup>(2)</sup>	—	—	—	—	C1OUT	NCO	—	DSM	TMR0	CCP1	PWM5	CWG1A CWG2A	SDO1 SDO2	DT <sup>(3)</sup>	CLC1OUT	CLKR	—	—	—
	—	—	—	—	C2OUT	—	—	—	—	CCP2	PWM6	CWG1B CWG2B	SCK1 SCK2	CK	CLC2OUT	—	—	—	—
	—	—	—	—	—	—	—	—	—	CCP3	—	CWG1C CWG2C	SCL1 <sup>(3)</sup> SCL2 <sup>(3)</sup>	TX	CLC3OUT	—	—	—	—
	—	—	—	—	—	—	—	—	—	CCP4	—	CWG1D CWG2D	SDA1 <sup>(3)</sup> SDA2 <sup>(3)</sup>	—	CLC4OUT	—	—	—	—

- Note**
- 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.
  - 2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.
  - 3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.
  - 4: These pins are configured for I<sup>2</sup>C™ logic levels; clock and data signals may be assigned to any of these pins. Assignments to other pins (e.g., RA5) will operate, but logic levels will be standard TTL/ST as selected by the INLVL register.

---

---

**Note the following details of the code protection feature on Microchip devices:**

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

#### **Trademarks**

The Microchip name and logo, the Microchip logo, dsPIC, FlashFlex, flexPWR, JukeBlox, KEELOQ, KEELOQ logo, Klear, LANCheck, MediaLB, MOST, MOST logo, MPLAB, OptoLyzer, PIC, PICSTART, PIC<sup>32</sup> logo, RightTouch, SpyNIC, SST, SST Logo, SuperFlash and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

The Embedded Control Solutions Company and mTouch are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, BodyCom, chipKIT, chipKIT logo, CodeGuard, dsPICDEM, dsPICDEM.net, ECAN, In-Circuit Serial Programming, ICSP, Inter-Chip Connectivity, KlearNet, KlearNet logo, MiWi, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, MultiTRAK, NetDetach, Omniscient Code Generation, PICDEM, PICDEM.net, PICkit, PICtail, RightTouch logo, REAL ICE, SQI, Serial Quad I/O, Total Endurance, TSHARC, USBCheck, VariSense, ViewSpan, WiperLock, Wireless DNA, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

Silicon Storage Technology is a registered trademark of Microchip Technology Inc. in other countries.

GestIC is a registered trademarks of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2014, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

ISBN: 978-1-63276-629-8

**QUALITY MANAGEMENT SYSTEM**  
**CERTIFIED BY DNV**  
**== ISO/TS 16949 ==**

*Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.*



# MICROCHIP

## Worldwide Sales and Service

### AMERICAS

**Corporate Office**  
2355 West Chandler Blvd.  
Chandler, AZ 85224-6199  
Tel: 480-792-7200  
Fax: 480-792-7277  
Technical Support:  
<http://www.microchip.com/support>  
Web Address:  
[www.microchip.com](http://www.microchip.com)

**Atlanta**  
Duluth, GA  
Tel: 678-957-9614  
Fax: 678-957-1455

**Austin, TX**  
Tel: 512-257-3370

**Boston**  
Westborough, MA  
Tel: 774-760-0087  
Fax: 774-760-0088

**Chicago**  
Itasca, IL  
Tel: 630-285-0071  
Fax: 630-285-0075

**Cleveland**  
Independence, OH  
Tel: 216-447-0464  
Fax: 216-447-0643

**Dallas**  
Addison, TX  
Tel: 972-818-7423  
Fax: 972-818-2924

**Detroit**  
Novi, MI  
Tel: 248-848-4000

**Houston, TX**  
Tel: 281-894-5983

**Indianapolis**  
Noblesville, IN  
Tel: 317-773-8323  
Fax: 317-773-5453

**Los Angeles**  
Mission Viejo, CA  
Tel: 949-462-9523  
Fax: 949-462-9608

**New York, NY**  
Tel: 631-435-6000

**San Jose, CA**  
Tel: 408-735-9110

**Canada - Toronto**  
Tel: 905-673-0699  
Fax: 905-673-6509

### ASIA/PACIFIC

**Asia Pacific Office**  
Suites 3707-14, 37th Floor  
Tower 6, The Gateway  
Harbour City, Kowloon  
Hong Kong  
Tel: 852-2943-5100  
Fax: 852-2401-3431

**Australia - Sydney**  
Tel: 61-2-9868-6733  
Fax: 61-2-9868-6755

**China - Beijing**  
Tel: 86-10-8569-7000  
Fax: 86-10-8528-2104

**China - Chengdu**  
Tel: 86-28-8665-5511  
Fax: 86-28-8665-7889

**China - Chongqing**  
Tel: 86-23-8980-9588  
Fax: 86-23-8980-9500

**China - Hangzhou**  
Tel: 86-571-8792-8115  
Fax: 86-571-8792-8116

**China - Hong Kong SAR**  
Tel: 852-2943-5100  
Fax: 852-2401-3431

**China - Nanjing**  
Tel: 86-25-8473-2460  
Fax: 86-25-8473-2470

**China - Qingdao**  
Tel: 86-532-8502-7355  
Fax: 86-532-8502-7205

**China - Shanghai**  
Tel: 86-21-5407-5533  
Fax: 86-21-5407-5066

**China - Shenyang**  
Tel: 86-24-2334-2829  
Fax: 86-24-2334-2393

**China - Shenzhen**  
Tel: 86-755-8864-2200  
Fax: 86-755-8203-1760

**China - Wuhan**  
Tel: 86-27-5980-5300  
Fax: 86-27-5980-5118

**China - Xian**  
Tel: 86-29-8833-7252  
Fax: 86-29-8833-7256

**China - Xiamen**  
Tel: 86-592-2388138  
Fax: 86-592-2388130

**China - Zhuhai**  
Tel: 86-756-3210040  
Fax: 86-756-3210049

### ASIA/PACIFIC

**India - Bangalore**  
Tel: 91-80-3090-4444  
Fax: 91-80-3090-4123

**India - New Delhi**  
Tel: 91-11-4160-8631  
Fax: 91-11-4160-8632

**India - Pune**  
Tel: 91-20-3019-1500

**Japan - Osaka**  
Tel: 81-6-6152-7160  
Fax: 81-6-6152-9310

**Japan - Tokyo**  
Tel: 81-3-6880-3770  
Fax: 81-3-6880-3771

**Korea - Daegu**  
Tel: 82-53-744-4301  
Fax: 82-53-744-4302

**Korea - Seoul**  
Tel: 82-2-554-7200  
Fax: 82-2-558-5932 or  
82-2-558-5934

**Malaysia - Kuala Lumpur**  
Tel: 60-3-6201-9857  
Fax: 60-3-6201-9859

**Malaysia - Penang**  
Tel: 60-4-227-8870  
Fax: 60-4-227-4068

**Philippines - Manila**  
Tel: 63-2-634-9065  
Fax: 63-2-634-9069

**Singapore**  
Tel: 65-6334-8870  
Fax: 65-6334-8850

**Taiwan - Hsin Chu**  
Tel: 886-3-5778-366  
Fax: 886-3-5770-955

**Taiwan - Kaohsiung**  
Tel: 886-7-213-7830

**Taiwan - Taipei**  
Tel: 886-2-2508-8600  
Fax: 886-2-2508-0102

**Thailand - Bangkok**  
Tel: 66-2-694-1351  
Fax: 66-2-694-1350

### EUROPE

**Austria - Wels**  
Tel: 43-7242-2244-39  
Fax: 43-7242-2244-393

**Denmark - Copenhagen**  
Tel: 45-4450-2828  
Fax: 45-4485-2829

**France - Paris**  
Tel: 33-1-69-53-63-20  
Fax: 33-1-69-30-90-79

**Germany - Dusseldorf**  
Tel: 49-2129-3766400

**Germany - Munich**  
Tel: 49-89-627-144-0  
Fax: 49-89-627-144-44

**Germany - Pforzheim**  
Tel: 49-7231-424750

**Italy - Milan**  
Tel: 39-0331-742611  
Fax: 39-0331-466781

**Italy - Venice**  
Tel: 39-049-7625286

**Netherlands - Drunen**  
Tel: 31-416-690399  
Fax: 31-416-690340

**Poland - Warsaw**  
Tel: 48-22-3325737

**Spain - Madrid**  
Tel: 34-91-708-08-90  
Fax: 34-91-708-08-91

**Sweden - Stockholm**  
Tel: 46-8-5090-4654

**UK - Wokingham**  
Tel: 44-118-921-5800  
Fax: 44-118-921-5820

03/25/14