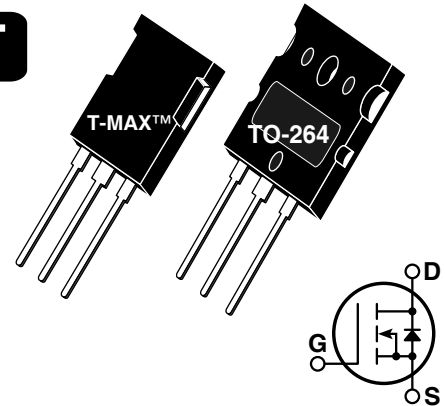


Super Junction MOSFET



- Ultra low $R_{DS(ON)}$
- Low Miller Capacitance
- Ultra Low Gate Charge, Q_g
- Avalanche Energy Rated
- Popular T-MAX™ or TO-264 Package



Unless stated otherwise, Microsemi discrete MOSFETs contain a single MOSFET die. This device is made with two parallel MOSFET die. It is intended for switch-mode operation. It is not suitable for linear mode operation.


MAXIMUM RATINGS

All Ratings: $T_C = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	APT34N80B2C3_LC3	UNIT
V_{DSS}	Drain-Source Voltage	800	Volts
I_D	Continuous Drain Current @ $T_C = 25^\circ\text{C}$	34	Amps
I_{DM}	Pulsed Drain Current ^①	102	
V_{GS}	Gate-Source Voltage Continuous	± 20	Volts
V_{GSM}	Gate-Source Voltage Transient	± 30	
P_D	Total Power Dissipation @ $T_C = 25^\circ\text{C}$	417	Watts
	Linear Derating Factor	3.33	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to 150	$^\circ\text{C}$
T_L	Lead Temperature: 0.063" from Case for 10 Sec.	300	
dv/dt	Drain-Source Voltage slope ($V_{DS} = 640\text{V}$, $I_D = 34\text{A}$, $T_J = 125^\circ\text{C}$)	50	V/ns
I_{AR}	Repetitive Avalanche Current ^⑦	17	Amps
E_{AR}	Repetitive Avalanche Energy ^⑦	0.5	mJ
E_{AS}	Single Pulse Avalanche Energy ^④	670	

STATIC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-Source Breakdown Voltage ($V_{GS} = 0\text{V}$, $I_D = 500\mu\text{A}$)	800			Volts
$R_{DS(on)}$	Drain-Source On-State Resistance ^② ($V_{GS} = 10\text{V}$, $I_D = 22\text{A}$)		0.125	0.145	Ohms
I_{DSS}	Zero Gate Voltage Drain Current ($V_{DS} = 800\text{V}$, $V_{GS} = 0\text{V}$)		1.0	50	μA
	Zero Gate Voltage Drain Current ($V_{DS} = 800\text{V}$, $V_{GS} = 0\text{V}$, $T_J = 150^\circ\text{C}$)			500	
I_{GSS}	Gate-Source Leakage Current ($V_{GS} = \pm 20\text{V}$, $V_{DS} = 0\text{V}$)			± 200	nA
$V_{GS(th)}$	Gate Threshold Voltage ($V_{DS} = V_{GS}$, $I_D = 2\text{mA}$)	2.10	3	3.9	Volts

 **CAUTION:** These Devices are Sensitive to Electrostatic Discharge. Proper Handling Procedures Should Be Followed.

Microsemi Website - <http://www.microsemi.com>

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DYNAMIC CHARACTERISTICS

APT34N80B2C3 LC3(G)

Symbol	Characteristic	Test Conditions	MIN	TYP	MAX	UNIT
C _{iss}	Input Capacitance	V _{GS} = 0V V _{DS} = 25V f = 1 MHz		4510		pF
C _{oss}	Output Capacitance			2050		
C _{rss}	Reverse Transfer Capacitance			110		
Q _g	Total Gate Charge ③	V _{GS} = 10V V _{DD} = 400V I _D = 34A @ 25°C		180	355	nC
Q _{gs}	Gate-Source Charge			22		
Q _{gd}	Gate-Drain ("Miller") Charge			90		
t _{d(on)}	Turn-on Delay Time	RESISTIVE SWITCHING V _{GS} = 10V V _{DD} = 400V I _D = 34A @ 125°C R _G = 2.5Ω		25		ns
t _r	Rise Time			15		
t _{d(off)}	Turn-off Delay Time			70	80	
t _f	Fall Time			6	9	
E _{on}	Turn-on Switching Energy ⑥	INDUCTIVE SWITCHING @ 25°C V _{DD} = 533V, V _{GS} = 15V I _D = 34A, R _G = 5Ω		675		μJ
E _{off}	Turn-off Switching Energy			580		
E _{on}	Turn-on Switching Energy ⑥	INDUCTIVE SWITCHING @ 125°C V _{DD} = 533V, V _{GS} = 15V I _D = 34A, R _G = 5Ω		1145		
E _{off}	Turn-off Switching Energy			670		

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
I _S	Continuous Source Current (Body Diode)			34	Amps
I _{SM}	Pulsed Source Current ① (Body Diode)			102	
V _{SD}	Diode Forward Voltage ② (V _{GS} = 0V, I _S = -34A)		1	1.2	Volts
t _{rr}	Reverse Recovery Time (I _S = -34A, di _S /dt = 100A/μs, V _R = 400V)		855		ns
Q _{rr}	Reverse Recovery Charge (I _S = -34A, di _S /dt = 100A/μs, V _R = 400V)		30		μC
dv/dt	Peak Diode Recovery dv/dt ⑤			6	V/ns

THERMAL CHARACTERISTICS

Symbol	Characteristic	MIN	TYP	MAX	UNIT
R _{θJC}	Junction to Case			.30	°C/W
R _{θJA}	Junction to Ambient			40	

① Repetitive Rating: Pulse width limited by maximum junction temperature

② Pulse Test: Pulse width < 380 μs, Duty Cycle < 2%

③ See MIL-STD-750 Method 3471

④ Starting T_J = +25°C, L = 115.92mH, R_G = 25Ω, Peak I_L = 3.4A

⑤ I_S = -34A di_S/dt = 100A/μs V_R = 480V T_J = 125°C

⑥ Eon includes diode reverse recovery. See figures 18, 20.

⑦ Repetitive avalanche causes additional power losses that can be calculated as P_{AV} = E_{AR} * f

Microsemi reserves the right to change, without notice, the specifications and information contained herein.

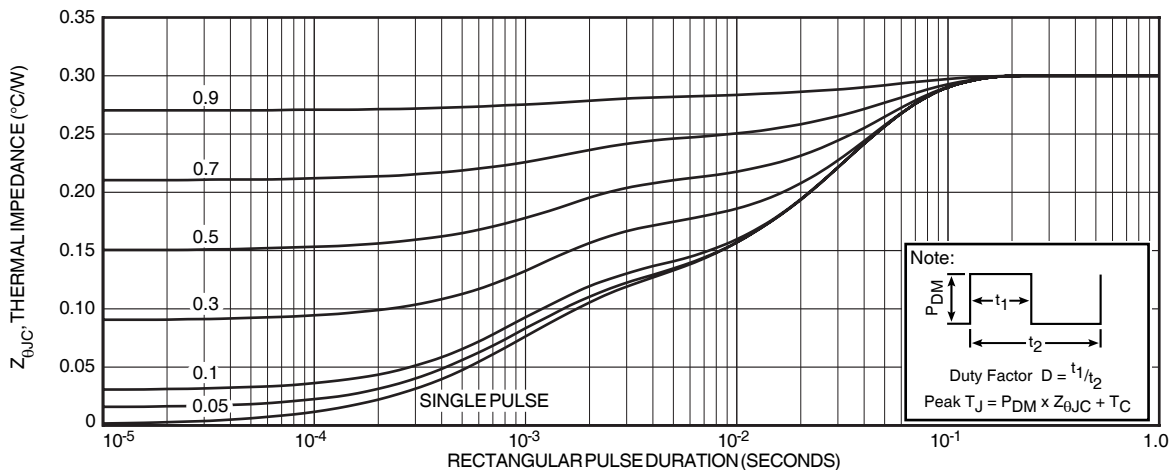


FIGURE 1, MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

Typical Performance Curves

APT34N80B2C3_LC3(G)

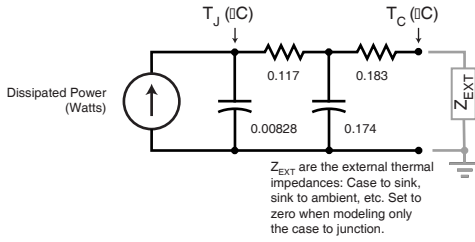


FIGURE 2, TRANSIENT THERMAL IMPEDANCE MODEL

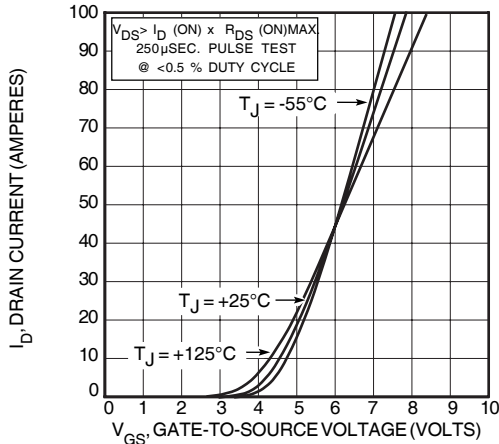


FIGURE 4, TRANSFER CHARACTERISTICS

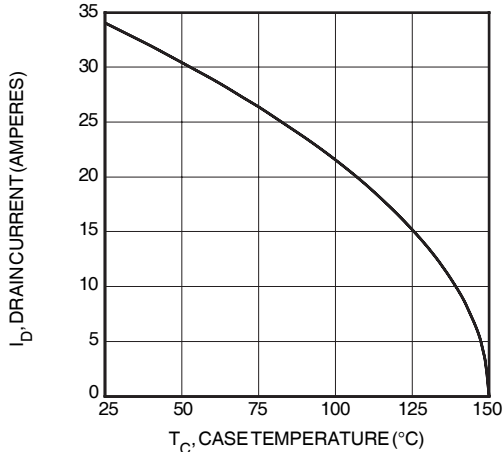


FIGURE 6, MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

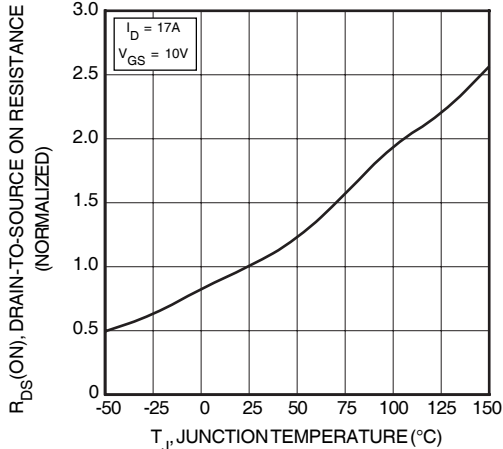


FIGURE 8, ON-RESISTANCE vs. TEMPERATURE

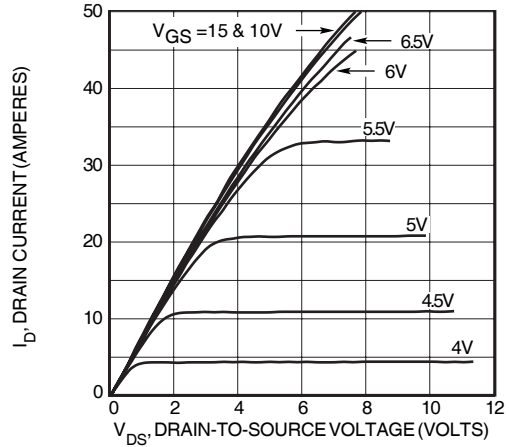


FIGURE 3, LOW VOLTAGE OUTPUT CHARACTERISTICS

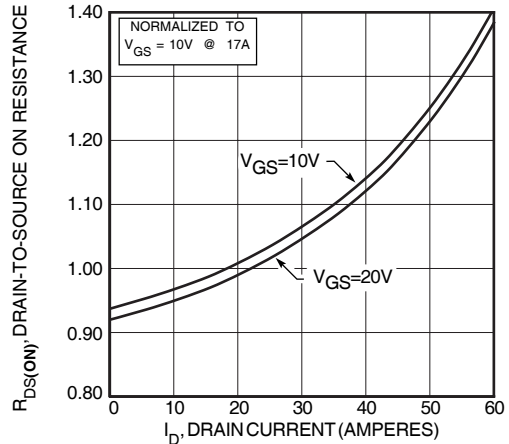


FIGURE 5, $R_{DS(ON)}$ vs DRAIN CURRENT

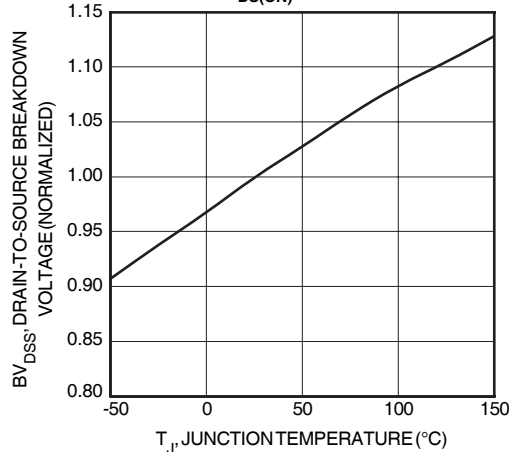


FIGURE 7, BREAKDOWN VOLTAGE vs TEMPERATURE

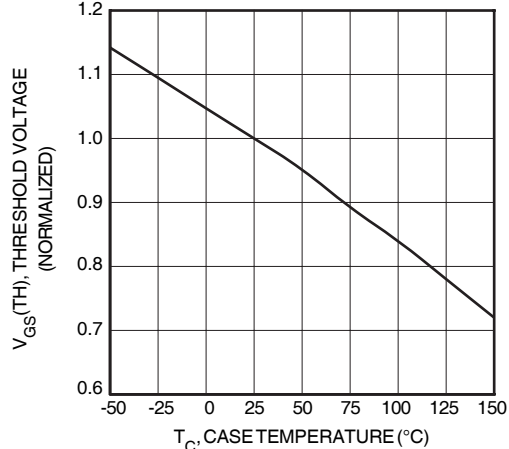


FIGURE 9, THRESHOLD VOLTAGE vs TEMPERATURE

Typical Performance Curves

APT34N80B2C3_LC3(G)

I_D , DRAIN CURRENT (AMPERES)

Graph removed

V_{DS} , DRAIN-TO-SOURCE VOLTAGE (VOLTS)
FIGURE 10, MAXIMUM SAFE OPERATING AREA

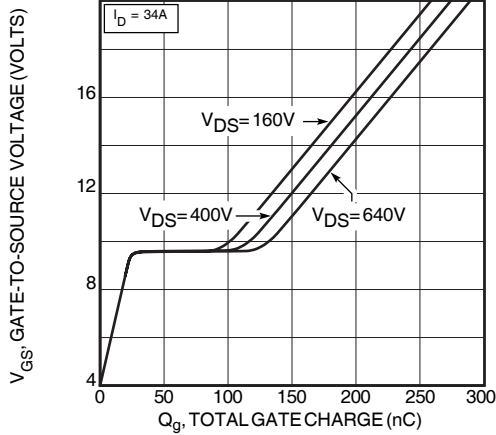


FIGURE 12, GATE CHARGES vs GATE-TO-SOURCE VOLTAGE

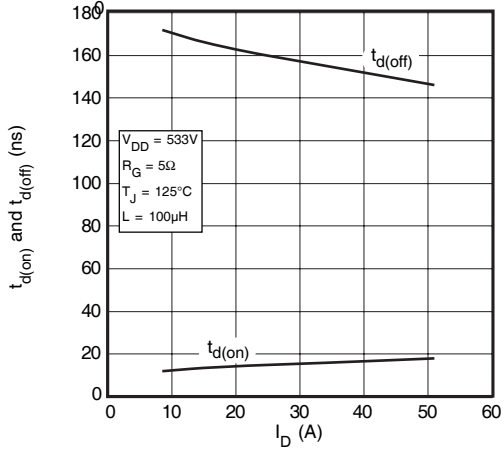


FIGURE 14, DELAY TIMES vs CURRENT

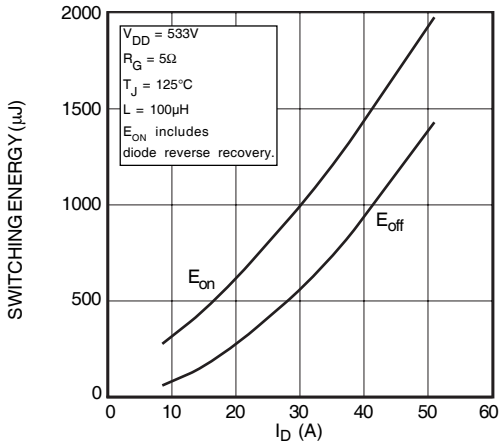


FIGURE 15, RISE AND FALL TIMES vs CURRENT

FIGURE 16, SWITCHING ENERGY vs CURRENT

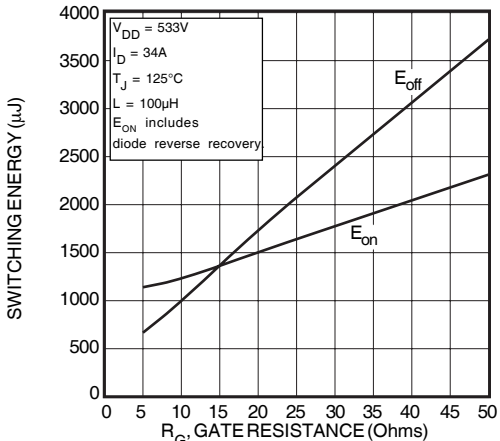
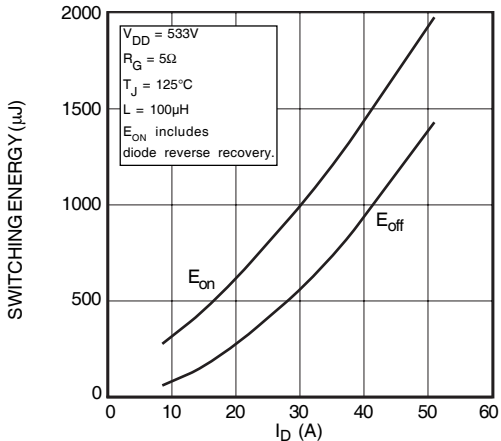


FIGURE 17, SWITCHING ENERGY VS. GATE RESISTANCE

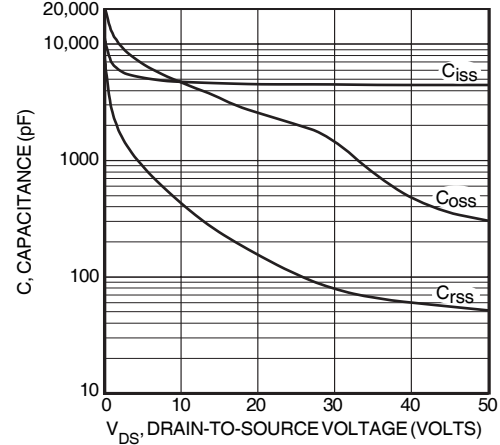


FIGURE 11, CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

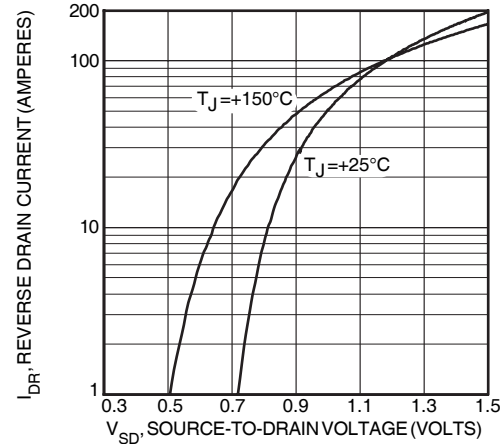


FIGURE 13, SOURCE-DRAIN DIODE FORWARD VOLTAGE

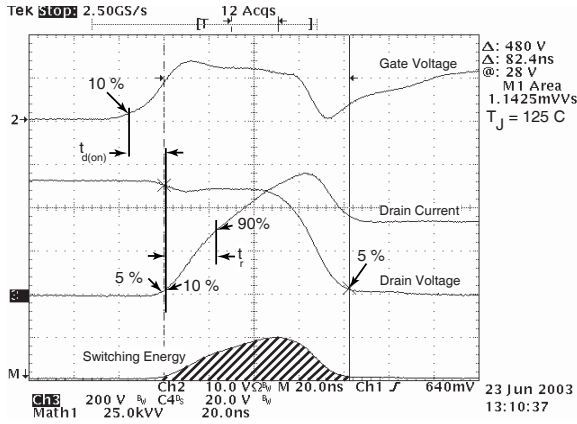


Figure 18, Turn-on Switching Waveforms and Definitions

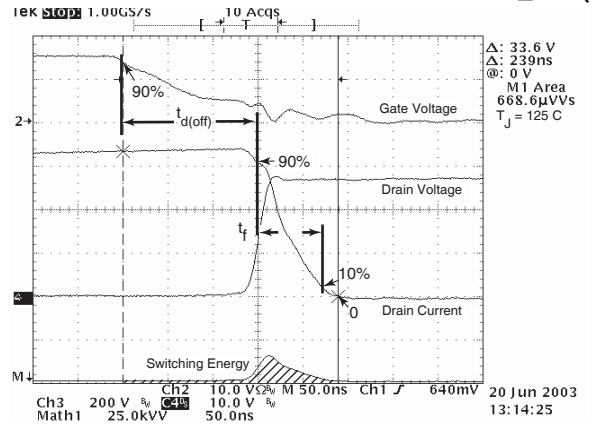


Figure 19, Turn-off Switching Waveforms and Definitions

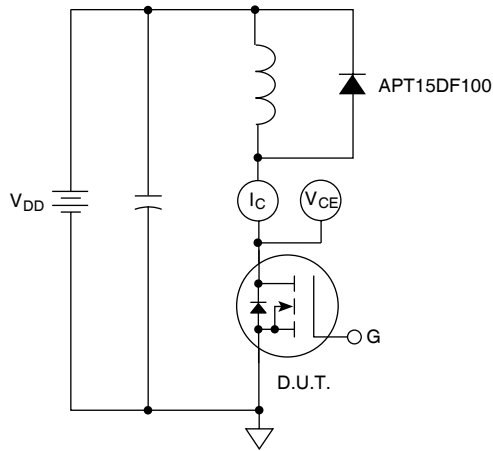
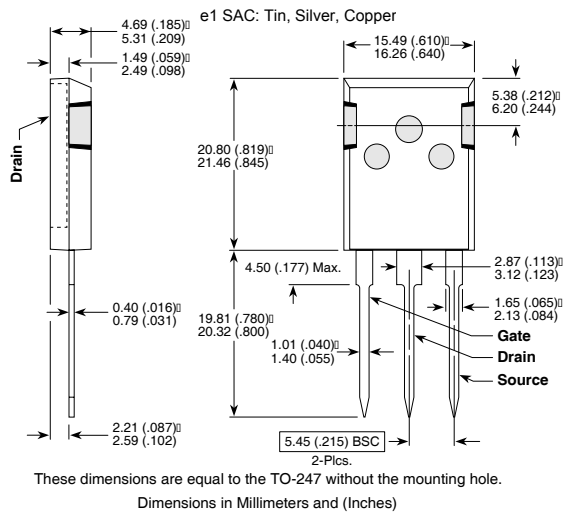


Figure 20, Inductive Switching Test Circuit

T-MAX™ (B2) Package Outline



TO-264 (L) Package Outline

