



NPN SILICON TRANSISTOR

Qualified per MIL-PRF-19500/366

*Qualified Levels:
JAN, JANTX, JANTXV
and JANS*

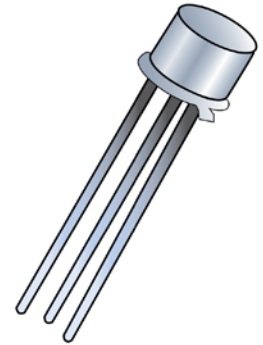
DESCRIPTION

This family of 2N3498 thru 2N3501 epitaxial planar transistors are military qualified up to a JANS level for high-reliability applications. These devices are also available in TO-5 and low profile U4 packaging. Microsemi also offers numerous other transistor products to meet higher and lower power ratings with various switching speed requirements in both through-hole and surface-mount packages.

Important: For the latest information, visit our website <http://www.microsemi.com>.

FEATURES

- JEDEC registered 2N3498 through 2N3501 series.
- JAN, JANTX, JANTXV, and JANS qualifications are available per MIL-PRF-19500/366. (See [part nomenclature](#) for all available options.)
- RoHS compliant versions available (commercial grade only).





**TO-39 (TO-205AD)
Package**

Also available in:

APPLICATIONS / BENEFITS

- General purpose transistors for medium power applications requiring high frequency switching and low package profile.
- Military and other high-reliability applications.

TO-5 package
(long-leaded)
 2N3498L – 2N3501L

U4 package
(surface mount)
 2N3498U4 – 2N3501U4

MAXIMUM RATINGS

Parameters / Test Conditions	Symbol	2N3498 2N3499	2N3500 2N3501	Unit
Collector-Emitter Voltage	V_{CE0}	100	150	V
Collector-Base Voltage	V_{CB0}	100	150	V
Emitter-Base Voltage	V_{EB0}	6.0	6.0	V
Collector Current	I_C	500	300	mA
Thermal Resistance Junction-to-Ambient	$R_{\theta JA}$	175		$^{\circ}C/W$
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	30		$^{\circ}C/W$
Total Power Dissipation @ $T_A = +25^{\circ}C$ ⁽¹⁾ @ $T_C = +25^{\circ}C$ ⁽²⁾	P_T	1.0 5.0		W
Operating & Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		$^{\circ}C$

- Notes:**
1. See [figure 1](#).
 2. See [figure 2](#).

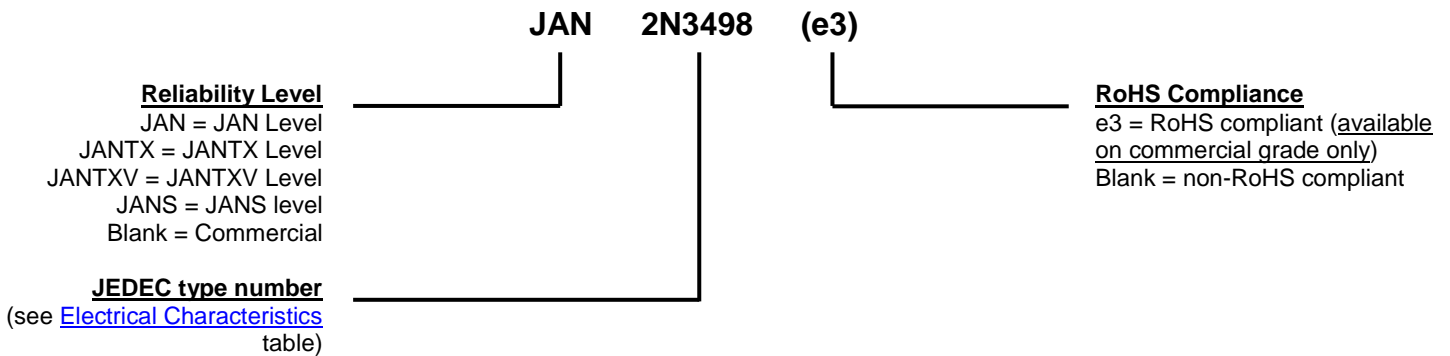
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MECHANICAL and PACKAGING

- CASE: Hermetically sealed, kovar base, nickel cap.
- TERMINALS: Leads are kovar, nickel plated, and finish is solder dip (Sn63/Pb37). Can be RoHS compliant with pure matte-tin (commercial grade only).
- MARKING: Part number, date code, manufacturer's ID.
- WEIGHT: Approximately 1.064 grams.
- See [Package Dimensions](#) on last page.

PART NOMENCLATURE

SYMBOLS & DEFINITIONS

Symbol	Definition
C_{obo}	Common-base open-circuit output capacitance
I_{CEO}	Collector cutoff current, base open
I_{CEX}	Collector cutoff current, circuit between base and emitter
I_{EBO}	Emitter cutoff current, collector open
h_{FE}	Common-emitter static forward current transfer ratio
V_{CEO}	Collector-emitter voltage, base open
V_{CBO}	Collector-emitter voltage, emitter open
V_{EBO}	Emitter-base voltage, collector open

ELECTRICAL CHARACTERISTICS @ $T_A = +25\text{ }^\circ\text{C}$, unless otherwise noted

Characteristic	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage $I_C = 10\text{ mA}$, pulsed	$V_{(BR)CEO}$	100 150		V
Collector-Base Cutoff Current $V_{CB} = 50\text{ V}$	I_{CBO}		50	nA
$V_{CB} = 75\text{ V}$			50	nA
$V_{CB} = 100\text{ V}$			10	μA
$V_{CB} = 150\text{ V}$			10	μA
Emitter-Base Cutoff Current $V_{EB} = 4.0\text{ V}$	I_{EBO}		25	nA
$V_{EB} = 6.0\text{ V}$			10	μA

ON CHARACTERISTICS ⁽¹⁾

Forward-Current Transfer Ratio $I_C = 0.1\text{ mA}$, $V_{CE} = 10\text{ V}$	h_{FE}	20 35		
$I_C = 1.0\text{ mA}$, $V_{CE} = 10\text{ V}$		25 50		
$I_C = 10\text{ mA}$, $V_{CE} = 10\text{ V}$		35 75		
$I_C = 150\text{ mA}$, $V_{CE} = 10\text{ V}$		40 100	120 300	
$I_C = 300\text{ mA}$, $V_{CE} = 10\text{ V}$		15 20		
$I_C = 500\text{ mA}$, $V_{CE} = 10\text{ V}$		15 20		
Collector-Emitter Saturation Voltage $I_C = 10\text{ mA}$, $I_B = 1.0\text{ mA}$		$V_{CE(sat)}$		0.2
$I_C = 300\text{ mA}$, $I_B = 30\text{ mA}$			0.6	
$I_C = 150\text{ mA}$, $I_B = 15\text{ mA}$			0.4	
Base-Emitter Saturation Voltage $I_C = 10\text{ mA}$, $I_B = 1.0\text{ mA}$	$V_{BE(sat)}$		0.8	V
$I_C = 300\text{ mA}$, $I_B = 30\text{ mA}$			1.4	
$I_C = 150\text{ mA}$, $I_B = 15\text{ mA}$			1.2	

DYNAMIC CHARACTERISTICS

Forward Current Transfer Ratio, Magnitude $I_C = 20\text{ mA}$, $V_{CE} = 20\text{ V}$, $f = 100\text{ MHz}$	$ h_{fe} $	1.5	8.0	
Output Capacitance $V_{CB} = 10\text{ V}$, $I_E = 0$, $100\text{ kHz} \leq f \leq 1.0\text{ MHz}$	C_{obo}		10 8.0	pF
Input Capacitance $V_{EB} = 0.5\text{ V}$, $I_C = 0$, $100\text{ kHz} \leq f \leq 1.0\text{ MHz}$		C_{ibo}		80

(1) Pulse Test: pulse width = 300 μs , duty cycle $\leq 2.0\%$.

ELECTRICAL CHARACTERISTICS @ $T_A = +25^\circ\text{C}$, unless otherwise noted
SWITCHING CHARACTERISTICS

Characteristic	Symbol	Min.	Max.	Unit
Turn-On Time $V_{EB} = 5\text{ V}; I_C = 150\text{ mA}; I_{B1} = 15\text{ mA}$	t_{on}		115	ns
Turn-Off Time $I_C = 150\text{ mA}; I_{B1} = I_{B2} = -15\text{ mA}$	t_{off}		1150	ns

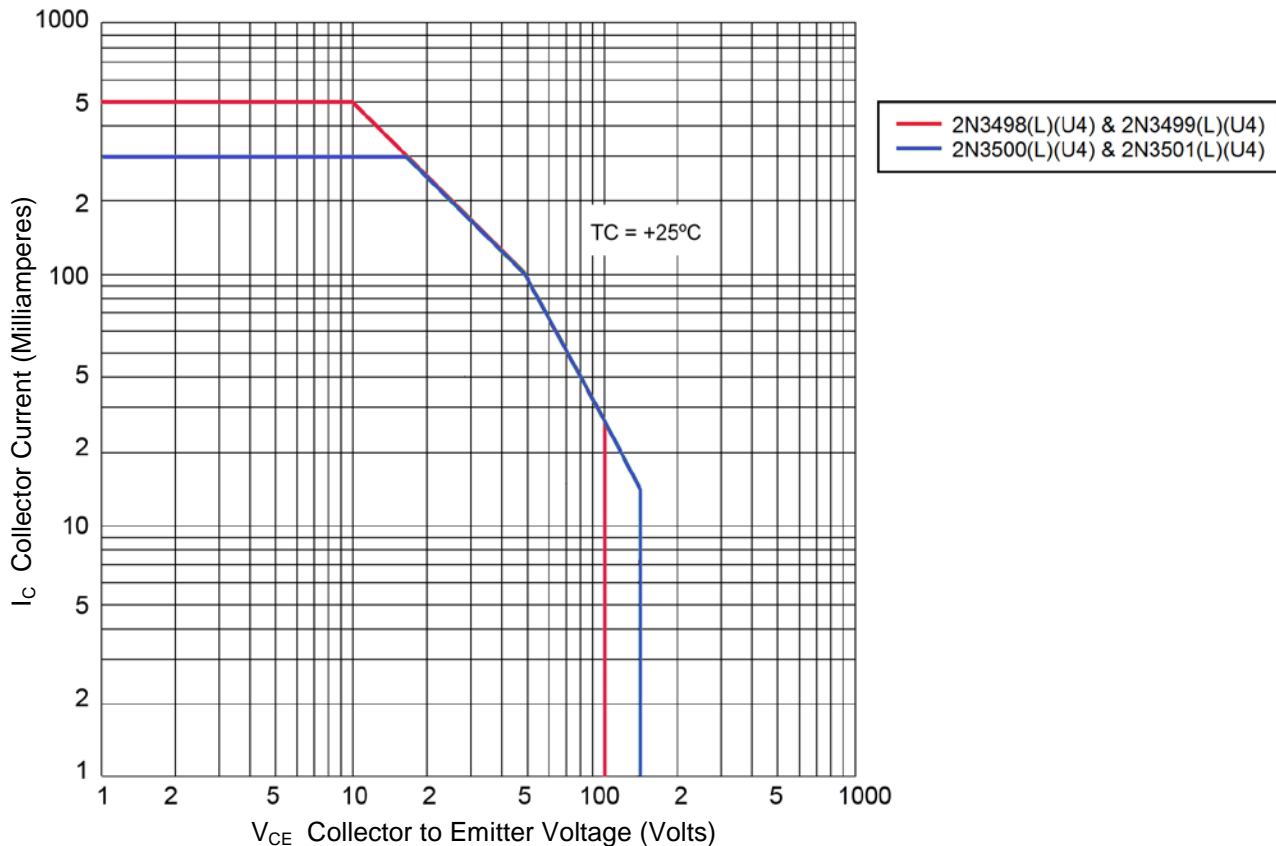
SAFE OPERATING AREA (See SOA figure and reference [MIL-STD-750 method 3053](#))
DC Tests
 $T_C = +25^\circ\text{C}$, $t_r \geq 10\text{ ns}$; 1 Cycle, $t = 1.0\text{ s}$
Test 1
 $V_{CE} = 10\text{ V}, I_C = 500\text{ mA}$ 2N3498, 2N3499

 $V_{CE} = 16.67\text{ V}, I_C = 300\text{ mA}$ 2N3500, 2N3501

Test 2
 $V_{CE} = 50\text{ V}, I_C = 100\text{ mA}$ All Types

Test 3
 $V_{CE} = 80\text{ V}, I_C = 40\text{ mA}$ All Types

Clamped Switching
 $T_A = +25^\circ\text{C}$
Test 1
 $I_B = 85\text{ mA}, I_C = 500\text{ mA}$ 2N3498, 2N3499

 $I_B = 50\text{ mA}, I_C = 300\text{ mA}$ 2N3500, 2N3501

Maximum Safe Operating Area

GRAPHS

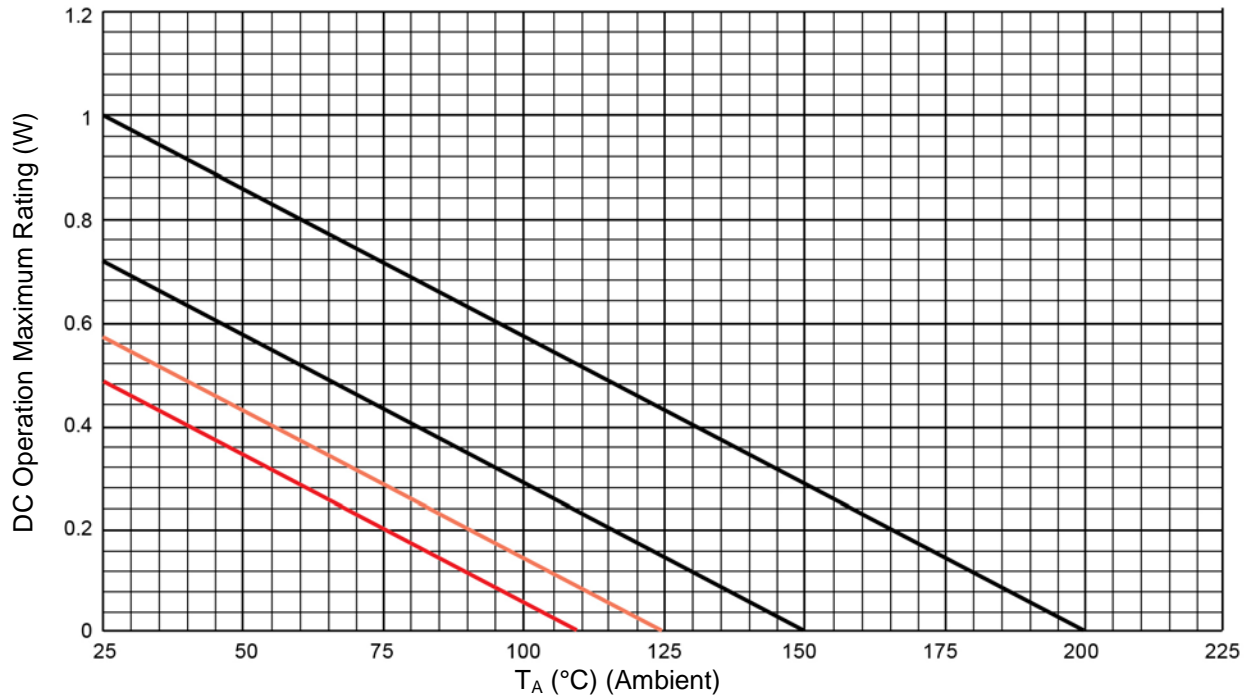


FIGURE 1
Derating for all devices ($R_{\theta JA}$)

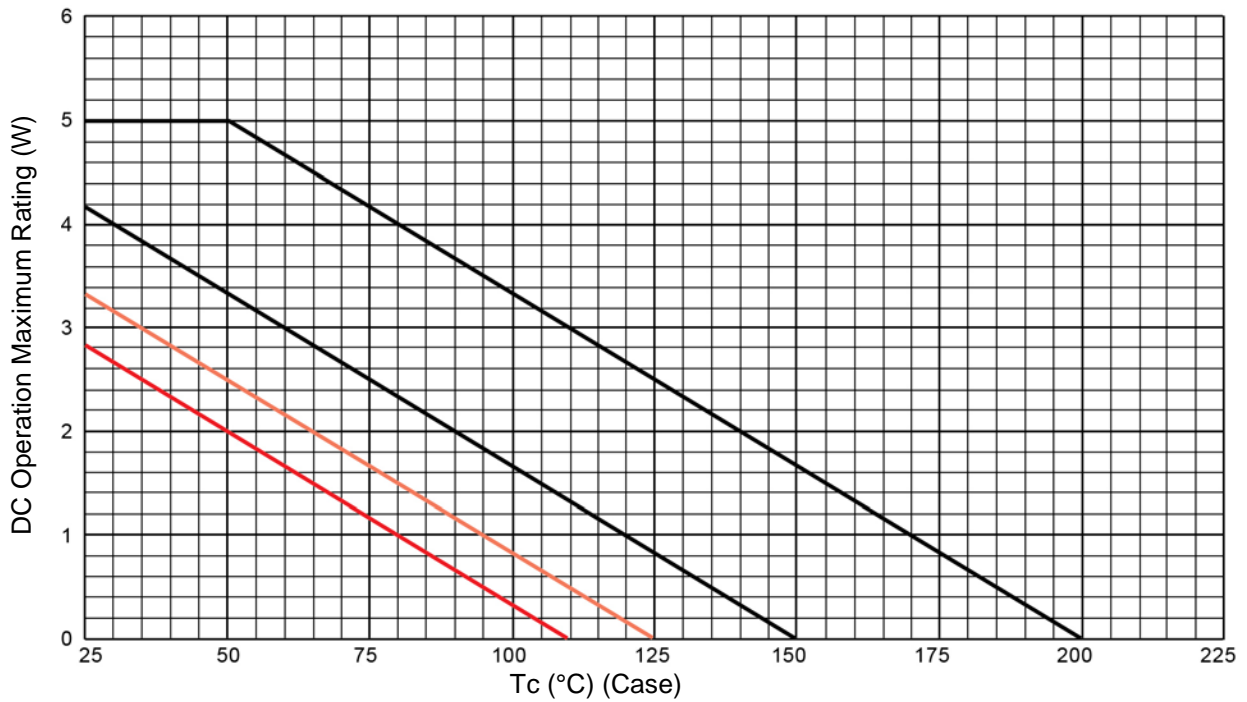


FIGURE 2
Derating for all devices ($R_{\theta JC}$)

GRAPHS

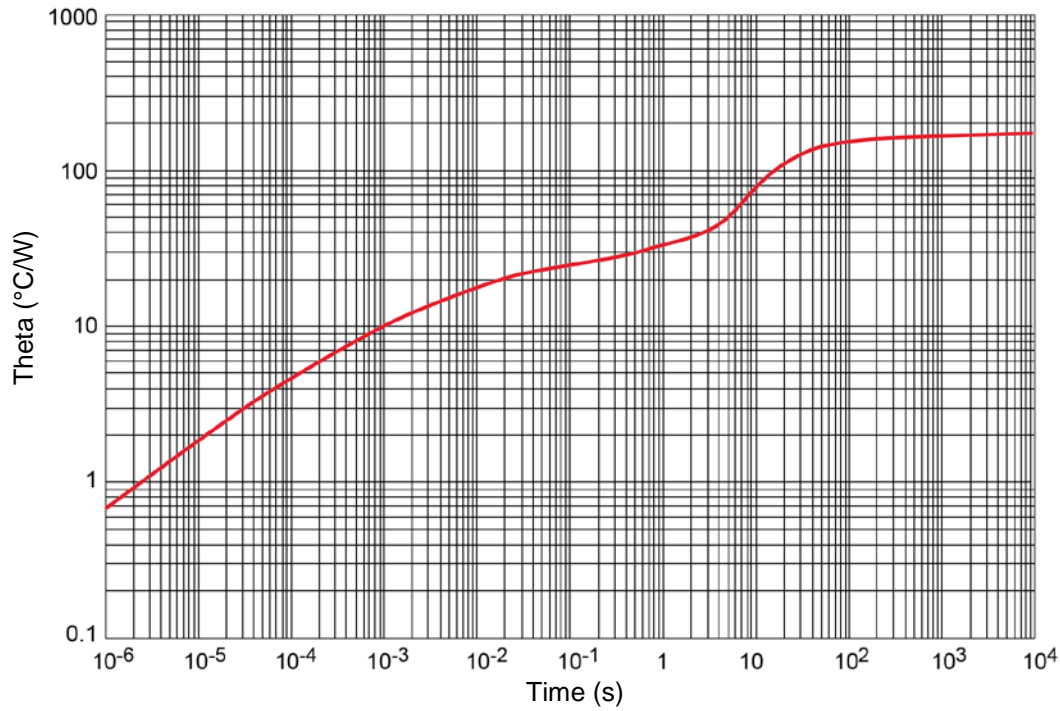


FIGURE 3
Thermal Impedance Graph ($R_{\theta JA}$)

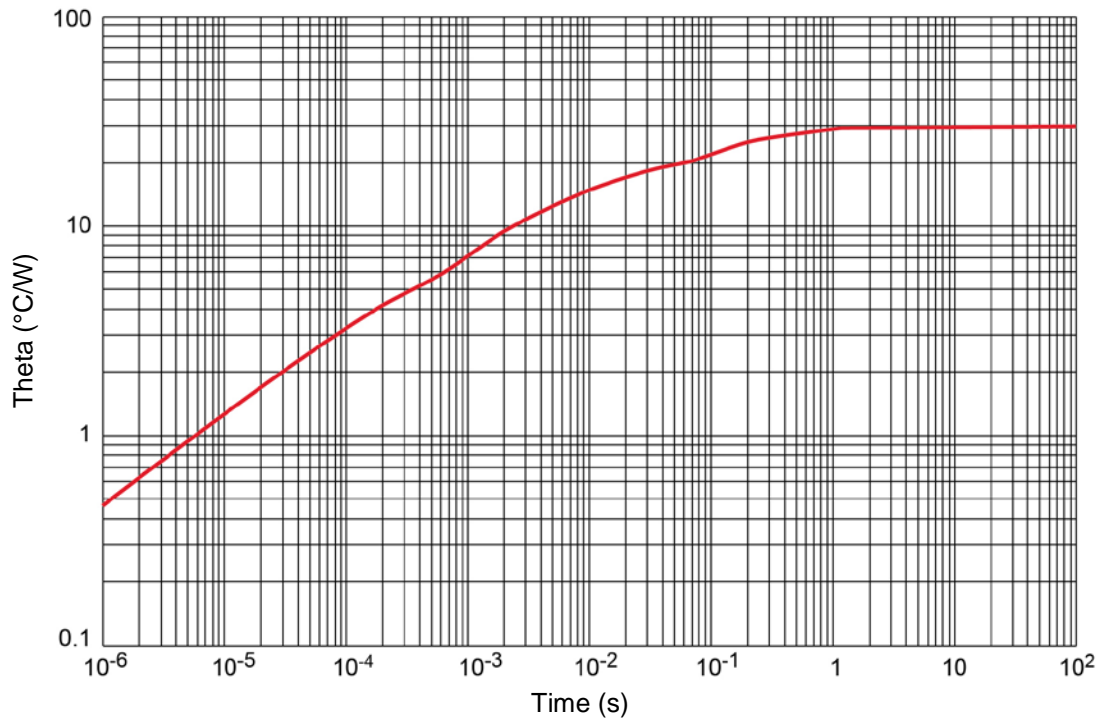
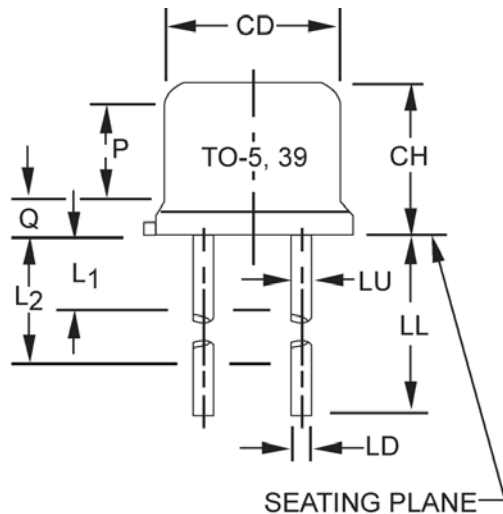


FIGURE 4
Thermal Impedance Graph ($R_{\theta JC}$)

PACKAGE DIMENSIONS


Symbol	Dimensions				Note
	Inch		Millimeters		
	Min	Max	Min	Max	
CD	0.305	0.335	7.75	8.51	
CH	0.240	0.260	6.10	6.60	
HD	0.335	0.370	8.51	9.40	
LC	0.200 TP		5.08 TP		6
LD	0.016	0.021	0.41	0.53	7
LL	See notes 7, 12 and 13				
LU	0.016	0.019	0.41	0.48	7, 13
L1		0.050		1.27	13
L2	0.250		6.35		13
P	0.100		2.54		5
Q		0.050		1.27	4
TL	0.029	0.045	0.74	1.14	3
TW	0.028	0.034	0.71	0.86	10, 11
r		0.010		0.25	11
α	45° TP		45° TP		6

NOTES:

1. Dimension are in inches.
2. Millimeters are given for general information only.
3. Symbol TL is measured from HD maximum.
4. Details of outline in this zone are optional.
5. Symbol CD shall not vary more than .010 (0.25 mm) in zone P. This zone is controlled for automatic handling.
6. Leads at gauge plane .054 inch (1.37 mm) +.001 inch (0.03 mm) -.000 inch (0.00 mm) below seating plane shall be within .007 inch (0.18 mm) radius of true position (TP) relative to tab. Device may be measured by direct methods or by gauge.
7. Symbol LD applies between L1 and L2. Dimension LD applies between L2 and LL minimum. Lead diameter shall not exceed .042 inch (1.07 mm) within L1 and beyond LL minimum.
8. Lead designation, shall be as follows: 1 - emitter, 2 - base, 3 - collector.
9. Lead number three is electrically connected to case.
10. Beyond r maximum, TW shall be held for a minimum length of .011 inch (0.28 mm).
11. Symbol r applied to both inside corners of tab.
12. For transistor types 2N3498, 2N3499, 2N3500, and 2N3501, LL = .50 inch (12.7 mm) minimum and .750 inch (19.1 mm) maximum. For transistor types 2N3498L, 2N3499L, 2N3500L, and 2N3501L, LL = 1.50 inches (38.1 mm) minimum and 1.750 inches (44.5 mm) maximum.
13. All three leads.
14. In accordance with ASME Y14.5M, diameters are equivalent to Φ x symbology.