

BT151S series L and R

Thyristors

Rev. 05 — 9 October 2006

Product data sheet

1. Product profile

1.1 General description

Passivated thyristors in a SOT428 plastic package.

1.2 Features

- High thermal cycling performance
- High bidirectional blocking voltage capability
- Surface-mounted package

1.3 Applications

- Motor control
- Ignition circuits
- Static switching
- Protection circuits

1.4 Quick reference data

- $V_{DRM} \leq 500$ V (BT151S-500L/R)
- $V_{RRM} \leq 500$ V (BT151S-500L/R)
- $V_{DRM} \leq 650$ V (BT151S-650L/R)
- $V_{RRM} \leq 650$ V (BT151S-650L/R)
- $V_{DRM} \leq 800$ V (BT151S-800R)
- $V_{RRM} \leq 800$ V (BT151S-800R)
- $I_{TSM} \leq 120$ A ($t = 10$ ms)
- $I_{T(RMS)} \leq 12$ A
- $I_{T(AV)} \leq 7.5$ A
- $I_{GT} \leq 5$ mA (BT151S series L)
- $I_{GT} \leq 15$ mA (BT151S series R)

2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline	Symbol
1	cathode (K)	<p>SOT428 (DPAK)</p>	<p>A K G sym037</p>
2	anode (A)		
3	gate (G)		
mb	mounting base; connected to anode		

3. Ordering information

Table 2. Ordering information

Type number	Package		Version
	Name	Description	
BT151S-500L	DPAK	plastic single-ended surface-mounted package; 3 leads (one lead cropped)	SOT428
BT151S-500R			
BT151S-650L			
BT151S-650R			
BT151S-800R			
BT151S-800R			

4. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage	BT151S-500L; BT151S-500R	[1] -	500	V
		BT151S-650L; BT151S-650R	[1] -	650	V
		BT151S-800R	-	800	V
V_{RRM}	repetitive peak reverse voltage	BT151S-500L; BT151S-500R	[1] -	500	V
		BT151S-650L; BT151S-650R	[1] -	650	V
		BT151S-800R	-	800	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{mb} \leq 103\text{ °C}$; see Figure 1	-	7.5	A
$I_{T(RMS)}$	RMS on-state current	all conduction angles; see Figure 4 and 5	-	12	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_j = 25\text{ °C}$ prior to surge; see Figure 2 and 3			
		$t = 10\text{ ms}$	-	120	A
		$t = 8.3\text{ ms}$	-	132	A
I^2t	I^2t for fusing	$t = 10\text{ ms}$	-	72	A ² s
di_T/dt	rate of rise of on-state current	$I_{TM} = 20\text{ A}$; $I_G = 50\text{ mA}$; $di_G/dt = 50\text{ mA}/\mu\text{s}$	-	50	A/ μs
I_{GM}	peak gate current		-	2	A
V_{RGM}	peak reverse gate voltage		-	5	V
P_{GM}	peak gate power		-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.5	W
T_{stg}	storage temperature		-40	+150	°C
T_j	junction temperature		-	125	°C

[1] Although not recommended, off-state voltages up to 800 V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15A/ μs .

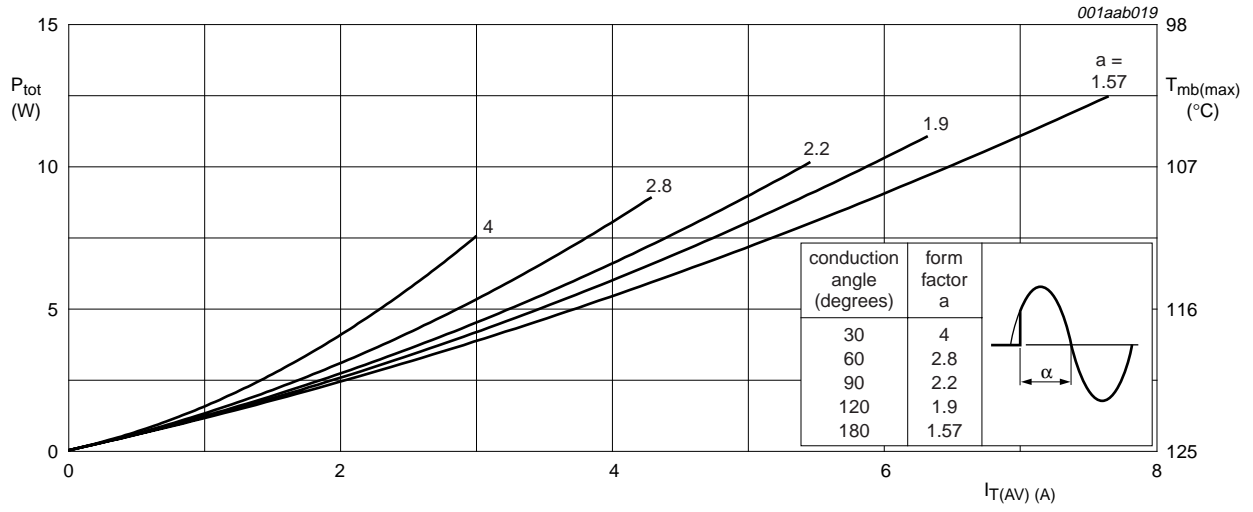


Fig 1. Total power dissipation as a function of average on-state current; maximum values

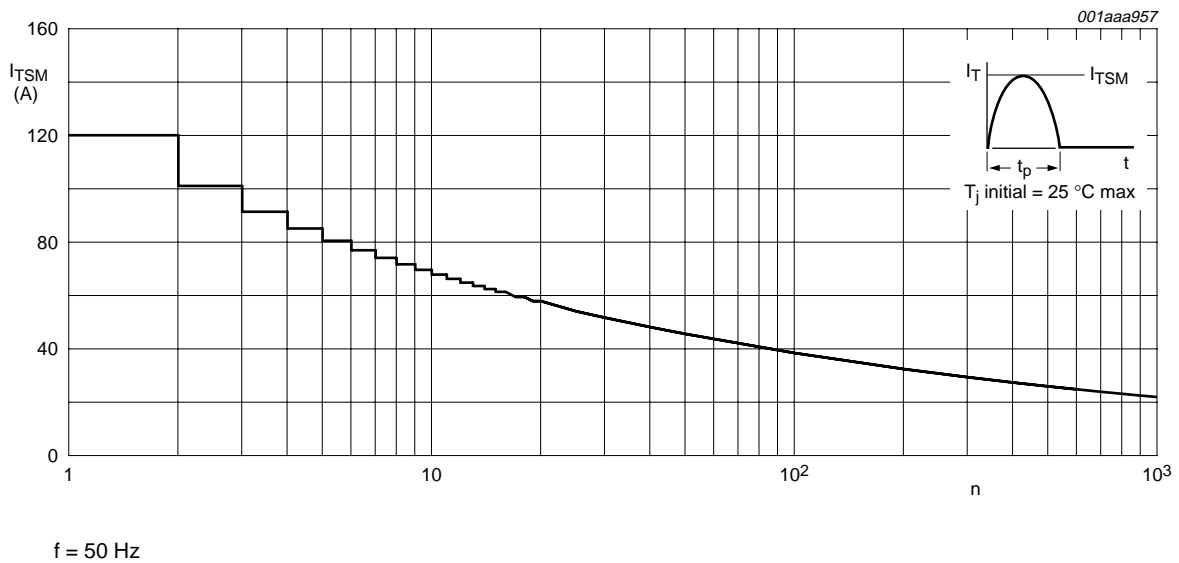
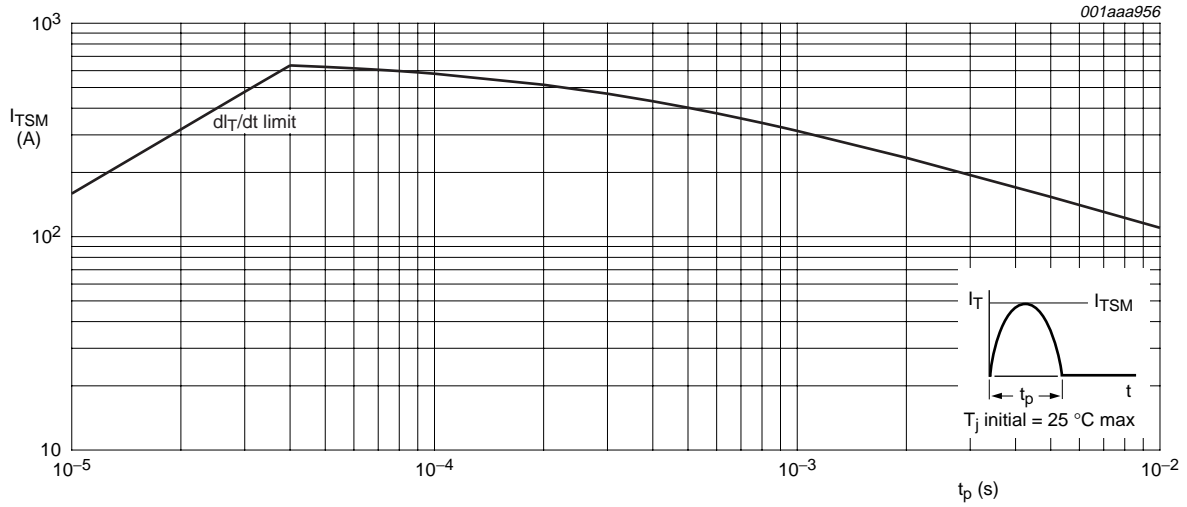
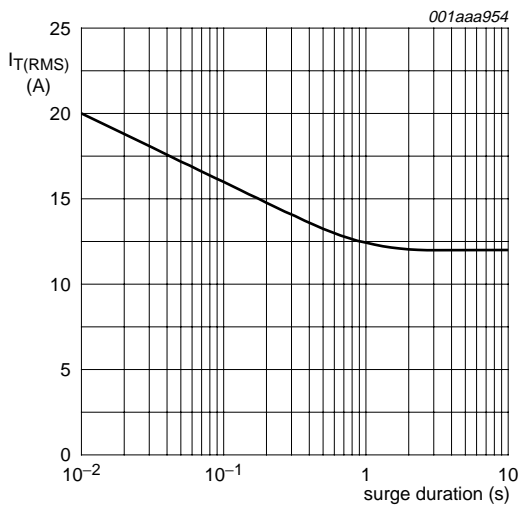


Fig 2. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



$t_p \leq 10$ ms

Fig 3. Non-repetitive peak on-state current as a function of pulse width for sinusoidal currents; maximum values



$f = 50$ Hz; $T_{mb} \leq 103$ °C

Fig 4. RMS on-state current as a function of surge duration; maximum values

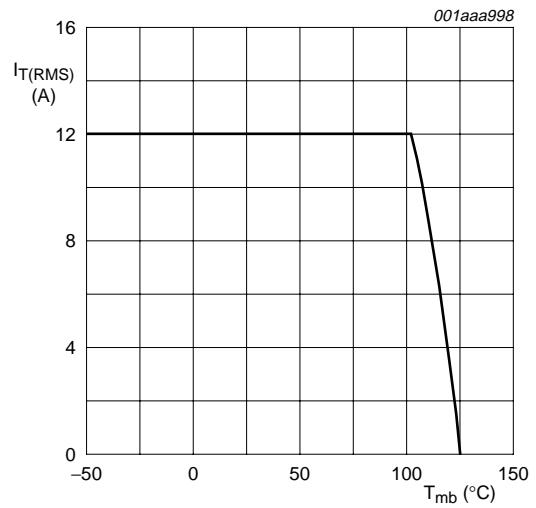
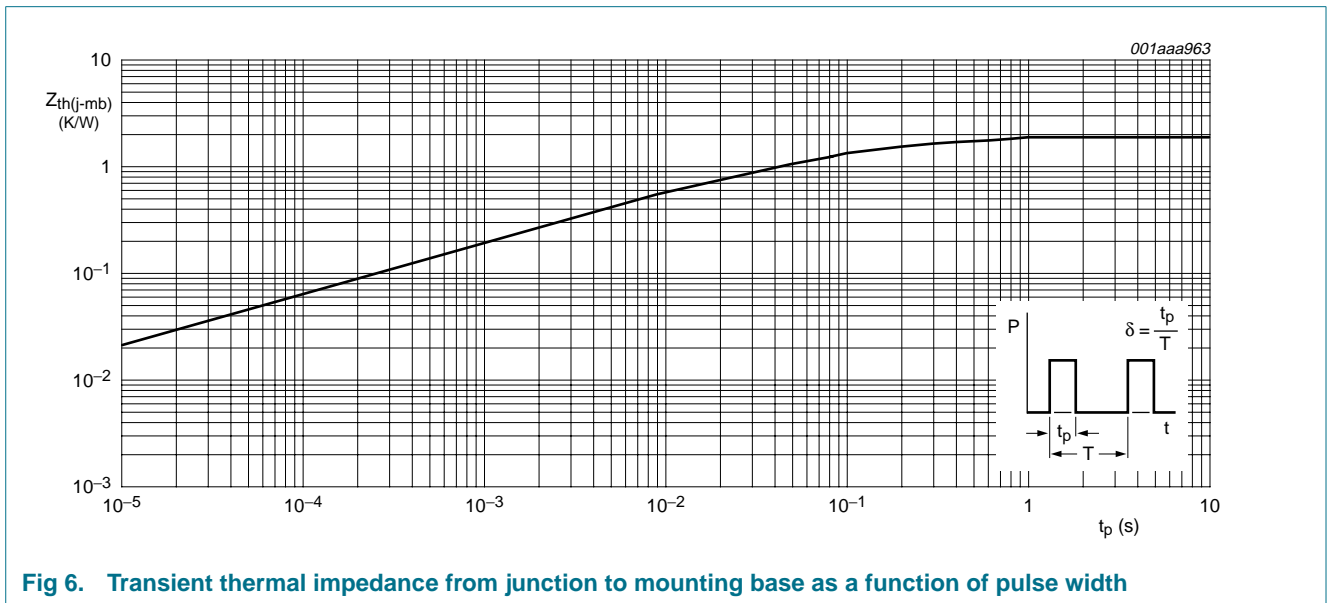


Fig 5. RMS on-state current as a function of mounting base temperature; maximum values

5. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 6	-	-	1.8	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on an FR4 printed-circuit board; see Figure 14	-	75	-	K/W



6. Characteristics

Table 5. Characteristics

$T_j = 25\text{ °C}$ unless otherwise stated.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 100\text{ mA}$; see Figure 8				
		BT151S-500L	-	2	5	mA
		BT151S-500R	-	2	15	mA
		BT151S-650L	-	2	5	mA
		BT151S-650R	-	2	15	mA
		BT151S-800R	-	2	15	mA
I_L	latching current	$V_D = 12\text{ V}$; $I_{GT} = 100\text{ mA}$; see Figure 10	-	10	40	mA
I_H	holding current	$V_D = 12\text{ V}$; $I_{GT} = 100\text{ mA}$; see Figure 11	-	7	20	mA
V_T	on-state voltage	$I_T = 23\text{ A}$; see Figure 9	-	1.4	1.75	V
V_{GT}	gate trigger voltage	$I_T = 100\text{ mA}$; $V_D = 12\text{ V}$; see Figure 7	-	0.6	1.5	V
		$I_T = 100\text{ mA}$; $V_D = V_{DRM(max)}$; $T_j = 125\text{ °C}$	0.25	0.4	-	V
I_D	off-state current	$V_D = V_{DRM(max)}$; $T_j = 125\text{ °C}$	-	0.1	0.5	mA
I_R	reverse current	$V_R = V_{RRM(max)}$; $T_j = 125\text{ °C}$	-	0.1	0.5	mA
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 0.67 \times V_{DRM(max)}$; $T_j = 125\text{ °C}$; exponential waveform; see Figure 12				
		$R_{GK} = 100\ \Omega$	200	1000	-	V/ μ s
		gate open circuit	50	130	-	V/ μ s
t_{gt}	gate-controlled turn-on time	$I_{TM} = 40\text{ A}$; $V_D = V_{DRM(max)}$; $I_G = 100\text{ mA}$; $dl_G/dt = 5\text{ A}/\mu\text{s}$	-	2	-	μ s
t_q	commutated turn-off time	$V_{DM} = 0.67 \times V_{DRM(max)}$; $T_j = 125\text{ °C}$; $I_{TM} = 20\text{ A}$; $V_R = 25\text{ V}$; $(dl_T/dt)_M = 30\text{ A}/\mu\text{s}$; $dV_D/dt = 50\text{ V}/\mu\text{s}$; $R_{GK} = 100\ \Omega$	-	70	-	μ s

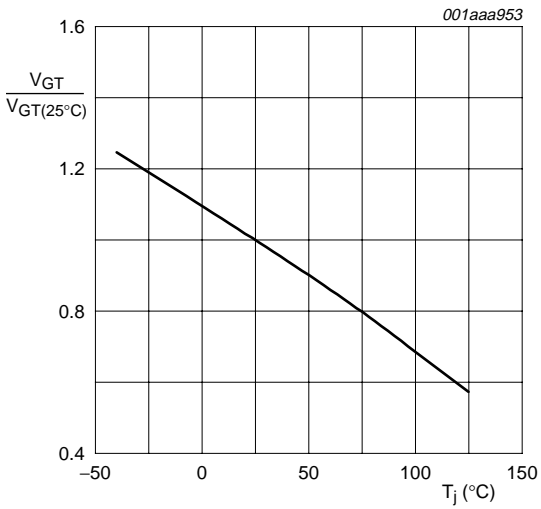


Fig 7. Normalized gate trigger voltage as a function of junction temperature

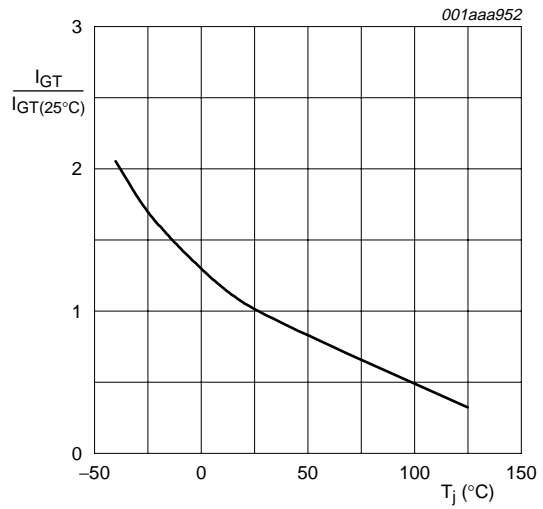
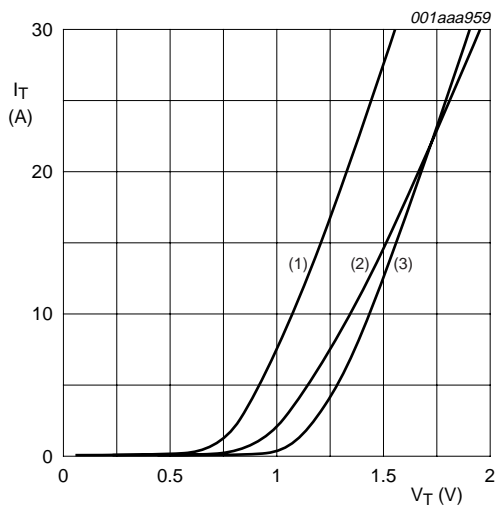


Fig 8. Normalized gate trigger current as a function of junction temperature



$V_o = 1.06\text{ V}$
 $R_s = 0.0304\ \Omega$

- (1) $T_j = 125\text{ }^\circ\text{C}$; typical values
- (2) $T_j = 125\text{ }^\circ\text{C}$; maximum values
- (3) $T_j = 25\text{ }^\circ\text{C}$; maximum values

Fig 9. On-state current as a function of on-state voltage

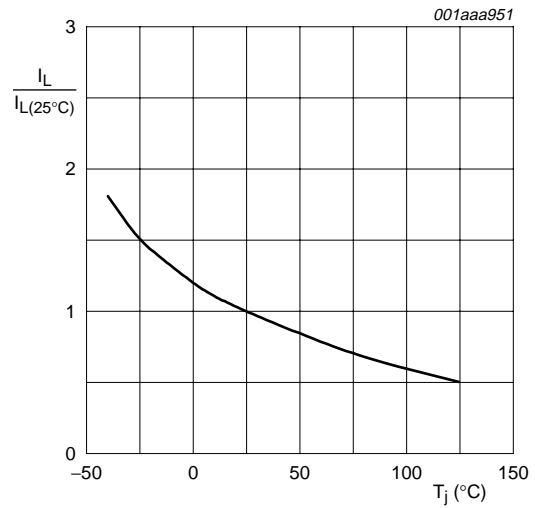


Fig 10. Normalized latching current as a function of junction temperature

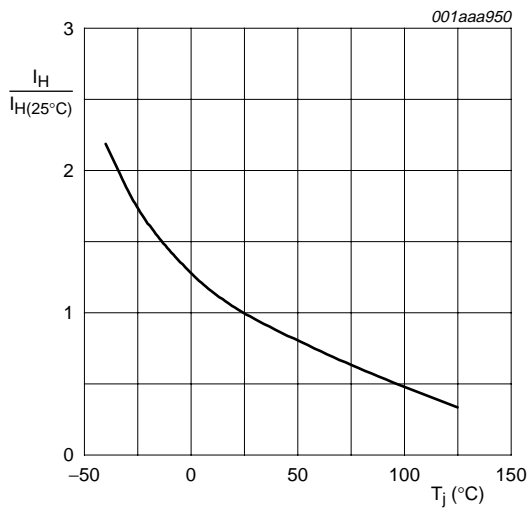


Fig 11. Normalized holding current as a function of junction temperature

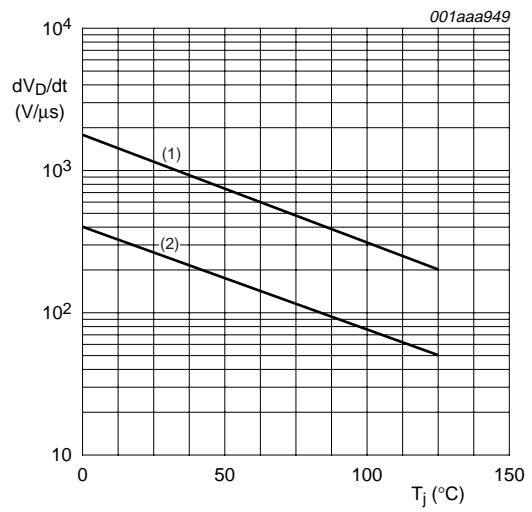


Fig 12. Critical rate of rise of off-state voltage as a function of junction temperature; minimum values

7. Package outline

Plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)

SOT428

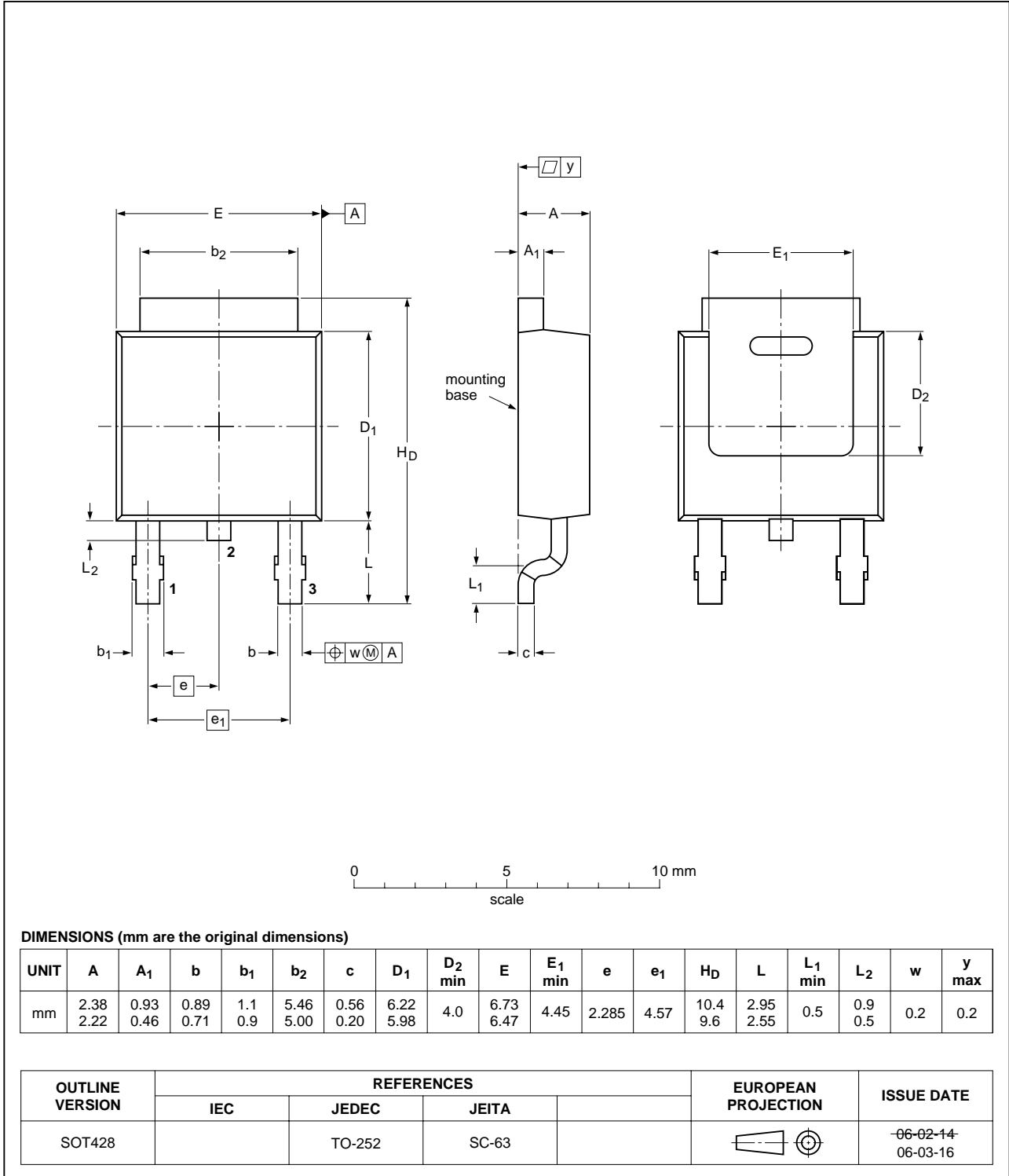
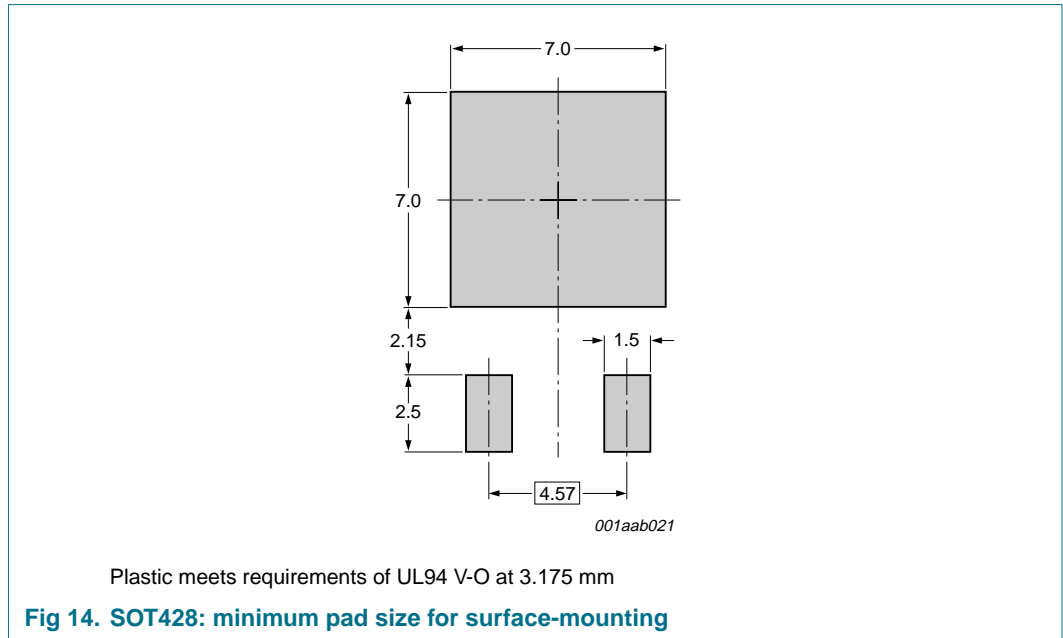


Fig 13. Package outline SOT428 (DPAK)

8. Mounting



9. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BT151S_SER_L_R_5	20061009	Product data sheet	-	BT151S_SERIES_4
Modifications:		<ul style="list-style-type: none">• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.• Legal texts have been adapted to the new company name where appropriate.• Added type numbers BT151S-500L and BT151S-650L		
BT151S_SERIES_4 (9397 750 13161)	20040609	Product specification	-	BT151S_SERIES_3
BT151S_SERIES_3	20020101	Product specification	-	BT151S_SERIES_2
BT151S_SERIES_2	19990601	Product specification	-	BT151S_SERIES_1
BT151S_SERIES_1	19970901	Product specification	-	-

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10.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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For sales office addresses, please send an email to: salesaddresses@nxp.com

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