# 74AHC1G07; 74AHCT1G07

# Buffer with open-drain output Rev. 7 — 18 November 2014

**Product data sheet** 

#### 1. **General description**

74AHC1G07 and 74AHCT1G07 are high-speed Si-gate CMOS devices. They provide a non-inverting buffer.

The output of these devices is open-drain and can be connected to other open-drain outputs to implement active-LOW wired-OR or active-HIGH wired-AND functions. For digital operation this device must have a pull-up resistor to establish a logic HIGH-level.

The AHC device has CMOS input switching levels and supply voltage range 2 V to 5.5 V.

The AHCT device has TTL input switching levels and supply voltage range 4.5 V to 5.5 V.

#### **Features and benefits** 2.

- High noise immunity
- Low power dissipation
- SOT353-1 and SOT753 package options
- ESD protection:
  - HBM JESD22-A114E: exceeds 2000 V
  - MM JESD22-A115-A: exceeds 200 V
  - CDM JESD22-C101C: exceeds 1000 V
- Specified from -40 °C to +125 °C

#### **Ordering information** 3.

#### Table 1. **Ordering information**

Type number	Package							
	Temperature range	Name	Description	Version				
74AHC1G07GW	−40 °C to +125 °C	TSSOP5	plastic thin shrink small outline package;	SOT353-1				
74AHCT1G07GW			5 leads; body width 1.25 mm					
74AHC1G07GV	−40 °C to +125 °C	SC-74A	plastic surface-mounted package; 5 leads	SOT753				
74AHCT1G07GV								



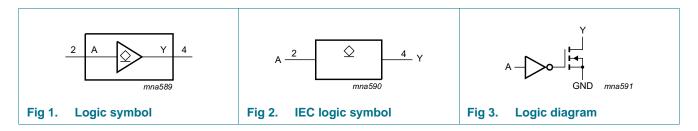
## 4. Marking

#### Table 2. Marking codes

Type number	Marking[1]
74AHC1G07GW	AS
74AHC1G07GV	A07
74AHCT1G07GW	CS
74AHCT1G07GV	C07

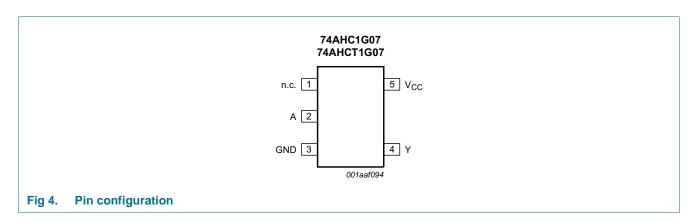
[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

## 5. Functional diagram



## 6. Pinning information

#### 6.1 Pinning



#### 6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
n.c.	1	not connected
Α	2	data input
GND	3	ground (0 V)
Υ	4	data output
V <sub>CC</sub>	5	supply voltage

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## 7. Functional description

#### Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state

Input	Output
A	Υ
L	L
Н	Z

## 8. Limiting values

#### Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>CC</sub>	supply voltage			-0.5	+7.0	V
V <sub>I</sub>	input voltage			-0.5	+7.0	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < -0.5 V		-20	-	mA
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < -0.5 V	<u>[1]</u>	-	±20	mA
Io	output current	$V_{\rm O} > -0.5 \text{ V}$		-	±25	mA
Vo	output voltage	active mode	<u>[1]</u>	-0.5	+7.0	V
		high-impedance mode	<u>[1]</u>	-0.5	+7.0	V
I <sub>CC</sub>	supply current			-	75	mA
I <sub>GND</sub>	ground current			-75	-	mA
T <sub>stg</sub>	storage temperature			-65	+150	°C
P <sub>tot</sub>	total power dissipation	$T_{amb} = -40  ^{\circ}\text{C} \text{ to } +125  ^{\circ}\text{C}$	[2]	-	250	mW

<sup>[1]</sup> The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

# 9. Recommended operating conditions

#### Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions 74AHC1G07				74	Unit		
			Min	Тур	Max	Min	Тур	Max	
V <sub>CC</sub>	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
VI	input voltage		0	-	5.5	0	-	5.5	V
Vo	output voltage	active mode	0	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V
		high-impedance mode	0	-	6.0	0	-	6.0	V
T <sub>amb</sub>	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV input transition rise		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	-	-	100	-	-	-	ns/V
	and fall rate	$V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$	-	-	20	-	-	20	ns/V

<sup>[2]</sup> For both TSSOP5 and SC-74A packages: above 87.5 °C the value of Ptot derates linearly with 4.0 mW/K.

## 10. Static characteristics

Table 7. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C		-40 °C	to +85 °C	-40 °C t	o +125 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	
For type	74AHC1G07							-		1
V <sub>IH</sub>	HIGH-level	V <sub>CC</sub> = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
	input voltage	V <sub>CC</sub> = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V <sub>CC</sub> = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
V <sub>IL</sub>	LOW-level	V <sub>CC</sub> = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
	input voltage	V <sub>CC</sub> = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V <sub>CC</sub> = 5.5 V	-	-	1.65	-	1.65	-	1.65	V
V <sub>OL</sub>	LOW-level	$V_I = V_{IH}$ or $V_{IL}$								
	output voltage	$I_O = 50 \mu A; V_{CC} = 2.0 \text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 50 \mu A; V_{CC} = 3.0 \text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 50 \mu A; V_{CC} = 4.5 V$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 4.0 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.36	-	0.44	-	0.55	V
		$I_O = 8.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	-	0.36	-	0.44	-	0.55	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μА
l <sub>OZ</sub>	OFF-state output current	$V_I = V_{IH}$ or $V_{IL}$ ; $V_O = V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$	-	-	±0.25		±2.5		±10.0	μА
I <sub>CC</sub>	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5 \text{ V}$	-	-	1.0	-	10	-	20	μΑ
Cı	input capacitance		-	1.5	10	-	10	-	10	pF
For type	74AHCT1G07					I			1	
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
V <sub>OL</sub>	LOW-level	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5 \text{ V}$								
	output voltage	I <sub>O</sub> = 50 μA	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 8.0 mA	-	-	0.36	-	0.44	-	0.55	V
l <sub>l</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μА
I <sub>OZ</sub>	OFF-state output current	$V_I = V_{IH}$ or $V_{IL}$ ; $V_O = V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$	-	-	±0.25		±2.5		±10.0	μА
I <sub>CC</sub>	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5 \text{ V}$	-	-	1.0	-	10	-	20	μА
Δl <sub>CC</sub>	additional supply current	per input pin; V <sub>I</sub> = 3.4 V;	-	-	1.35	-	1.5	-	1.5	mA
Cı	input capacitance		-	1.5	10	-	10	-	10	pF

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## 11. Dynamic characteristics

#### Table 8. Dynamic characteristics

GND = 0 V;  $t_r = t_f = \le 3.0$  ns. For test circuit see <u>Figure 6</u>.

Symbol Parameter		Conditions			25 °C		-40 °C	to +85 °C	-40 °C t	o +125 °C	Unit
				Min	Тур	Max	Min	Max	Min	Max	
For type	74AHC1G07		•							1	
t <sub>PZL</sub>	OFF-state	A to Y; see Figure 5									
	to LOW propagation	$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	[1]								
	delay	C <sub>L</sub> = 15 pF		-	3.5	5.6	1.0	6.3	1.0	7.0	ns
		C <sub>L</sub> = 50 pF		-	5.0	8.0	1.0	9.0	1.0	10.0	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	[2]								
		C <sub>L</sub> = 15 pF		-	2.5	3.9	1.0	4.6	1.0	4.9	ns
	C <sub>L</sub> = 50 pF		-	3.6	5.5	1.0	6.5	1.0	7.0	ns	
t <sub>PLZ</sub> LOW to	A to Y; see Figure 5										
	OFF-state propagation	$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	[1]								
	delay	C <sub>L</sub> = 15 pF		-	5.8	7.9	1.0	8.4	1.0	8.9	ns
		C <sub>L</sub> = 50 pF		-	8.3	11.5	1.0	12.0	1.0	12.5	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	[2]								
		C <sub>L</sub> = 15 pF		-	4.2	5.1	1.0	5.6	1.0	6.1	ns
		C <sub>L</sub> = 50 pF		-	6.0	7.5	1.0	8.0	1.0	8.5	ns
$C_{PD}$	power dissipation capacitance	per buffer; $C_L = 50 \text{ pF}$ ; $f = 1 \text{ MHz}$ ; $V_I = \text{GND to } V_{CC}$	[3]	-	5	-	-	-	-	-	pF
For type	74AHCT1G07	<u>'</u>								1	
t <sub>PZL</sub>	OFF-state	A to Y; see Figure 5									
	to LOW propagation	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	[2]								
	delay	C <sub>L</sub> = 15 pF		-	2.8	4.6	1.0	5.3	1.0	5.6	ns
		C <sub>L</sub> = 50 pF		-	4.0	6.5	1.0	7.5	1.0	8.0	ns
t <sub>PLZ</sub>	LOW to	A to Y; see Figure 5									
	OFF-state	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	[2]								
	propagation delay	C <sub>L</sub> = 15 pF		-	3.9	5.6	1.0	6.1	1.0	6.6	ns
		C <sub>L</sub> = 50 pF		-	5.5	8.0	1.0	8.5	1.0	9.0	ns
C <sub>PD</sub>	power dissipation capacitance	per buffer; $C_L = 50 \text{ pF}$ ; $f = 1 \text{ MHz}$ ; $V_I = \text{GND to } V_{CC}$		-	6.5	-	-	-	-	-	pF

<sup>[1]</sup> Typical values are measured at  $V_{CC}$  = 3.3 V.

 $P_D = C_{PD} \times V_{CC}{}^2 \times f_i + \sum{(C_L \times V_{CC}{}^2 \times f_o)}$  where:

 $f_i$  = input frequency in MHz;

 $f_o$  = output frequency in MHz;

C<sub>L</sub> = output load capacitance in pF;

 $V_{CC}$  = supply voltage in Volts

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<sup>[2]</sup> Typical values are measured at  $V_{CC}$  = 5.0 V.

<sup>[3]</sup>  $C_{PD}$  is used to determine the dynamic power dissipation  $P_D$  ( $\mu W$ ).

### 12. Waveforms

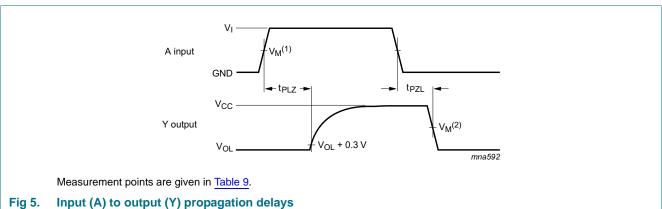
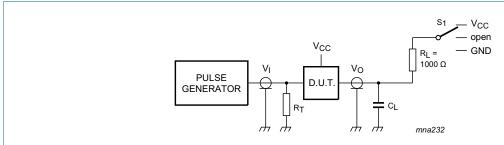


Table 9. **Measurement point** 

Туре	Input	Input					
	V <sub>I</sub>	V <sub>M</sub> <sup>(1)</sup>	V <sub>M</sub> <sup>(2)</sup>				
74AHC1G07	GND to V <sub>CC</sub>	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$				
74AHCT1G07	GND to 3.0 V	1.5 V	$0.5 \times V_{CC}$				



Test data is given in Table 8. Definitions for test circuit:

C<sub>L</sub> = Load capacitance including jig and probe capacitance.

 $R_T$  = Termination resistance should be equal to output impedance  $Z_0$  of the pulse generator.

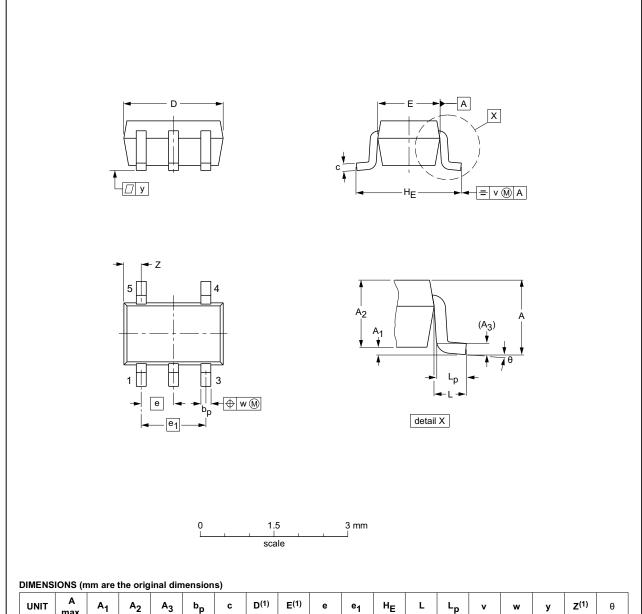
For  $t_{PLZ}$ ,  $t_{PZL}$ ,  $S_1 = V_{CC}$ 

Test circuit for measuring switching times Fig 6.

## 13. Package outline

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm

SOT353-1



UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	С	D <sup>(1)</sup>	E(1)	е	e <sub>1</sub>	HE	L	Lp	v	w	у	Z <sup>(1)</sup>	θ
mm	1.1	0.1 0	1.0 0.8	0.15	0.30 0.15	0.25 0.08	2.25 1.85	1.35 1.15	0.65	1.3	2.25 2.0	0.425	0.46 0.21	0.3	0.1	0.1	0.60 0.15	7° 0°

#### Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE		EUROPEAN	ISSUE DATE				
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE	
SOT353-1		MO-203	SC-88A			<del>00-09-01</del> 03-02-19	

Fig 7. Package outline SOT353-1 (TSSOP5)

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#### **SOT753** Plastic surface-mounted package; 5 leads В Α X = v (M) A $H_{\mathsf{E}}$ 5 Q 3 detail X **→ | w (M) B** е scale **DIMENSIONS** (mm are the original dimensions) UNIT D Q Α С Ε $A_1$ bp е ΗE $L_{\mathbf{p}}$ w у 0.100 0.40 3.0 2.5 3.1 2.7 1.1 0.26 1.7 0.6 0.33 0.95 0.1 0.013 0.25 0.9 0.10 1.3 0.23 0.2 REFERENCES **EUROPEAN** OUTLINE ISSUE DATE VERSION JEDEC **PROJECTION** IEC **JEITA**

Fig 8. Package outline SOT753 (SC-74A)

74AHC\_AHCT1G07

SC-74A

02-04-16

06-03-16

SOT753

## 14. Abbreviations

#### Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

# 15. Revision history

#### Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT1G07 v.7	20141118	Product data sheet	-	74AHC_AHCT1G07 v.6
Modifications:	Section 4: table note added.			
74AHC_AHCT1G07 v.6	20070607	Product data sheet	-	74AHC_AHCT1G07 v.5
Modifications:	<ul> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> </ul>			
	<ul> <li>Legal texts have</li> </ul>	ave been adapted to the new c	ompany name wher	e appropriate.
	Package SOT	Γ353 changed to SOT353-1 in	Section 3 and Section	on 13.
	Quick referen	ce data and Soldering sections	s removed.	
74AHC_AHCT1G07 v.5	20021002	Product specification	-	74AHC_AHCT1G07 v.4
74AHC_AHCT1G07 v.4	20020606	Product specification	-	74AHC_AHCT1G07 v.3
74AHC_AHCT1G07 v.3	20020221	Product specification	-	74AHC_AHCT1G07 v.2
74AHC_AHCT1G07 v.2	20010209	Product specification	-	74AHC_AHCT1G07 v.1
74AHC_AHCT1G07 v.1	20000502	Product specification	-	-

## 16. Legal information

#### 16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions"
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <a href="http://www.nxp.com">http://www.nxp.com</a>.

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#### **Buffer with open-drain output**

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