BLF178P

Power LDMOS transistor

Rev. 3 — 1 September 2015

AMPLEON

Product data sheet

1. Product profile

1.1 General description

A 1200 W LDMOS power transistor for broadcast applications and industrial applications in the HF to 110 MHz band.

Table 1. Application information

Test signal	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
CW	108	50	1000	26	75
pulsed RF	108	50	1200	28.5	75

1.2 Features and benefits

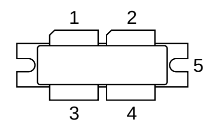
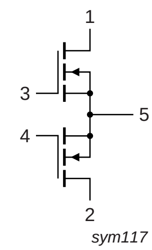
- Typical pulsed performance at frequency of 108 MHz, a supply voltage of 50 V and an I_{Dq} of 40 mA, a t_p of 100 μs with δ of 20 %:
  - Output power = 1200 W
  - Power gain = 28.5 dB
  - Efficiency = 75 %
- Easy power control
- Integrated ESD protection
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (10 MHz to 110 MHz)
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- Industrial, scientific and medical applications
- FM transmitter applications

2. Pinning information

Table 2. Pinning

Pin	Description		Simplified outline	Graphic symbol
1	drain1			
2	drain2			
3	gate1			
4	gate2			
5	source	[1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF178P	-	flanged balanced LDMOST ceramic package; 2 mounting holes; 4 leads	SOT539A

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	110	V
V_{GS}	gate-source voltage		–0.5	+11	V
I_D	drain current		-	88	A
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		-	225	°C

5. Thermal characteristics

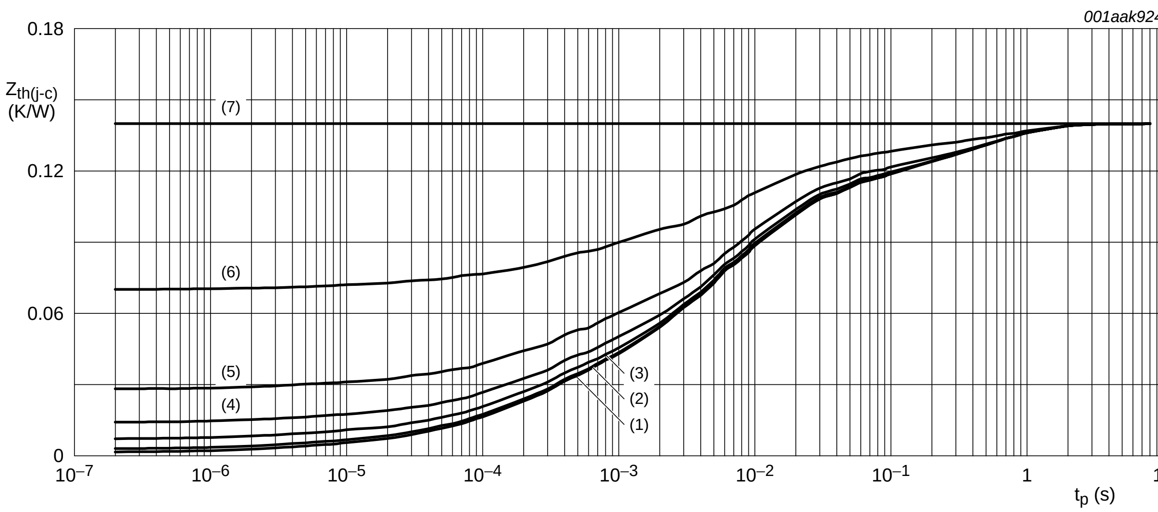
Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_j = 150 °C	[1][2]	0.14	K/W
$Z_{th(j-c)}$	transient thermal impedance from junction to case	T_j = 150 °C; t_p = 100 μs; δ = 20 %	[3]	0.04	K/W

[1] T_j is the junction temperature.

[2] $R_{th(j-c)}$ is measured under RF conditions.

[3] See Figure 1.



(1) δ = 1 %
(2) δ = 2 %
(3) δ = 5 %
(4) δ = 10 %
(5) δ = 20 %
(6) δ = 50 %
(7) δ = 100 % (DC)

Fig 1. Transient thermal impedance from junction to case as a function of pulse duration

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 2.5 mA	110	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 500 mA	1.25	1.7	2.25	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 50 V; I_D = 20 mA	0.8	1.3	1.8	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 50 V	-	-	2.8	μA

Table 6. DC characteristics *...continued*

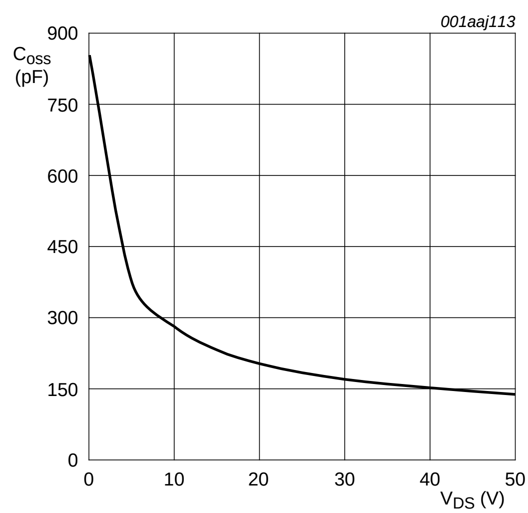
T_j = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	58	71	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	280	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)}$ + 3.75 V; I_D = 16.66 A	-	0.07	-	Ω
C_{rs}	feedback capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz	-	3	-	pF
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz	-	403	-	pF
C_{oss}	output capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz	-	138	-	pF

Table 7. RF characteristics

Test signal: pulsed RF; t_p = 100 μs; δ = 20 %; f = 108 MHz; RF performance at V_{DS} = 50 V; I_{Dq} = 40 mA; T_{case} = 25 °C; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	P_L = 1200 W	27	28.5	31	dB
RL_{in}	input return loss	P_L = 1200 W	-	−16	−12	dB
η_D	drain efficiency	P_L = 1200 W	71	75	-	%



V_{GS} = 0 V; f = 1 MHz.

Fig 2. Output capacitance as a function of drain-source voltage; typical values per section

6.1 Ruggedness in class-AB operation

The BLF178P is capable of withstanding a load mismatch corresponding to VSWR = 13 : 1 through all phases under the following conditions: V_{DS} = 50 V; I_{Dq} = 40 mA; P_L = 1200 W pulsed; f = 108 MHz.

7. Test information

7.1 Impedance information

Table 8. Typical impedance
Simulated Z_S and Z_L test circuit impedances.

f MHz	Z_S Ω	Z_L Ω
108	3.91 – j3.56	3.59 – j1.73

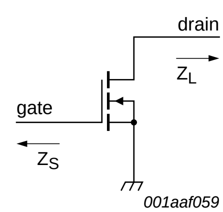
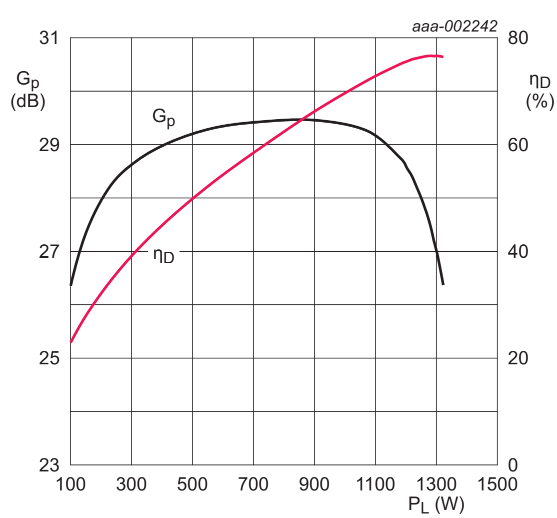


Fig 3. Definition of transistor impedance

7.2 RF performance

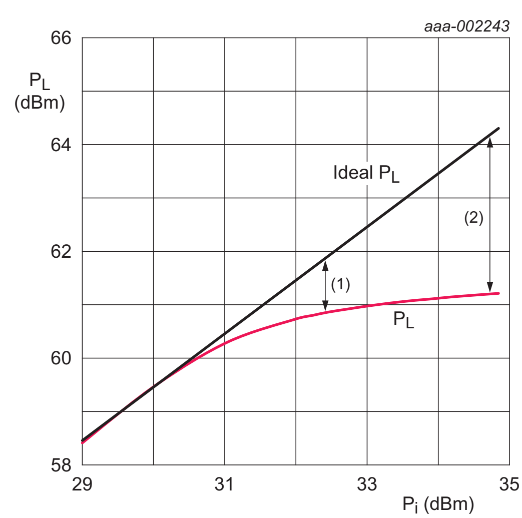
The following figures are measured in a class-AB production test circuit.

7.2.1 1-Tone CW pulsed



V_{DS} = 50 V; I_{Dq} = 40 mA; f = 108 MHz; t_p = 100 μs; δ = 20 %.

Fig 4. Power gain and drain efficiency as function of output power; typical values

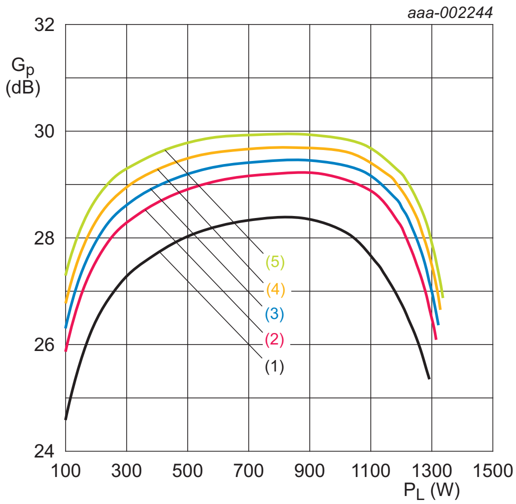


V_{DS} = 50 V; I_{Dq} = 40 mA; f = 108 MHz; t_p = 100 μs; δ = 20 %.

(1) $P_{L(1dB)}$ = 60.8 dBm (1214 W)

(2) $P_{L(3dB)}$ = 61.2 dBm (1319 W)

Fig 5. Output power as a function of input power; typical values



V_{DS} = 50 V; f = 108 MHz; t_p = 100 μs; δ = 20 %.

(1) I_{Dq} = 0 mA

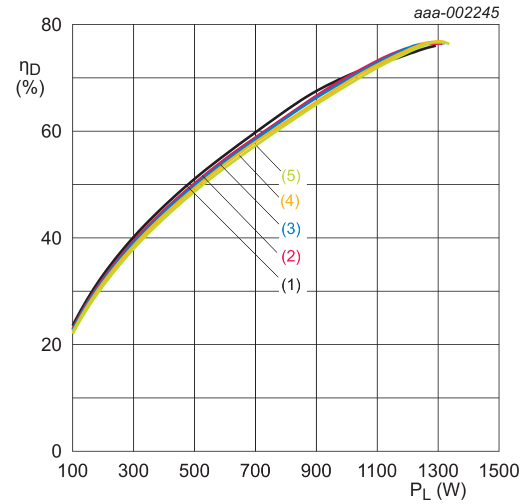
(2) I_{Dq} = 20 mA

(3) I_{Dq} = 40 mA

(4) I_{Dq} = 80 mA

(5) I_{Dq} = 160 mA

Fig 6. Power gain as a function of output power; typical values



V_{DS} = 50 V; f = 108 MHz; t_p = 100 μs; δ = 20 %.

(1) I_{Dq} = 0 mA

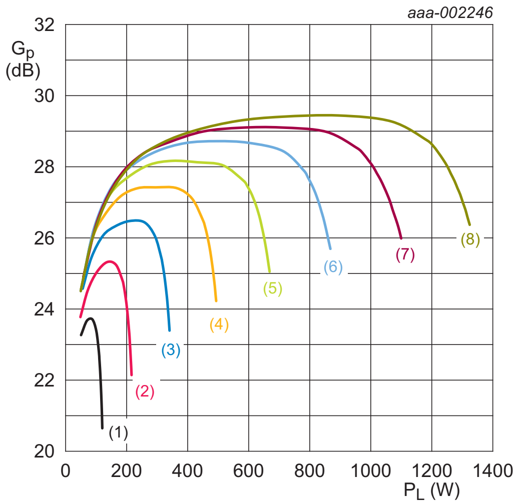
(2) I_{Dq} = 20 mA

(3) I_{Dq} = 40 mA

(4) I_{Dq} = 80 mA

(5) I_{Dq} = 160 mA

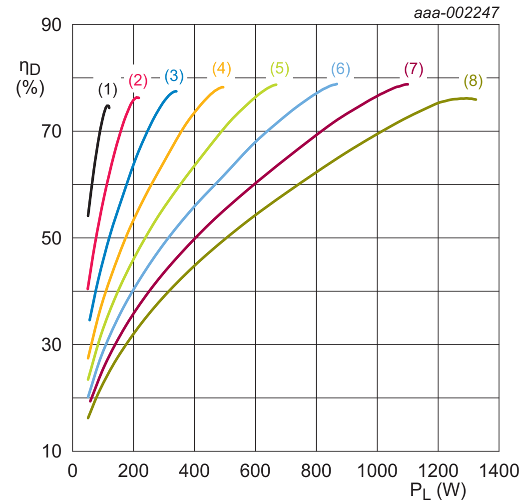
Fig 7. Drain efficiency as a function of output power; typical values



I_{Dq} = 40 mA; f = 108 MHz; t_p = 100 μs; δ = 20 %.

(1) V_{DS} = 15 V
(2) V_{DS} = 20 V
(3) V_{DS} = 25 V
(4) V_{DS} = 30 V
(5) V_{DS} = 35 V
(6) V_{DS} = 40 V
(7) V_{DS} = 45 V
(8) V_{DS} = 50 V

Fig 8. Power gain as a function of output power; typical values

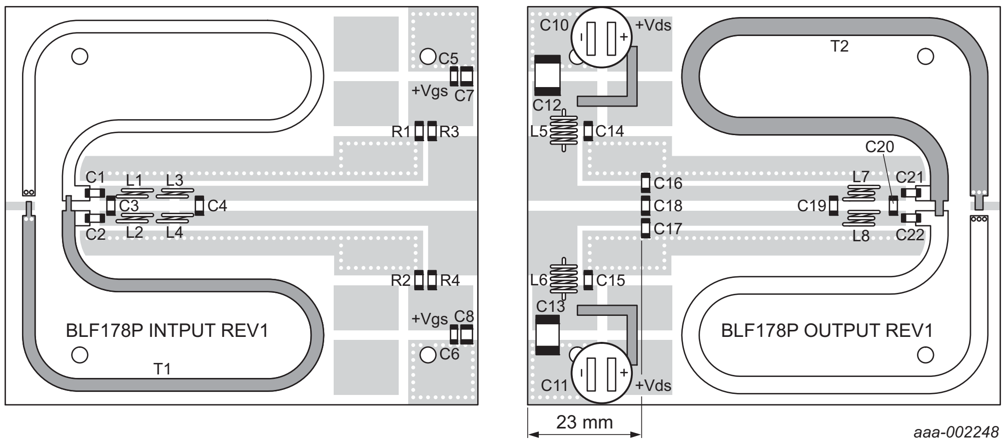


I_{Dq} = 40 mA; f = 108 MHz; t_p = 100 μs; δ = 20 %.

(1) V_{DS} = 15 V
(2) V_{DS} = 20 V
(3) V_{DS} = 25 V
(4) V_{DS} = 30 V
(5) V_{DS} = 35 V
(6) V_{DS} = 40 V
(7) V_{DS} = 45 V
(8) V_{DS} = 50 V

Fig 9. Drain efficiency as a function of output power; typical values

7.3 Test circuit



Printed-Circuit Board (PCB): RF 35; ε_r = 3.5; thickness = 0.76 mm; thickness copper plating = 35 μm.

See Table 9 for a list of components.

Fig 10. Component layout for class-AB production test circuit

Table 9. List of components

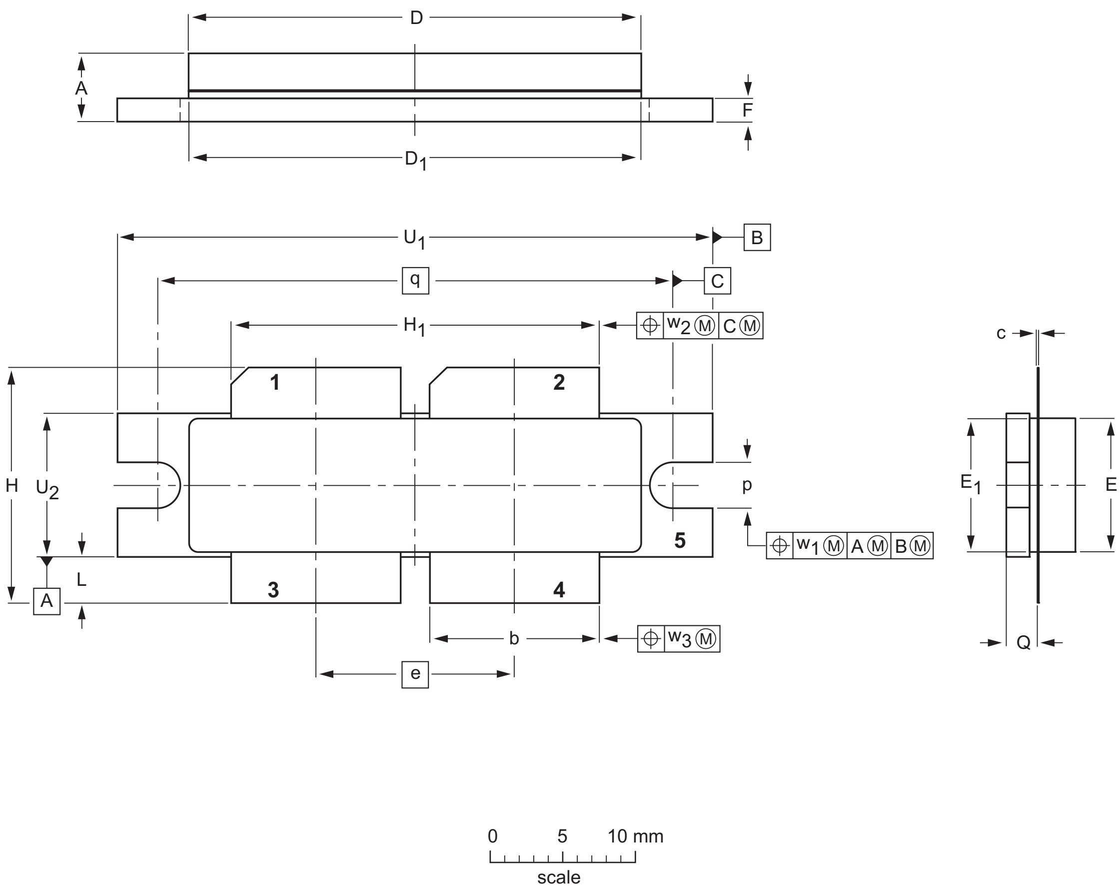
For test circuit see Figure 10.

Component	Description	Value		Remarks
C1, C2, C5, C6, C14, C15, C21, C22	multilayer ceramic chip capacitor	1 nF	[1]	
C3	multilayer ceramic chip capacitor	82 pF	[1]	
C4	multilayer ceramic chip capacitor	240 pF	[1]	
C7, C8	multilayer ceramic chip capacitor	4.7 μF; 50 V		
C10, C11	electrolytic capacitor	1000 μF; 63 V		
C12, C13	multilayer ceramic chip capacitor	4.7 μF; 100 V		
C16, C17	multilayer ceramic chip capacitor	120 pF	[1]	
C18	multilayer ceramic chip capacitor	82 pF	[1]	
C19	multilayer ceramic chip capacitor	110 pF	[1]	
C20	multilayer ceramic chip capacitor	56 pF	[1]	
L1, L2, L3, L4	1.5 turn 0.8 mm copper wire	D = 3 mm; length = 2 mm		
L5, L6	5 turn 0.8 mm copper wire	D = 3 mm; length = 4.5 mm		
L7, L8	2.5 turn 0.8 mm copper wire	D = 3 mm; length = 3 mm		
R1, R2	SMD resistor	100 Ω		Philips 1206
R3, R4	SMD resistor	9.1 Ω		Philips 1206
T1	semi rigid coax	25 Ω; 160 mm		UT-090C-25
T2	semi rigid coax	25 Ω; 160 mm		UT-141C-25

[1] American Technical Ceramics type 800B or capacitor of same quality.

8. Package outline

Flanged balanced ceramic package; 2 mounting holes; 4 leads **SOT539A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H_1	L	p	Q	q	U_1	U_2	w_1	w_2	w_3
mm	4.7 4.2	11.81 11.56	0.18 0.10	31.55 30.94	31.52 30.96	13.72	9.50 9.30	9.53 9.27	1.75 1.50	17.12 16.10	25.53 25.27	3.48 2.97	3.30 3.05	2.26 2.01	35.56	41.28 41.02	10.29 10.03	0.25	0.51	0.25
inches	0.185 0.165	0.465 0.455	0.007 0.004	1.242 1.218	1.241 1.219	0.540	0.374 0.366	0.375 0.365	0.069 0.059	0.674 0.634	1.005 0.995	0.137 0.117	0.130 0.120	0.089 0.079	1.400	1.625 1.615	0.405 0.395	0.010	0.020	0.010

Note
1. millimeter dimensions are derived from the original inch dimensions.
2. recommended screw pitch dimension of 1.52 inch (38.6 mm) based on M3 screw.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT539A						~~10-02-02~~ 12-05-02

Fig 11. Package outline SOT539A

9. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

10. Abbreviations

Table 10. Abbreviations

Acronym	Description
CW	Continuous Wave
DC	Direct Current
ESD	ElectroStatic Discharge
FM	Frequency Modulation
HF	High Frequency
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
LDMOST	Laterally Diffused Metal-Oxide Semiconductor Transistor
RF	Radio Frequency
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio

11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF178P#3	20150901	Product data sheet	-	BLF178P v.2
Modifications:	• The format of this document has been redesigned to comply with the new identity guidelines of Ampleon. • Legal texts have been adapted to the new company name where appropriate.			
BLF178P v.2	20120216	Product data sheet	-	BLF178P v.1
BLF178P v.1	20110405	Objective data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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14. Contents

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