PCF8576C

Universal LCD driver for low multiplex rates

Rev. 13 — 16 December 2013 **Product data sheet**

1. General description

The PCF8576C is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD)[1] with low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 40 segments and can easily be cascaded for larger LCD applications. The PCF8576C is compatible with most microcontrollers and communicates via the two-line bidirectional I^2C-bus. Communication overheads are minimized by a display RAM with auto-incremented addressing and by hardware subaddressing.

For a selection of NXP LCD segment drivers, see Table 24 on page 52.

2. Features and benefits

- Single-chip LCD controller and driver
- 40 segment drives:
  - Up to twenty 7-segment alphanumeric characters
  - Up to ten 14-segment alphanumeric characters
  - Any graphics of up to 160 elements
- Versatile blinking modes
- No external components required (even in multiple device applications)
- Selectable backplane drive configuration: static, 2, 3, or 4 backplane multiplexing
- Selectable display bias configuration: static, $\frac{1}{2}$, or $\frac{1}{3}$
- Internal LCD bias generation with voltage-follower buffers
- 40 $\times$ 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Wide logic LCD supply range:
  - From 2 V for low-threshold LCDs
  - Up to 6 V for high-threshold twisted nematic LCDs
- Low power consumption
- May be cascaded for large LCD applications (up to 2560 elements possible)
- No external components required
- Separate or combined LCD and logic supplies
- Optimized pinning for plane wiring in both single and multiple PCF8576C applications
- Power-saving mode for extremely low power consumption in battery-operated and telephone applications

1. The definition of the abbreviations and acronyms used in this data sheet can be found in Section 20.

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCF8576CHL/1	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
PCF8576CT/1	VSO56	plastic very small outline package, 56 leads	SOT190-1
PCF8576CU/2/F2	bare die	bare die; 56 bumps; 3.2 × 2.92 × 0.40 mm	PCF8576CU/2
PCF8576CU/F1	bare die	wire bond die; 56 bonding pads; 3.2 × 2.92 × 0.38 mm	PCF8576CU

3.1 Ordering options

Table 2. Ordering options

Product type number	Sales item (12NC)	Orderable part number	IC revision	Delivery form
PCF8576CHL/1	935290305118	PCF8576CHL/1,118	1	tape and reel, 13 inch
	935290305157	PCF8576CHL/1,157	1	tray pack
PCF8576CT/1	935278818518	PCF8576CT/1,518	1	tape and reel, 13 inch, dry pack
PCF8576CU/2/F2	935261851026	PCF8576CU/2/F2,026	1	chips in tray
PCF8576CU/F1	935208600026	PCF8576CU/F1,026	1	chips in tray

4. Marking

Table 3. Marking codes

Product type number	Marking code
PCF8576CHL/1	PCF8576CHL
PCF8576CT/1	PCF8576CT
PCF8576CU/2/F2	PC8576C-2
PCF8576CU/F1	PC8576C-1

5. Block diagram

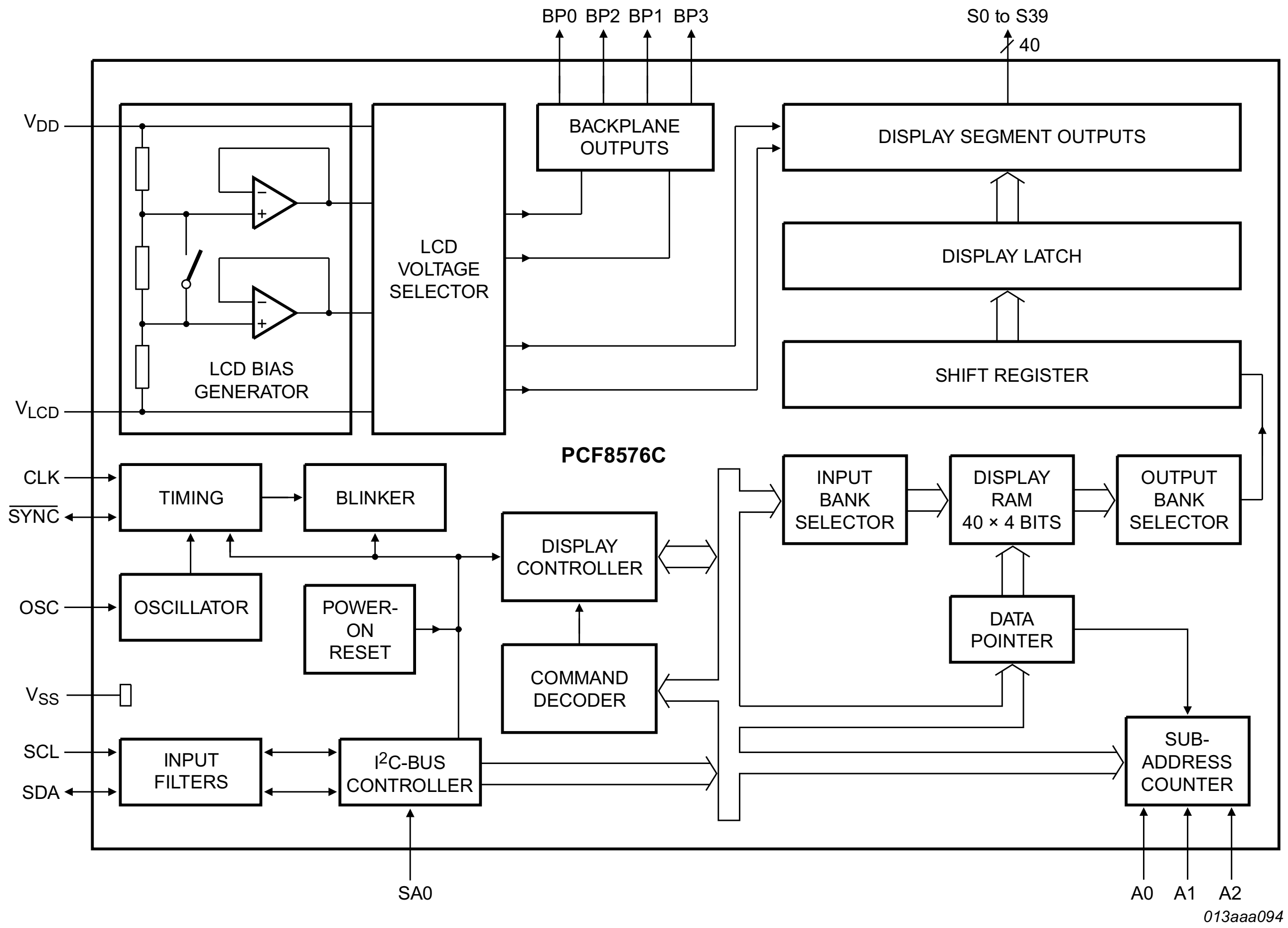
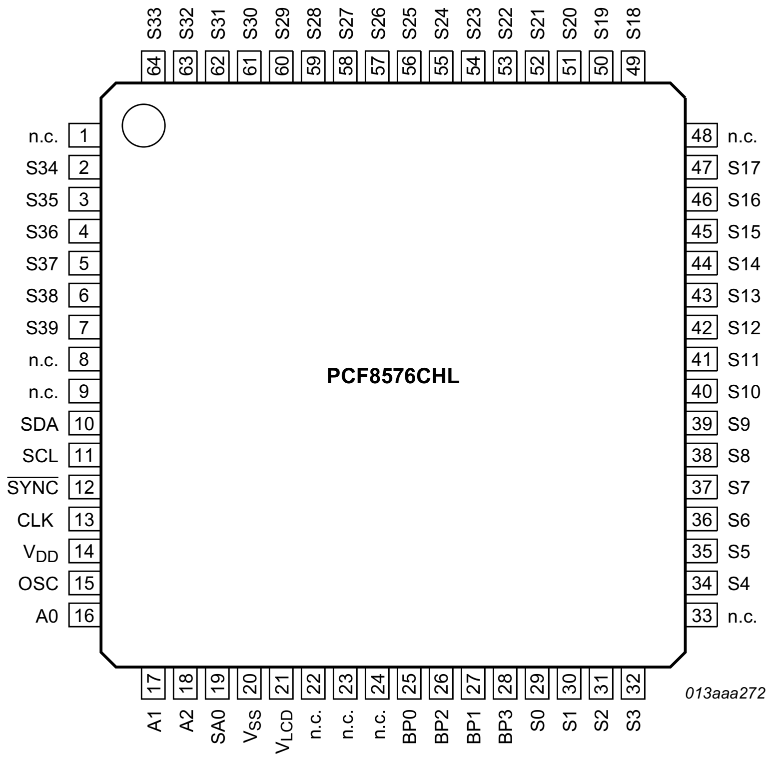


Fig 1. Block diagram of PCF8576C

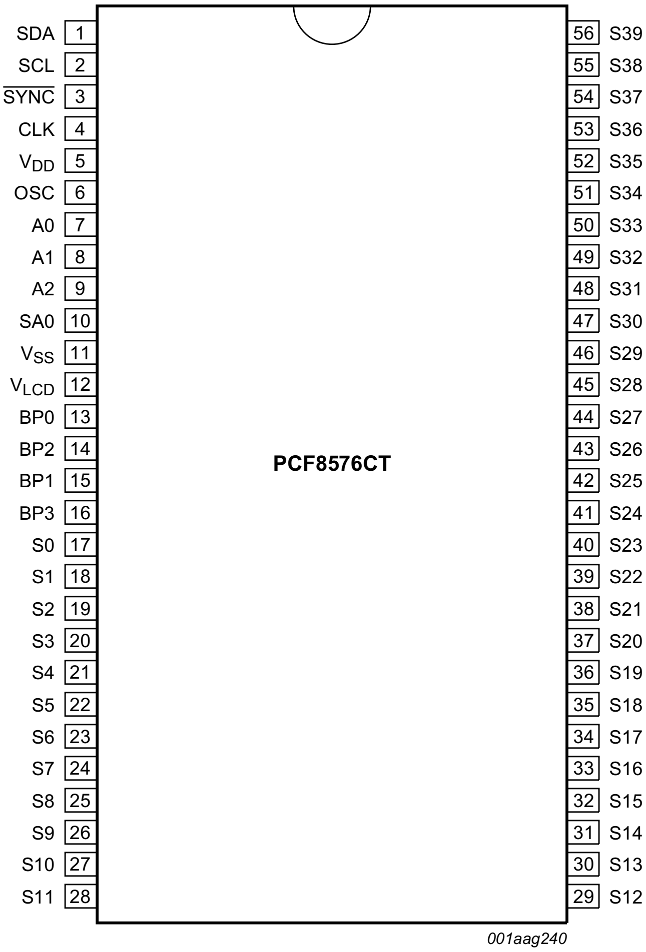
6. Pinning information

6.1 Pinning



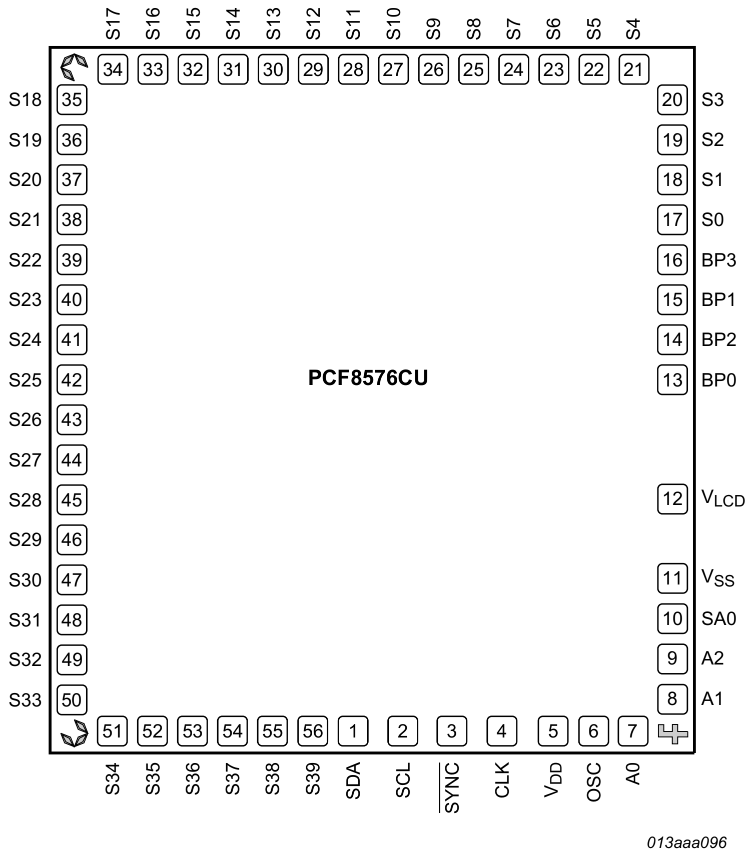
Top view. For mechanical details, see Figure 33.

Fig 2. Pin configuration for LQFP64 (PCF8576CHL/1)



Top view. For mechanical details, see Figure 34.

Fig 3. Pin configuration for VSO56 (PCF8576CT/1)



Viewed from pin side. For mechanical details, see Figure 36 and Figure 35.

Fig 4. Pin locations of PCF8576CU/F1 and PCF8576CU/2/F2

6.2 Pin description

Table 4. Pin description

Input or input/output pins must always be at a defined level (V_{SS} or V_{DD}) unless otherwise specified.

Symbol	Pin				Description
	LQFP64 (PCF8576CHL)	VSO56 (PCF8576CT)	PCF8576CU	Type	
SDA	10	1	1	input/output	I^2C-bus serial data input and output
SCL	11	2	2	input	I^2C-bus serial clock input
$\overline{SYNC}$	12	3	3	input/output	cascade synchronization input and output
CLK	13	4	4	input/output	external clock input/output
V_{DD}	14	5	5[1]	supply	supply voltage
OSC	15	6	6	input	internal oscillator enable input
A0 to A2	16 to 18	7 to 9	7 to 9	input	subaddress inputs
SA0	19	10	10	input	I^2C-bus address input; bit 0
V_{SS}	20	11	11	supply	ground supply voltage
V_{LCD}	21	12	12	supply	LCD supply voltage
BP0, BP2, BP1, BP3	25 to 28	13 to 16	13 to 16	output	LCD backplane outputs
S0 to S39	2 to 7, 29 to 32, 34 to 47, 49 to 64	17 to 56	17 to 56	output	LCD segment outputs
n.c.	1, 8, 9, 22 to 24, 33, 48	-	-	-	not connected; do not connect and do not use as feed through

[1] The substrate (rear side of the die) is connected to V_{DD} and should be electrically isolated.

7. Functional description

The PCF8576C is a versatile peripheral device designed to interface between any microcontroller to a wide variety of LCD segment or dot matrix displays (see Figure 5). It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 40 segments.

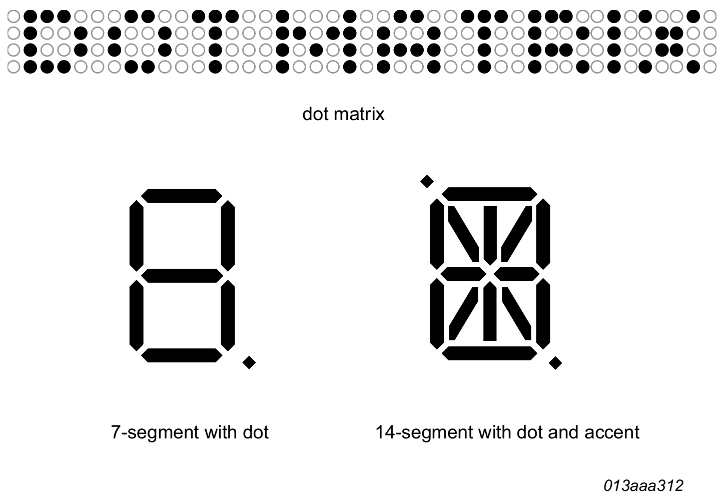


Fig 5. Example of displays suitable for PCF8576C

The possible display configurations of the PCF8576C depend on the number of active backplane outputs required. A selection of display configurations is shown in Table 5. All of these configurations can be implemented in the typical system shown in Figure 6.

Table 5. Selection of possible display configurations

Number of				
Backplanes	Icons	Digits/Characters		Dot matrix/ Elements
		7-segment	14-segment	
4	160	20	10	160 dots (4 × 40)
3	120	15	7	120 dots (3 × 40)
2	80	10	5	80 dots (2 × 40)
1	40	5	2	40 dots (1 × 40)

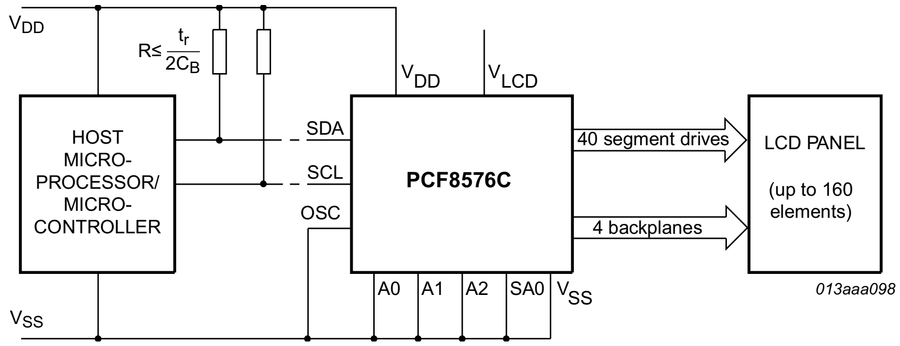


Fig 6. Typical system configuration

The host microprocessor or microcontroller maintains the 2-line I²C-bus communication channel with the PCF8576C.

Biasing voltages for the multiplexed LCD waveforms are generated internally, removing the need for an external bias generator. The internal oscillator is selected by connecting pin OSC to V_{SS}. The only other connections required to complete the system are the power supplies (pins V_{DD}, V_{SS}, and V_{LCD}) and the LCD panel selected for the application.

7.1 Power-On-Reset (POR)

At power-on the PCF8576C resets to the following starting conditions:

- All backplane and segment outputs are set to V_{DD}
- The selected drive mode is 1:4 multiplex with $\frac{1}{3}$ bias
- Blinking is switched off
- Input and output bank selectors are reset
- The I²C-bus interface is initialized
- The data pointer and the subaddress counter are cleared

Remark: Do not transfer data on the I²C-bus for at least 1 ms after a power-on to allow the reset action to complete.

7.2 LCD bias generator

The full-scale LCD voltage (V_{oper}) is obtained from $V_{DD} - V_{LCD}$. The LCD voltage may be temperature compensated externally through the V_{LCD} supply to pin V_{LCD}.

Fractional LCD biasing voltages are obtained from an internal voltage divider comprising three series resistors connected between V_{DD} and V_{LCD}. The center resistor can be switched out of the circuit to provide a $\frac{1}{2}$ bias voltage level for the 1:2 multiplex configuration.

7.3 LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD in accordance with the selected LCD drive configuration. The operation of the voltage selector is controlled by the mode-set command from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of V_{LCD} and the resulting discrimination ratios (D) are given in Table 6.

Discrimination is a term which is defined as the ratio of the on and off RMS voltage across a segment. It can be thought of as a measurement of contrast.

Table 6. Biasing characteristics

LCD drive mode	Number of:		LCD bias configuration	$\frac{V_{off(RMS)}}{V_{LCD}}$	$\frac{V_{on(RMS)}}{V_{LCD}}$	$D = \frac{V_{on(RMS)}}{V_{off(RMS)}}$
	Backplanes	Levels				
static	1	2	static	0	1	∞
1:2 multiplex	2	3	½	0.354	0.791	2.236
1:2 multiplex	2	4	⅓	0.333	0.745	2.236
1:3 multiplex	3	4	⅓	0.333	0.638	1.915
1:4 multiplex	4	4	⅓	0.333	0.577	1.732

A practical value for V_{LCD} is determined by equating $V_{off(RMS)}$ with a defined LCD threshold voltage (V_{th}), typically when the LCD exhibits approximately 10 % contrast. In the static drive mode, a suitable choice is $V_{LCD} > 3V_{th}$.

Multiplex drive modes of 1:3 and 1:4 with ½ bias are possible but the discrimination and hence the contrast ratios are smaller.

Bias is calculated by $\frac{1}{1 + a}$, where the values for a are

a = 1 for ½ bias

a = 2 for ⅓ bias

The RMS on-state voltage ($V_{on(RMS)}$) for the LCD is calculated with Equation 1:

$$V_{on(RMS)} = V_{LCD}\sqrt{\frac{a^2 + 2a + n}{n \times (1 + a)^2}} \quad (1)$$

where the values for n are

n = 1 for static drive mode

n = 2 for 1:2 multiplex drive mode

n = 3 for 1:3 multiplex drive mode

n = 4 for 1:4 multiplex drive mode

The RMS off-state voltage ($V_{off(RMS)}$) for the LCD is calculated with Equation 2:

$$V_{off(RMS)} = V_{LCD}\sqrt{\frac{a^2 - 2a + n}{n \times (1 + a)^2}} \quad (2)$$

Discrimination is the ratio of $V_{on(RMS)}$ to $V_{off(RMS)}$ and is determined from Equation 3:

$$D = \frac{V_{on(RMS)}}{V_{off(RMS)}} = \sqrt{\frac{(a+1)^2 + (n-1)}{(a-1)^2 + (n-1)}} \quad (3)$$

Using Equation 3, the discrimination for an LCD drive mode of 1:3 multiplex with ½ bias is $\sqrt{3} = 1.732$ and the discrimination for an LCD drive mode of 1:4 multiplex with ½ bias is $\frac{\sqrt{21}}{3} = 1.528$.

The advantage of these LCD drive modes is a reduction of the LCD full scale voltage V_{LCD} as follows:

- 1:3 multiplex (½ bias): $V_{LCD} = \sqrt{6} \times V_{off(RMS)} = 2.449V_{off(RMS)}$
- 1:4 multiplex (½ bias): $V_{LCD} = \left[\frac{(4 \times \sqrt{3})}{3}\right] = 2.309V_{off(RMS)}$

These compare with $V_{LCD} = 3V_{off(RMS)}$ when ⅓ bias is used.

V_{LCD} is sometimes referred as the LCD operating voltage.

7.3.1 Electro-optical performance

Suitable values for $V_{on(RMS)}$ and $V_{off(RMS)}$ are dependent on the LCD liquid used. The RMS voltage, at which a pixel will be switched on or off, determine the transmissibility of the pixel.

For any given liquid, there are two threshold values defined. One point is at 10 % relative transmission (at $V_{th(off)}$) and the other at 90 % relative transmission (at $V_{th(on)}$), see Figure 7. For a good contrast performance, the following rules should be followed:

$$V_{on(RMS)} \geq V_{th(on)} \quad (4)$$

$$V_{off(RMS)} \leq V_{th(off)} \quad (5)$$

$V_{on(RMS)}$ and $V_{off(RMS)}$ are properties of the display driver and are affected by the selection of a (see Equation 1), n (see Equation 3), and the V_{LCD} voltage.

$V_{th(off)}$ and $V_{th(on)}$ are properties of the LCD liquid and can be provided by the module manufacturer. $V_{th(off)}$ is sometimes named V_{th}. $V_{th(on)}$ is sometimes named saturation voltage V_{sat}.

It is important to match the module properties to those of the driver in order to achieve optimum performance.

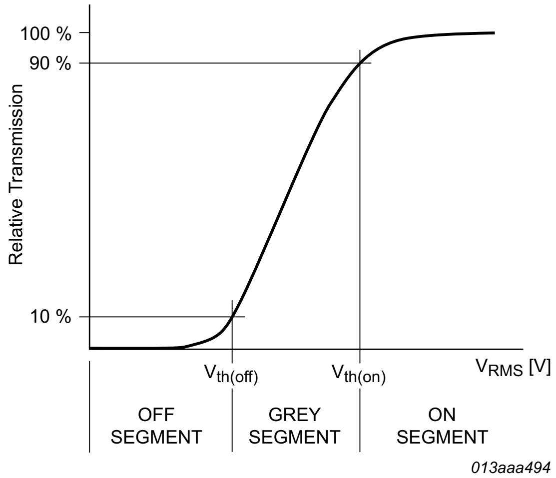
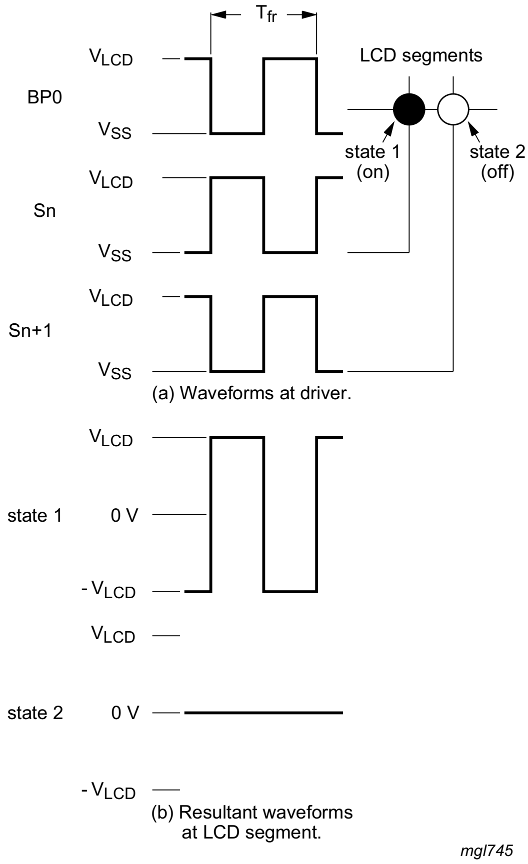


Fig 7. Electro-optical characteristic: relative transmission curve of the liquid

7.4 LCD drive mode waveforms

7.4.1 Static drive mode

The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and segment drive waveforms for this mode are shown in Figure 8.



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = V_{LCD}$.

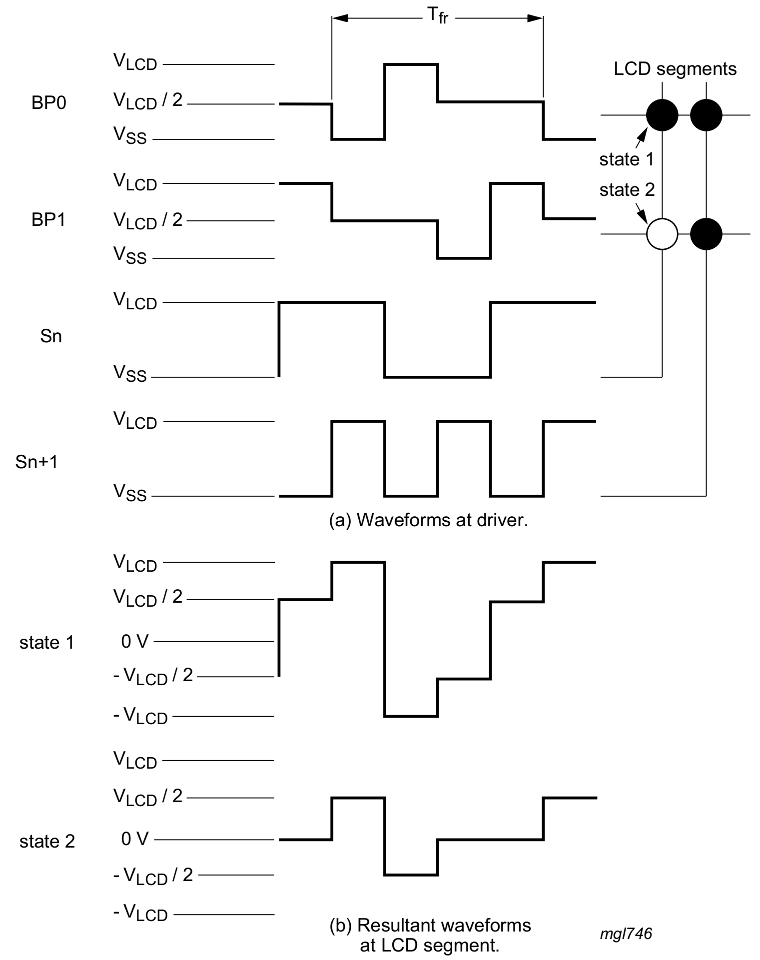
$V_{state2}(t) = V_{Sn+1}(t) - V_{BP0}(t)$.

$V_{off(RMS)} = 0$ V.

Fig 8. Static drive mode waveforms

7.4.2 1:2 Multiplex drive mode

When two backplanes are provided in the LCD, the 1:2 multiplex mode applies. The PCF8576C allows the use of ½ bias or ⅓ bias (see Figure 9 and Figure 10).



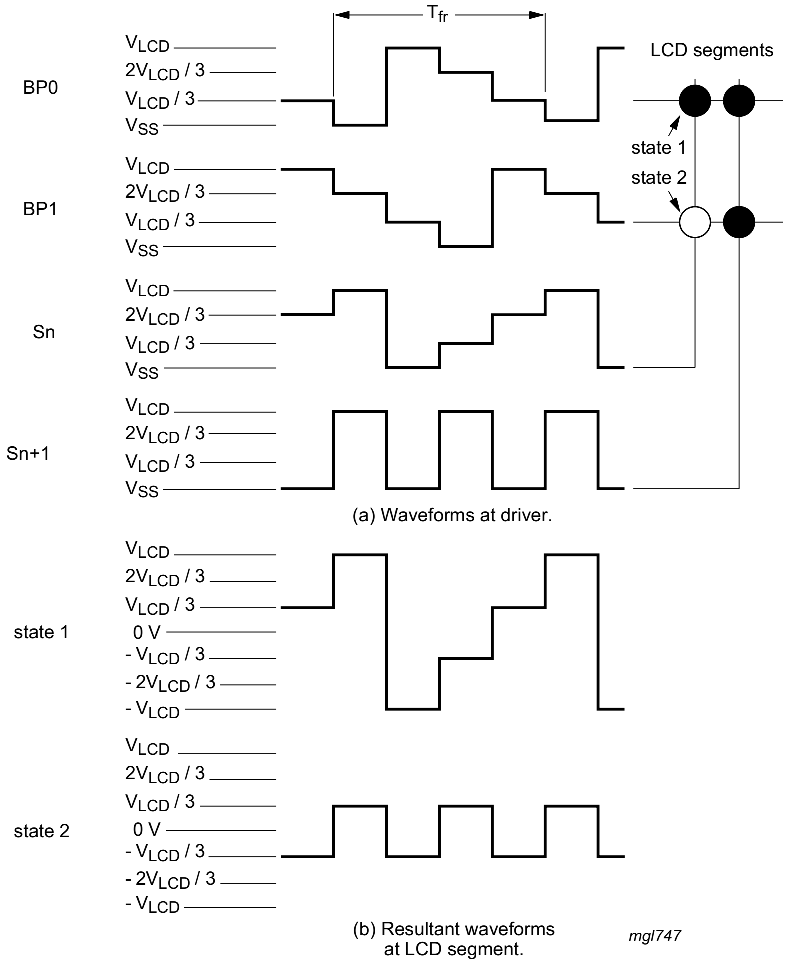
$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.791V_{LCD}$.

$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.354V_{LCD}$

Fig 9. Waveforms for the 1:2 multiplex drive mode with ½ bias



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.745V_{LCD}$

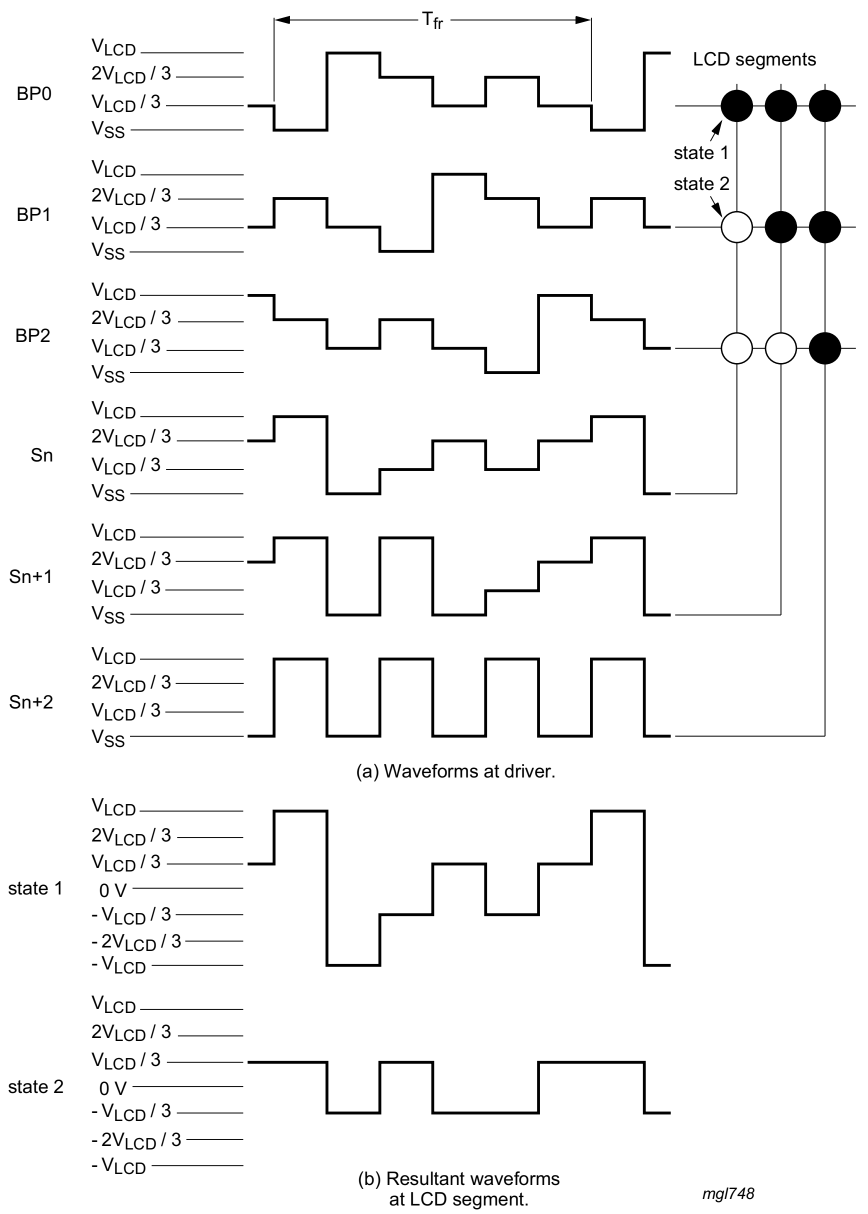
$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$

$V_{off(RMS)} = 0.333V_{LCD}$.

Fig 10. Waveforms for the 1:2 multiplex drive mode with 1⁄3 bias

7.4.3 1:3 Multiplex drive mode

When three backplanes are provided in the LCD, the 1:3 multiplex drive mode applies as shown in Figure 11.



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.638V_{LCD}$.

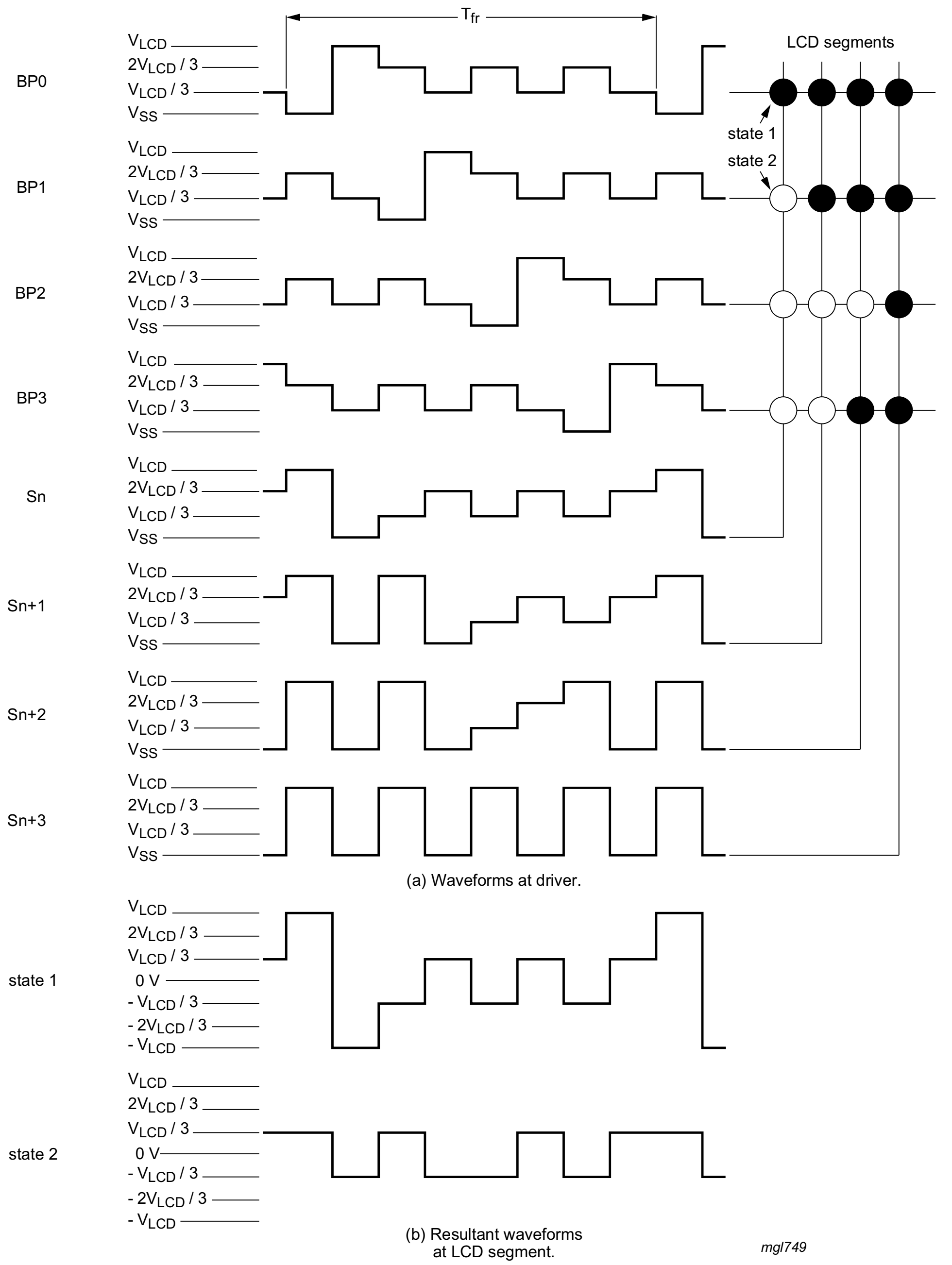
$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.333V_{LCD}$.

Fig 11. Waveforms for the 1:3 multiplex drive mode with ⅓ bias

7.4.4 1:4 multiplex drive mode

When four backplanes are provided in the LCD, the 1:4 multiplex drive mode applies, as shown in Figure 12.



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.577V_{LCD}$.

$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.333V_{LCD}$.

Fig 12. Waveforms for the 1:4 multiplex mode with 1/3 bias

7.5 Oscillator

The internal logic and the LCD drive signals of the PCF8576C are timed by the frequency f_{clk}, which equals either the built-in oscillator frequency f_{osc} or the external clock frequency $f_{clk(ext)}$.

The clock frequency (f_{clk}) determines the LCD frame frequency (f_{fr}) and the maximum rate for data reception from the I^{2}C-bus. To allow I^{2}C-bus transmissions at their maximum data rate of 100 kHz, f_{clk} should be chosen to be above 125 kHz.

7.5.1 Internal clock

The internal oscillator is enabled by connecting pin OSC to pin V_{SS}. In this case, the output from pin CLK is the clock signal for any cascaded PCF8576C in the system.

7.5.2 External clock

Connecting pin OSC to V_{DD} enables an external clock source. Pin CLK then becomes the external clock input.

Remark: A clock signal must always be supplied to the device. Removing the clock, freezes the LCD in a DC state, which is not suitable for the liquid crystal.

7.6 Timing

The timing of the PCF8576C sequences the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the synchronization signal ($\overline{SYNC}$) maintains the correct timing relationship between the PCF8576Cs in the system. The timing also generates the LCD frame frequency which is derived as an integer division of the clock frequency (see Table 7). The frame frequency is set by the mode-set command (see Table 10) when an internal clock is used or by the frequency applied to the pin CLK when an external clock is used.

Table 7. LCD frame frequencies [1]

Power mode	Frame frequency	Nominal frame frequency (Hz)
Normal-power mode	$f_{fr} = \frac{f_{clk}}{2880}$	69 [2]
Power-saving mode	$f_{fr} = \frac{f_{clk}}{480}$	65 [3]

[1] The possible values for f_{clk} see Table 17.

[2] For f_{clk} = 200 kHz.

[3] For f_{clk} = 31 kHz.

The ratio between the clock frequency and the LCD frame frequency depends on the power mode in which the device is operating. In the power-saving mode, the reduction ratio is six times smaller; this allows the clock frequency to be reduced by a factor of six. The reduced clock frequency results in a significant reduction in power consumption.

The lower clock frequency has the disadvantage of increasing the response time when large amounts of display data are transmitted on the I^{2}C-bus. When a device is unable to process a display data byte before the next one arrives, it holds the SCL line LOW until the first display data byte is stored. This slows down the transmission rate of the I^{2}C-bus but no data loss occurs.

7.7 Display register

The display register holds the display data while the corresponding multiplex signals are generated.

7.8 Shift register

The shift register transfers display information from the display RAM to the display register while previous data is displayed.

7.9 Segment outputs

The LCD drive section includes 40 segment outputs, S0 to S39, which must be connected directly to the LCD. The segment output signals are generated based on the multiplexed backplane signals and with data residing in the display register. When less than 40 segment outputs are required, the unused segment outputs should be left open-circuit.

7.10 Backplane outputs

The LCD drive section includes four backplane outputs: BP0 to BP3. The backplane output signals are generated based on the selected LCD drive mode.

- In 1:4 multiplex drive mode: BP0 to BP3 must be connected directly to the LCD.

If less than four backplane outputs are required, the unused outputs can be left as an open-circuit.

- In 1:3 multiplex drive mode: BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities.
- In 1:2 multiplex drive mode: BP0 and BP2, BP1 and BP3 respectively carry the same signals and can also be paired to increase the drive capabilities.
- In static drive mode: the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

7.11 Display RAM

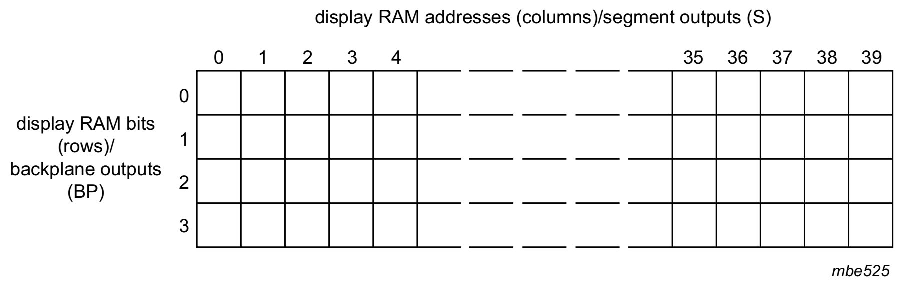
The display RAM is a static 40 × 4-bit RAM which stores LCD data.

There is a one-to-one correspondence between

- the bits in the RAM bitmap and the LCD elements
- the RAM columns and the segment outputs
- the RAM rows and the backplane outputs.

A logic 1 in the RAM bitmap indicates the on-state of the corresponding LCD element; similarly, a logic 0 indicates the off-state.

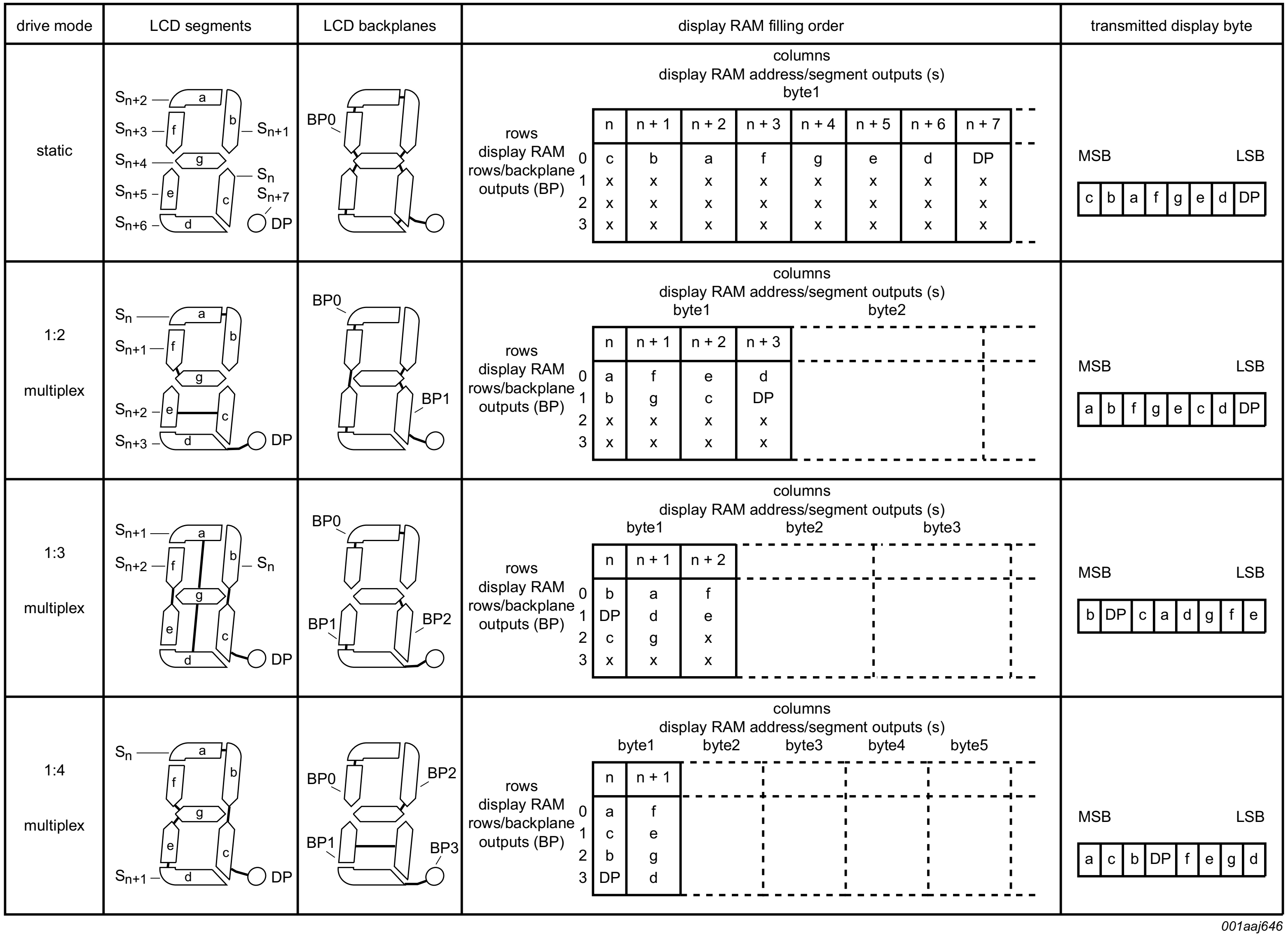
The display RAM bit map Figure 13 shows the rows 0 to 3 which correspond with the backplane outputs BP0 to BP3, and the columns 0 to 39 which correspond with the segment outputs S0 to S39. In multiplexed LCD applications the segment data of the first, second, third and fourth row of the display RAM are time-multiplexed with BP0, BP1, BP2, and BP3 respectively.



The display RAM bitmap shows the direct relationship between the display RAM column and the segment outputs; and between the bits in a RAM row and the backplane outputs.

Fig 13. Display RAM bit map

When display data is transmitted to the PCF8576C, the display bytes received are stored in the display RAM in accordance with the selected LCD drive mode. The data is stored as it arrives and does not wait for an acknowledge cycle as with the commands. Depending on the current multiplex drive mode, data is stored singularly, in pairs, triples or quadruples. To illustrate the filling order, an example of a 7-segment numeric display showing all drive modes is given in Figure 14; the RAM filling organization depicted applies equally to other LCD types.



x = data bit unchanged.

Fig 14. Relationship between LCD layout, drive mode, display RAM filling order, and display data transmitted over the I²C-bus

The following applies to Figure 14:

- In the static drive mode, the eight transmitted data bits are placed in row 0 of eight successive 4-bit RAM words.
- In the 1:2 multiplex mode, the eight transmitted data bits are placed in pairs into row 0 and 1 of four successive 4-bit RAM words.
- In the 1:3 multiplex mode, the eight bits are placed in triples into row 0, 1, and 2 to three successive 3-bit RAM words, with bit 3 of the third address left unchanged. It is not recommended to use this bit in a display because of the difficult addressing. This last bit may, if necessary, be controlled by an additional transfer to this address but care should be taken to avoid overwriting adjacent data because always full bytes are transmitted.
- In the 1:4 multiplex mode, the eight transmitted data bits are placed in quadruples into row 0, 1, 2, and 3 of two successive 4-bit RAM words.

7.12 Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the load-data-pointer command (see Table 11). After this, the data byte is stored starting at the display RAM address indicated by the data pointer (see Figure 14). Once each byte is stored, the data pointer is automatically incremented based on the selected LCD configuration.

The contents of the data pointer are incremented as follows:

- In static drive mode by eight.
- In 1:2 multiplex drive mode by four.
- In 1:3 multiplex drive mode by three.
- In 1:4 multiplex drive mode by two.

If an I^2C-bus data access terminates early, the state of the data pointer is unknown. Consequently, the data pointer must be rewritten prior to further RAM accesses.

7.13 Sub-address counter

The storage of display data is conditioned by the contents of the subaddress counter. Storage is allowed to take place only when the contents of the subaddress counter match with the hardware subaddress applied to A0, A1, and A2. The subaddress counter value is defined by the device-select command (see Table 12). If the contents of the subaddress counter and the hardware subaddress do not match, then data storage is blocked but the data pointer will be incremented as if data storage had taken place. The subaddress counter is also incremented when the data pointer overflows.

The storage arrangements described lead to extremely efficient data loading in cascaded applications. When a series of display bytes are sent to the display RAM, automatic wrap-over to the next PCF8576C occurs when the last RAM address is exceeded. Subaddressing across device boundaries is successful even if the change to the next device in the cascade occurs within a transmitted character.

7.14 Bank selector

7.14.1 Output bank selector

The output bank selector (see Table 13), selects one of the four rows per display RAM address for transfer to the display register. The actual row selected depends on the LCD drive mode in operation and on the instant in the multiplex sequence.

- In 1:4 multiplex mode: all RAM addresses of row 0 are selected, followed sequentially by the contents of row 1, row 2, and then row 3.
- In 1:3 multiplex mode: rows 0, 1, and 2 are selected sequentially.
- In 1:2 multiplex mode: rows 0 and 1 are selected.
- In the static mode: row 0 is selected.

The PCF8576C includes a RAM bank switching feature in the static and 1:2 multiplex drive modes. In the static drive mode, the bank-select command may request the contents of row 2 to be selected for display instead of the contents of row 0. In 1:2 multiplex drive mode, the contents of rows 2 and 3 may be selected instead of rows 0 and 1. This enables preparation of display information in an alternative bank and the ability to switch to it once it has been assembled.

7.14.2 Input bank selector

The input bank selector (see Table 13) loads display data into the display RAM based on the selected LCD drive configuration. Using the bank-select command, display data can be loaded in row 2 into static drive mode or in rows 2 and 3 into 1:2 multiplex drive mode. The input bank selector functions independently of the output bank selector.

7.15 Blinking

The display blinking capabilities of the PCF8576C are very versatile. The whole display can be blinked at frequencies selected by the blink-select command. The blinking frequencies are integer fractions of the clock frequency; the ratios between the clock and blinking frequencies depend on the mode in which the device is operating (see Table 8).

Table 8. Blink frequencies

Blinking mode	Normal-power mode ratio	Power-saving mode ratio	Blink frequency
off	-	-	blinking off
1	$f_{blink} = \frac{f_{clk}}{92160}$	$f_{blink} = \frac{f_{clk}}{15360}$	2 Hz
2	$f_{blink} = \frac{f_{clk}}{184320}$	$f_{blink} = \frac{f_{clk}}{30720}$	1 Hz
3	$f_{blink} = \frac{f_{clk}}{368640}$	$f_{blink} = \frac{f_{clk}}{61440}$	0.5 Hz

An additional feature is for an arbitrary selection of LCD segments to be blinked. This applies to the static and 1:2 multiplex drive modes and can be implemented without any communication overheads. Using the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blinking frequency. This mode can also be specified by the blink-select command (see Table 14).

In the 1:3 and 1:4 multiplex modes, where no alternate RAM bank is available, groups of LCD segments can be blinked by selectively changing the display RAM data at fixed time intervals.

If the entire display must be blinked at a frequency other than the nominal blink frequency, this can be done using the mode-set command to set and reset the display enable bit E at the required rate (see Table 10).

7.16 Characteristics of the I²C-bus

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial DAta line (SDA) and a Serial CLock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

7.16.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse. Changes in the data line at this time will be interpreted as a control signal. Bit transfer is illustrated in Figure 15.

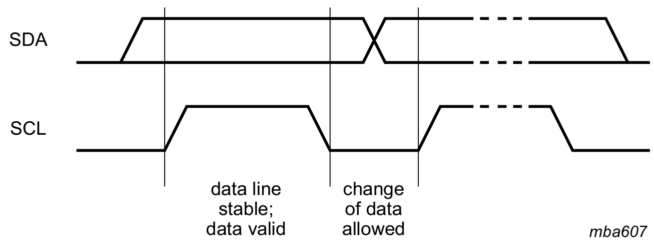


Fig 15. Bit transfer

7.16.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW change of the data line, while the clock is HIGH, is defined as the START condition (S).
A LOW-to-HIGH change of the data line, while the clock is HIGH, is defined as the STOP condition (P). The START and STOP conditions are illustrated in Figure 16.

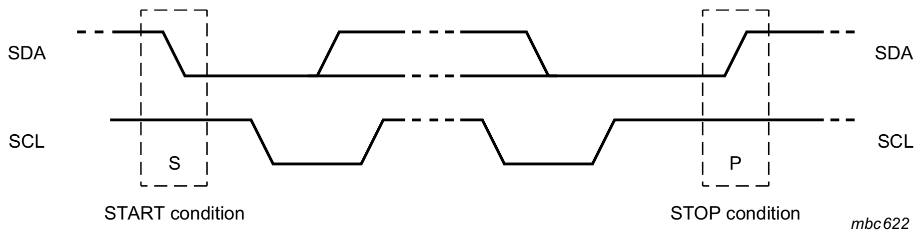


Fig 16. Definition of START and STOP conditions

7.16.3 System configuration

A device generating a message is a transmitter and a device receiving a message is the receiver. The device that controls the message is the master and the devices which are controlled by the master are the slaves. The system configuration is illustrated in Figure 17.

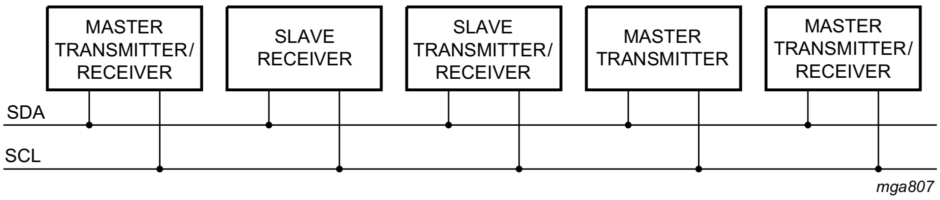


Fig 17. System configuration

7.16.4 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge cycle.

- A slave receiver, which is addressed, must generate an acknowledge after the reception of each byte.
- A master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.
- The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be considered).
- A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

Acknowledgement on the I²C-bus is illustrated in Figure 18.

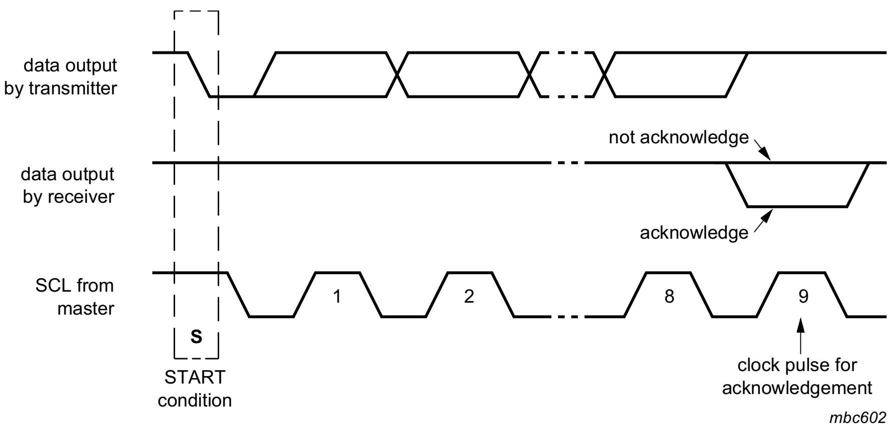


Fig 18. Acknowledgement of the I²C-bus

7.16.5 PCF8576C I^{2}C-bus controller

The PCF8576C acts as an I^{2}C-bus slave receiver. It does not initiate I^{2}C-bus transfers or transmit data to an I^{2}C-bus master receiver. The only data output from the PCF8576C are the acknowledge signals of the selected devices. Device selection depends on the I^{2}C-bus slave address, the transferred command data and the hardware subaddress.

In single device application, the hardware subaddress inputs A0, A1, and A2 are normally tied to V_{SS} which defines the hardware subaddress 0. In multiple device applications A0, A1, and A2 are tied to V_{SS} or V_{DD} using a binary coding scheme so that no two devices with a common I^{2}C-bus slave address have the same hardware subaddress.

In the power-saving mode, it is possible that the PCF8576C is not able to keep up with the highest transmission rates when large amounts of display data are transmitted. If this situation occurs, the PCF8576C forces the SCL line LOW until its internal operations are completed. This is known as the clock synchronization feature of the I^{2}C-bus and serves to slow down fast transmitters. Data loss does not occur.

7.16.6 Input filter

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

7.17 I^{2}C-bus protocol

Two I^{2}C-bus slave addresses (0111000 and 0111001) are reserved for the PCF8576C. The least significant bit of the slave address that a PCF8576C responds to is defined by the level tied at its input SA0. Therefore, two types of PCF8576C can be distinguished on the same I^{2}C-bus which allows:

- Up to 16 PCF8576Cs on the same I^{2}C-bus for very large LCD applications.
- The use of two types of LCD multiplexes on the same I^{2}C-bus.

The I^{2}C-bus protocol is shown in Figure 19. The sequence is initiated with a START condition (S) from the I^{2}C-bus master which is followed by one of the two PCF8576C slave addresses available. All PCF8576Cs with the corresponding SA0 level acknowledge in parallel with the slave address but all PCF8576Cs with the alternative SA0 level ignore the whole I^{2}C-bus transfer.

After acknowledgement, one or more command bytes follow which define the status of the addressed PCF8576Cs.

The last command byte is tagged with a cleared most significant bit, the continuation bit C. The command bytes are also acknowledged by all addressed PCF8576Cs on the bus.

After the last command byte, a series of display data bytes may follow. These display bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated and the data is directed to the intended PCF8576C device. The acknowledgement after each byte is made only by the (A0, A1, and A2) addressed PCF8576C. After the last display byte, the I^{2}C-bus master issues a STOP condition (P).

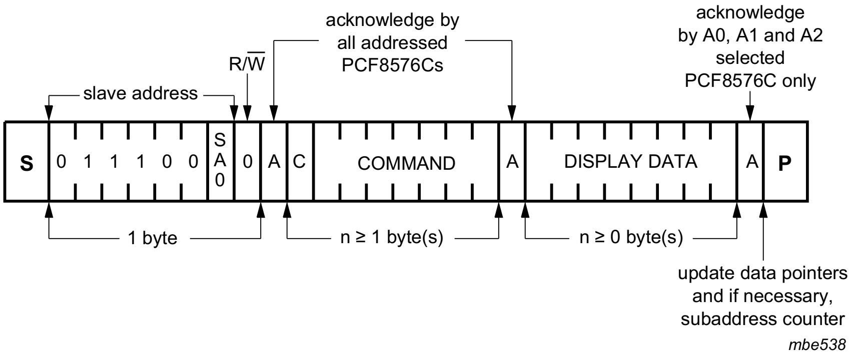
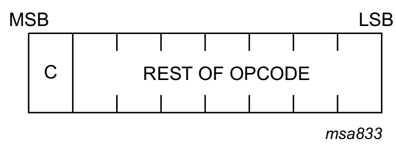


Fig 19. I²C-bus protocol

7.18 Command decoder

The command decoder identifies command bytes that arrive on the I²C-bus. All available commands carry a continuation bit C in the most significant bit position as shown in Figure 20. When this bit is set logic 1, it indicates that the next byte of the transfer to arrive will also represent a command. If this bit is set logic 0, it indicates that the command byte is the last in the transfer. Further bytes will be regarded as display data.



(1) C = 0; last command.

(2) C = 1; commands continue.

Fig 20. General format of the command byte

The five commands available to the PCF8576C are defined in Table 9.

Table 9. Definition of PCF8576C commands

Command	Operation Code								Reference
Bit	7	6	5	4	3	2	1	0	
mode-set	C	1	0	LP	E	B	M[1:0]		Section 7.18.1
load-data-pointer	C	0	P[5:0]						Section 7.18.2
device-select	C	1	1	0	0	A[2:0]			Section 7.18.3
bank-select	C	1	1	1	1	0	I	O	Section 7.18.4
blink-select	C	1	1	1	0	AB	BF[1:0]		Section 7.18.5

7.18.1 Mode-set command

Table 10. Mode-set command bit description

Bit	Symbol	Value	Description
7	C	0, 1	see Figure 20
6 to 5	-	10	fixed value
4	LP		**power dissipation** (see Table 7)
		0	normal-power mode
		1	power-saving mode
3	E		**display status**
		0	disabled[1]
		1	enabled
2	B		**LCD bias configuration**[2]
		0	$\frac{1}{3}$ bias
		1	$\frac{1}{2}$ bias
1 to 0	M[1:0]		**LCD drive mode selection**
		01	static; BP0
		10	1:2 multiplex; BP0, BP1
		11	1:3 multiplex; BP0, BP1, BP2
		00	1:4 multiplex; BP0, BP1, BP2, BP3

[1] The possibility to disable the display allows implementation of blinking under external control.

[2] Bit B is not applicable for the static LCD drive mode.

7.18.2 Load-data-pointer command

Table 11. Load-data-pointer command bit description

Bit	Symbol	Value	Description
7	C	0, 1	see Figure 20
6	-	0	fixed value
5 to 0	P[5:0]	000000 to 100111	6-bit binary value, 0 to 39; transferred to the data pointer to define one of forty display RAM addresses

7.18.3 Device-select command

Table 12. Device-select command bit description

Bit	Symbol	Value	Description
7	C	0, 1	see Figure 20
6 to 4	-	1100	fixed value
3 to 0	A[2:0]	000 to 111	3-bit binary value, 0 to 7; transferred to the subaddress counter to define one of eight hardware subaddresses

7.18.4 Bank-select command

Table 13. Bank-select command bit description

Bit	Symbol	Value	Description	
			Static	1:2 multiplex[1]
7	C	0, 1	see Figure 20	
6 to 2	-	11110	fixed value	
1	I		**input bank selection**; storage of arriving display data	
		0	RAM bit 0	RAM bits 0 and 1
		1	RAM bit 2	RAM bits 2 and 3
0	O		**output bank selection**; retrieval of LCD display data	
		0	RAM bit 0	RAM bits 0 and 1
		1	RAM bit 2	RAM bits 2 and 3

[1] The bank-select command has no effect in 1:3 and 1:4 multiplex drive modes.

7.18.5 Blink-select command

Table 14. Blink-select command bit description

Bit	Symbol	Value	Description
7	C	0, 1	see Figure 20
6 to 3	-	1110	fixed value
2	AB		**blink mode selection**
		0	normal blinking[1]
		1	alternate RAM bank blinking[2]
1 to 0	BF[1:0]		**blink frequency selection**
		00	off
		01	1
		10	2
		11	3

[1] Normal blinking is assumed when the LCD multiplex drive modes 1:3 or 1:4 are selected.

[2] Alternate RAM bank blinking does not apply in 1:3 and 1:4 multiplex drive modes.

7.19 Display controller

The display controller executes the commands identified by the command decoder. It contains the status registers of the PCF8576C and coordinates their effects. The controller is also responsible for loading display data into the display RAM as required by the filling order.

8. Internal circuitry

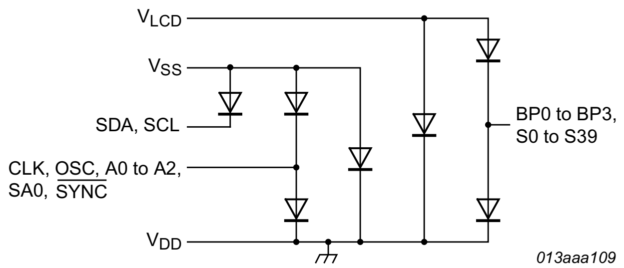


Fig 21. Device protection diagram

9. Safety notes

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

CAUTION

Static voltages across the liquid crystal display can build up when the LCD supply voltage (V_{LCD}) is on while the IC supply voltage (V_{DD}) is off, or vice versa. This may cause unwanted display artifacts. To avoid such artifacts, V_{LCD} and V_{DD} must be applied or removed together.

CAUTION

Semiconductors are light sensitive. Exposure to light sources can cause the IC to malfunction. The IC must be protected against light. The protection must be applied to all sides of the IC.

10. Limiting values

Table 15. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			–0.5	+8.0	V
V_{LCD}	LCD supply voltage		[1]	V_{DD} – 8.0	V_{DD}	V
V_I	input voltage	on each of the pins SCL, SDA, CLK, $\overline{SYNC}$, SA0, OSC and A0 to A2		–0.5	+8.0	V
V_O	output voltage	on each of the pins S0 to S39 and BP0 to BP3	[1]	–0.5	+8.0	V
I_I	input current			–20	+20	mA
I_O	output current			–25	+25	mA
I_{DD}	supply current			–50	+50	mA
I_{SS}	ground supply current			–50	+50	mA
$I_{DD(LCD)}$	LCD supply current			–50	+50	mA
P_{tot}	total power dissipation			-	400	mW
P_o	output power			-	100	mW
V_{ESD}	electrostatic discharge voltage	HBM	[2]	-	±4000	V
		CDM	[4]			
		PCF8576CHL				
		all pins		-	500	V
		corner pins		-	1000	V
		PCF8576CT				
		all pins		-	500	V
		corner pins		-	750	V
I_{lu}	latch-up current		[5]	-	150	mA
T_{stg}	storage temperature		[6]	–65	+150	°C
T_{amb}	ambient temperature	operating device		–40	+85	°C

[1] Values with respect to V_{DD}.

[2] Pass level; Human Body Model (HBM), according to Ref. 8 "JESD22-A114".

[3] Pass level; Machine Model (MM), according to Ref. 9 "JESD22-A115".

[4] Pass level; Charged-Device Model (CDM), according to Ref. 10 "JESD22-C101".

[5] Pass level; latch-up testing according to Ref. 11 "JESD78" at maximum ambient temperature ($T_{amb(max)}$).

[6] According to the store and transport requirements (see Ref. 13 "UM10569") the devices have to be stored at a temperature of +8 °C to +45 °C and a humidity of 25 % to 75 %.

11. Static characteristics

Table 16. Static characteristics

V_{DD} = 2.0 V to 6.0 V; V_{SS} = 0 V; V_{LCD} = V_{DD} − 2.0 V to V_{DD} − 6.0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
V_{DD}	supply voltage		2.0	-	6.0	V
V_{LCD}	LCD supply voltage	[1]	V_{DD} − 6.0	-	V_{DD} − 2.0	V
I_{DD}	supply current:	f_{clk} = 200 kHz [2]	-	-	120	µA
$I_{DD(lp)}$	low-power mode supply current	V_{DD} = 3.5 V; V_{LCD} = 0 V; f_{clk} = 35 kHz; A0, A1 and A2 connected to V_{SS}	-	-	60	µA
Logic						
V_{IL}	LOW-level input voltage	on pins CLK, $\overline{\text{SYNC}}$, OSC, A0 to A2 and SA0	V_{SS}	-	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage	on pins CLK, $\overline{\text{SYNC}}$, OSC, A0 to A2 and SA0	$0.7V_{DD}$	-	V_{DD}	V
V_{OL}	LOW-level output voltage	I_{OL} = 0 mA	-	-	0.05	V
V_{OH}	HIGH-level output voltage	I_{OH} = 0 mA	V_{DD} − 0.05	-	-	V
I_{OL}	LOW-level output current	output sink current; V_{OL} = 1.0 V; V_{DD} = 5.0 V; on pins CLK and $\overline{\text{SYNC}}$	1	-	-	mA
I_L	leakage current	V_I = V_{DD} or V_{SS}; on pins CLK, SCL, SDA, A0 to A2 and SA0	−1	-	+1	µA
$I_{L(OSC)}$	leakage current on pin OSC	V_I = V_{DD}	−1	-	+1	µA
I_{pd}	pull-down current	V_I = 1.0 V; V_{DD} = 5.0 V; on pins A0 to A2 and OSC	15	50	150	µA
R_{SYNC_N}	$\overline{\text{SYNC}}$ resistance		20	50	150	kΩ
V_{POR}	power-on reset voltage	[3]	-	1.0	1.6	V
C_I	input capacitance	[4]	-	-	7	pF
I²C-bus; pins SDA and SCL						
V_{IL}	LOW-level input voltage		V_{SS}	-	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	-	6.0	V
$I_{OH(CLK)}$	HIGH-level output current on pin CLK	output source current; V_{OH} = 4.0 V; V_{DD} = 5.0 V	1	-	-	mA
$I_{OL(SDA)}$	LOW-level output current on pin SDA	output sink current; V_{OL} = 0.4 V; V_{DD} = 5.0 V	3	-	-	mA

Table 16. Static characteristics *…continued*

V_{DD} = 2.0 V to 6.0 V; V_{SS} = 0 V; V_{LCD} = V_{DD} − 2.0 V to V_{DD} − 6.0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LCD outputs						
V_{BP}	voltage on pin BP	C_{bpl} = 35 nF; on pins BP0 to BP3	−20	-	+20	mV
V_S	voltage on pin S	C_{sgm} = 5 nF; on pins S0 to S39	−20	-	+20	mV
R_{BP}	resistance on pin BP	V_{LCD} = V_{DD} − 5 V; on pins BP0 to BP3 [5]	-	-	5	kΩ
R_S	resistance on pin S	V_{LCD} = V_{DD} − 5 V; on pins S0 to S39 [5]	-	-	7.5	kΩ

[1] $V_{LCD} \leq V_{DD} - 3$ V for ⅓ bias.

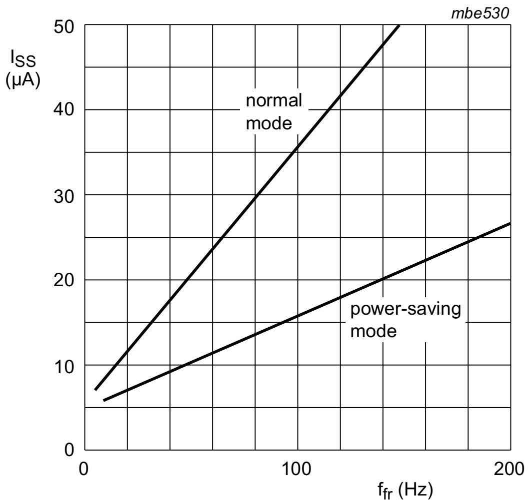
[2] LCD outputs are open-circuit; inputs at V_{SS} or V_{DD}; external clock with 50 % duty factor; I^2C-bus inactive.

[3] Resets all logic when $V_{DD} < V_{POR}$.

[4] Periodically sampled, not 100 % tested.

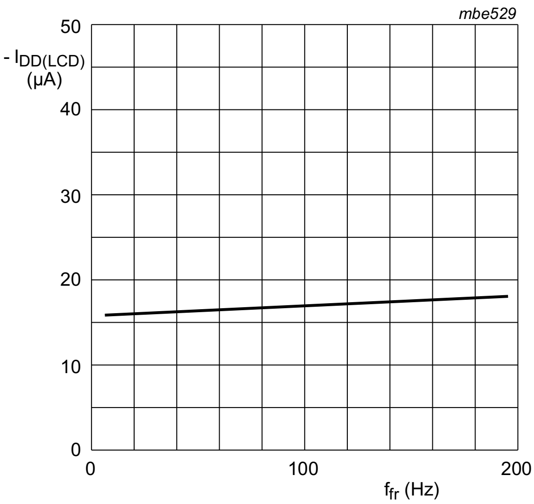
[5] Outputs measured one at a time.

11.1 Typical supply current characteristics



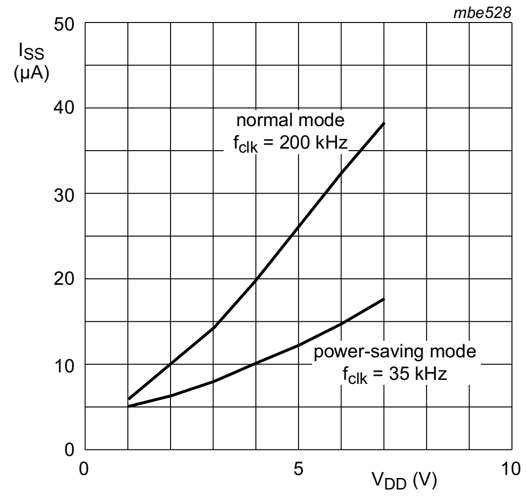
V_{DD} = 5 V; V_{LCD} = 0 V; T_{amb} = 25 °C

Fig 22. I_{SS} as a function of f_{fr}



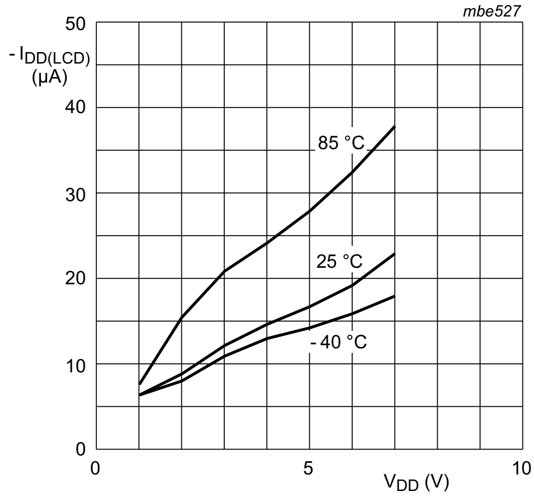
V_{DD} = 5 V; V_{LCD} = 0 V; T_{amb} = 25 °C

Fig 23. $I_{DD(LCD)}$ as a function of f_{fr}



V_{LCD} = 0 V; external clock; T_{amb} = 25 °C

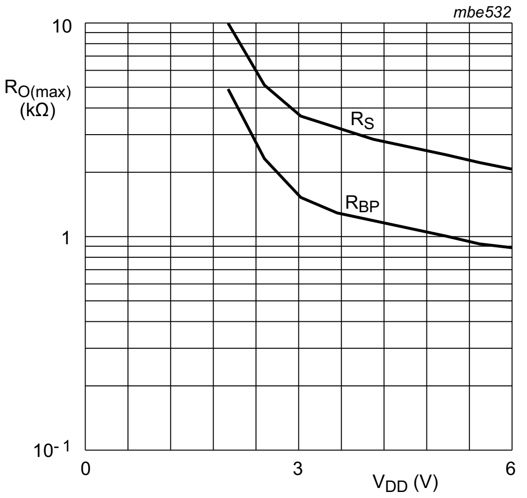
Fig 24. I_{SS} as a function of V_{DD}



V_{LCD} = 0 V; external clock; T_{amb} = 25 °C

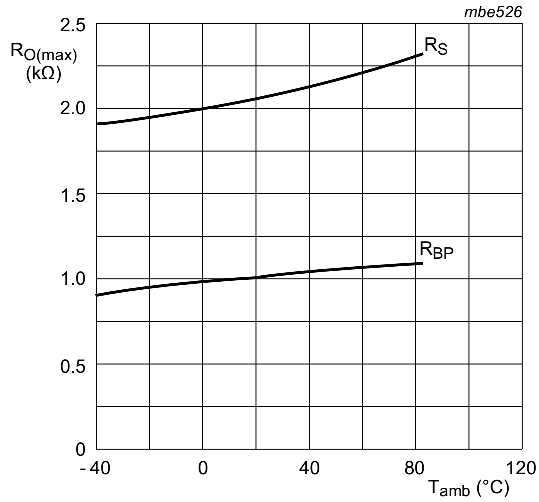
Fig 25. $I_{DD(LCD)}$ as a function of V_{DD}

11.2 Typical LCD output characteristics



V_{LCD} = 0 V; T_{amb} = 25 °C

Fig 26. $R_{O(max)}$ as a function of V_{DD}



V_{DD} = 5 V; V_{LCD} = 0 V

Fig 27. $R_{O(max)}$ as a function of T_{amb}

12. Dynamic characteristics

Table 17. Dynamic characteristics

V_{DD} = 1.8 V to 5.5 V; V_{SS} = 0 V; V_{LCD} = V_{DD} − 2.0 V to V_{DD} − 6.0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Timing characteristics: driver timing waveforms (see Figure 28)							
f_{clk}	clock frequency	normal-power mode; V_{DD} = 5 V	[1]	125	200	315	kHz
		power-saving mode; V_{DD} = 3 V		21	31	48	kHz
$t_{clk(H)}$	clock HIGH time			1	-	-	µs
$t_{clk(L)}$	clock LOW time			1	-	-	µs
$t_{PD(SYNC\_N)}$	$\overline{\text{SYNC}}$ propagation delay			-	-	400	ns
t_{SYNC_NL}	$\overline{\text{SYNC}}$ LOW time			1	-	-	µs
$t_{PD(drv)}$	driver propagation delay	V_{LCD} = 5 V		-	-	30	µs
Timing characteristics: I²C-bus (see Figure 29)			[2]				
t_{BUF}	bus free time between a STOP and START condition			4.7	-	-	µs
$t_{HD;STA}$	hold time (repeated) START condition			4.0	-	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition			4.7	-	-	µs
t_{LOW}	LOW period of the SCL clock			4.7	-	-	µs
t_{HIGH}	HIGH period of the SCL clock			4.0	-	-	µs
t_r	rise time of both SDA and SCL signals			-	-	1	µs
t_f	fall time of both SDA and SCL signals			-	-	0.3	µs
C_b	capacitive load for each bus line			-	-	400	pF
$t_{SU;DAT}$	data set-up time			250	-	-	ns
$t_{HD;DAT}$	data hold time			0	-	-	ns
$t_{SU;STO}$	set-up time for STOP condition			4.0	-	-	µs

[1] f_{clk} < 125 kHz, I²C-bus maximum transmission speed is derated.

[2] All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

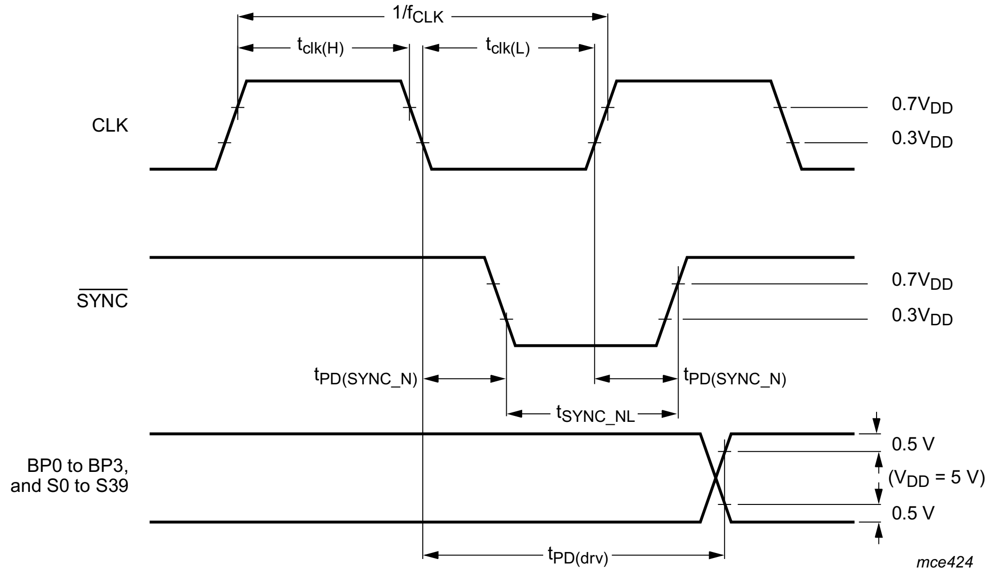


Fig 28. Driver timing waveforms

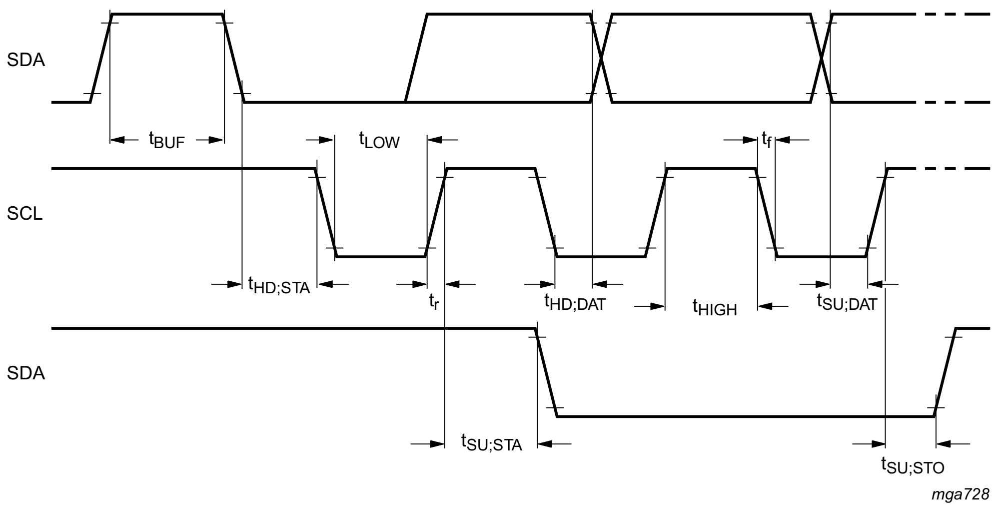


Fig 29. I²C-bus timing waveforms

13. Application information

13.1 Cascaded operation

In large display configurations, up to 16 PCF8576Cs can be recognized on the same I^2C-bus by using the 3-bit hardware subaddress (A0, A1, and A2) and the programmable I^2C-bus slave address (SA0).

Table 18. Addressing cascaded PCF8576C

Cluster	Bit SA0	Pin A2	Pin A1	Pin A0	Device
1	0	0	0	0	0
		0	0	1	1
		0	1	0	2
		0	1	1	3
		1	0	0	4
		1	0	1	5
		1	1	0	6
		1	1	1	7
2	1	0	0	0	8
		0	0	1	9
		0	1	0	10
		0	1	1	11
		1	0	0	12
		1	0	1	13
		1	1	0	14
		1	1	1	15

Cascaded PCF8576Cs are synchronized. They can share the backplane signals from one of the devices in the cascade. Such an arrangement is cost-effective in large LCD applications since the backplane outputs of only one device must be through-plated to the backplane electrodes of the display. The other PCF8576C of the cascade contribute additional segment outputs. The backplanes can either be connected together to enhance the drive capability, some can be left open-circuit (as shown in Figure 30) or just some of one and some of the other device can be taken to facilitate the layout of the display.

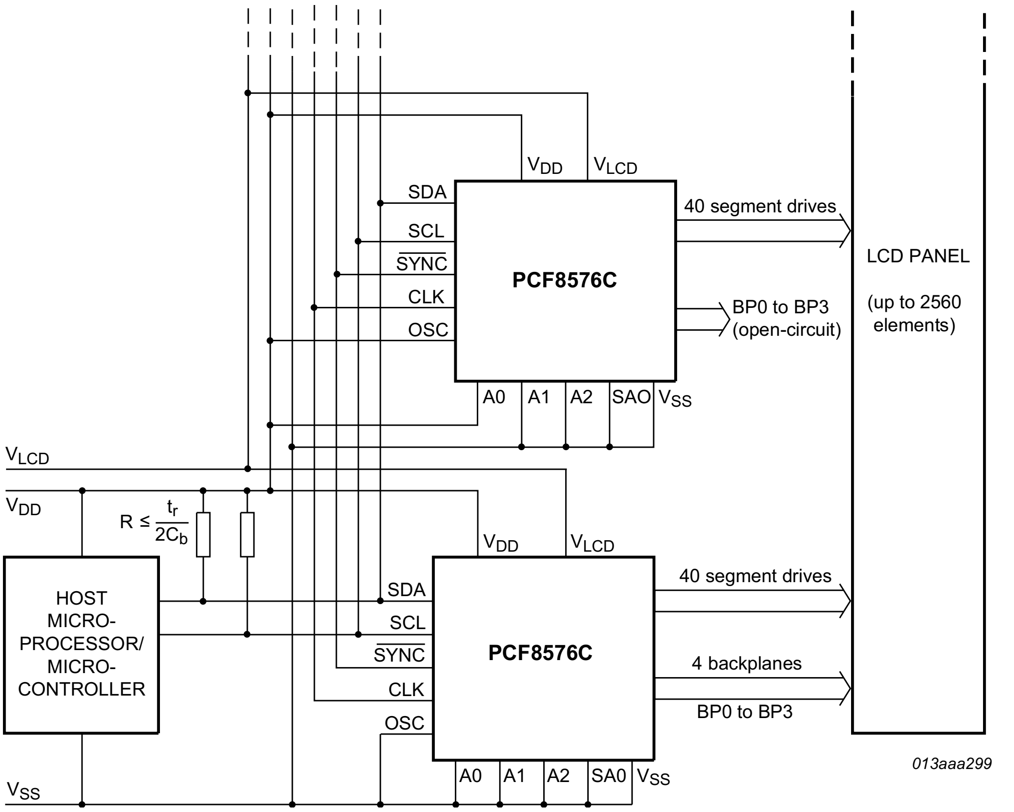
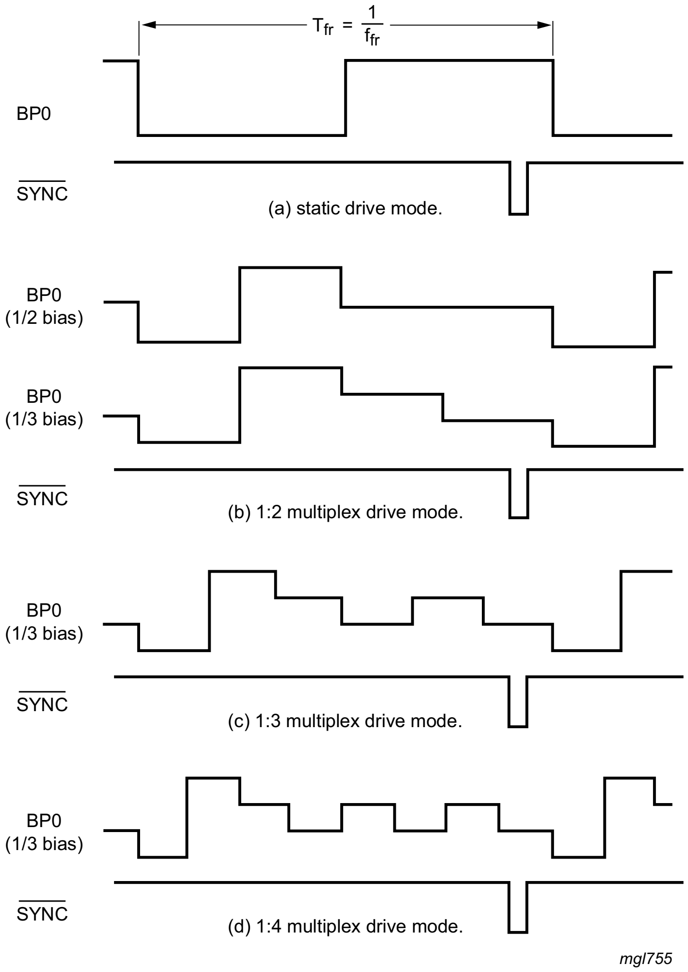


Fig 30. Cascaded PCF8576C configuration

The $\overline{SYNC}$ line is provided to maintain the correct synchronization between all cascaded PCF8576Cs. This synchronization is guaranteed after the power-on reset. The only time that $\overline{SYNC}$ is likely to be needed is if synchronization is accidentally lost (e.g. by noise in adverse electrical environments; or by the defining a multiplex mode when PCF8576Cs with differing SA0 levels are cascaded).

$\overline{SYNC}$ is organized as an input/output pin; the output selection being realized as an open-drain driver with an internal pull-up resistor. A PCF8576C asserts the $\overline{SYNC}$ line and monitors the $\overline{SYNC}$ line at all other times. If synchronization in the cascade is lost, it is restored by the first PCF8576C to assert $\overline{SYNC}$. The timing relationship between the backplane waveforms and the $\overline{SYNC}$ signal for the various drive modes of the PCF8576C are shown in Figure 31.



Excessive capacitive coupling between SCL or CLK and $\overline{\text{SYNC}}$ causes erroneous synchronization. If this is a problem, you can increase the capacitance of the $\overline{\text{SYNC}}$ line (e.g. by an external capacitor between $\overline{\text{SYNC}}$ and V_{DD}.) Degradation of the positive edge of the $\overline{\text{SYNC}}$ pulse can be countered by an external pull-up resistor.

Fig 31. Synchronization of the cascade for the various PCF8576C drive modes

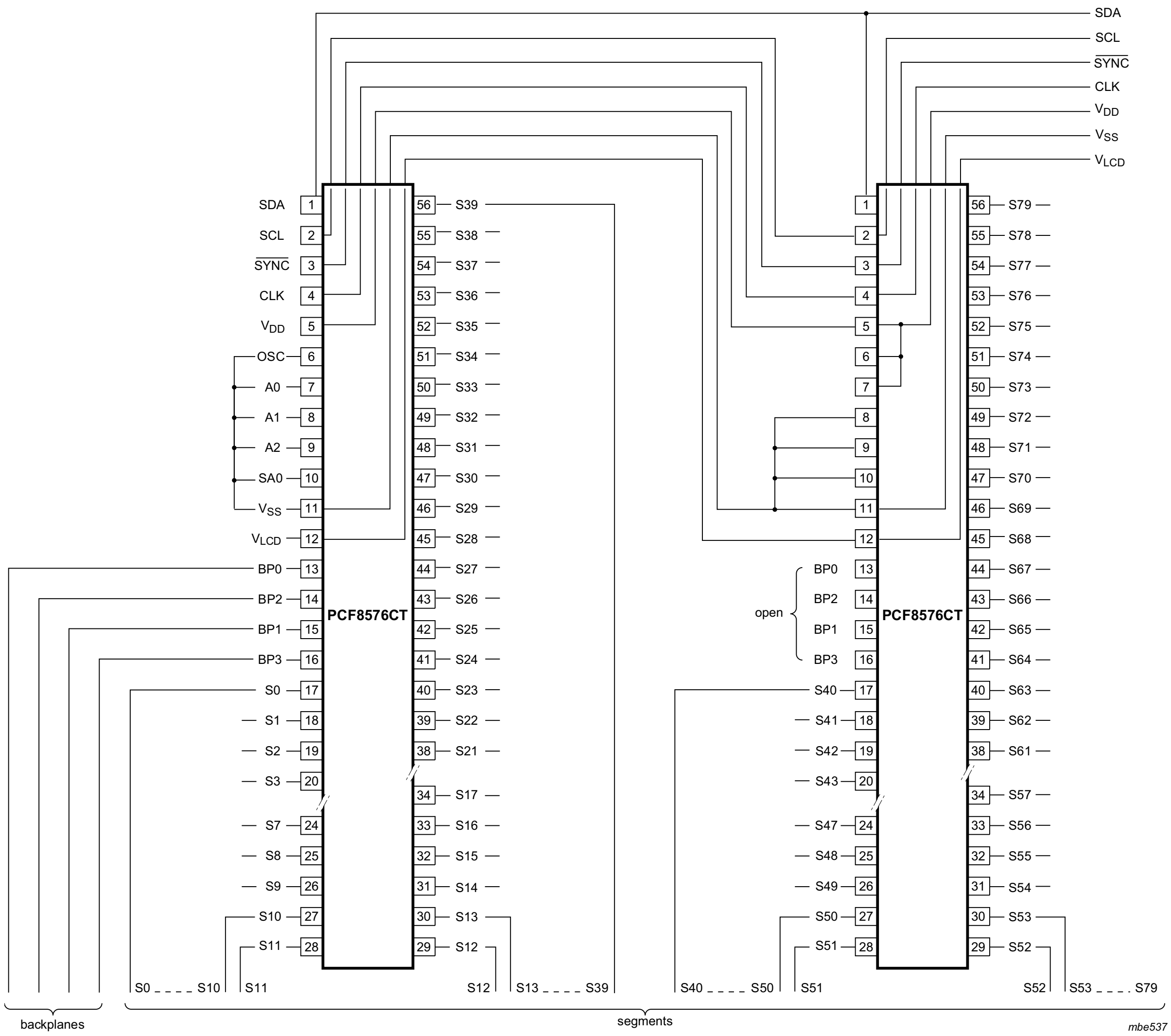
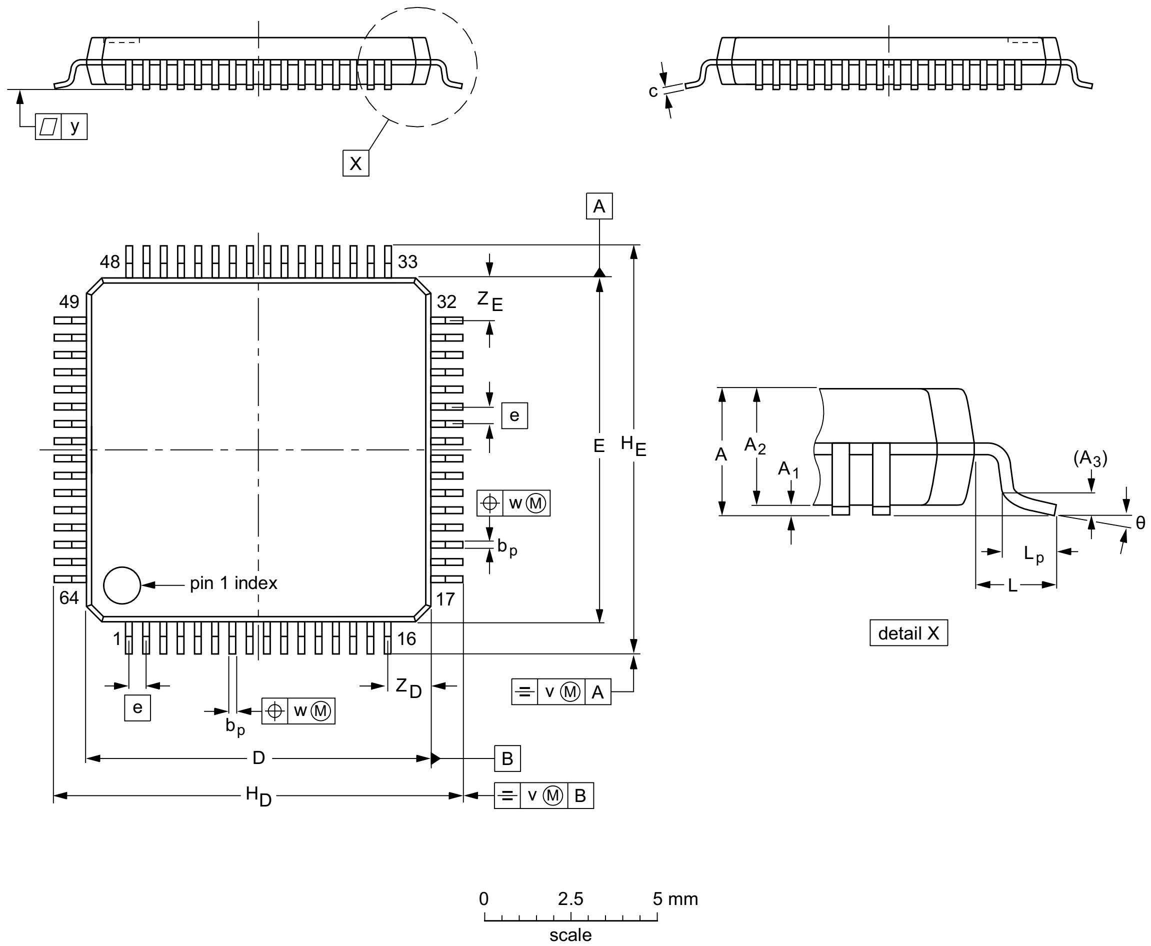


Fig 32. Single plane wiring of packaged PCF8576CT

14. Package outline

LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm **SOT314-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_D	H_E	L	L_p	v	w	y	Z_D(1)	Z_E(1)	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1	0.75 0.45	0.2	0.12	0.1	1.45 1.05	1.45 1.05	7° 0°

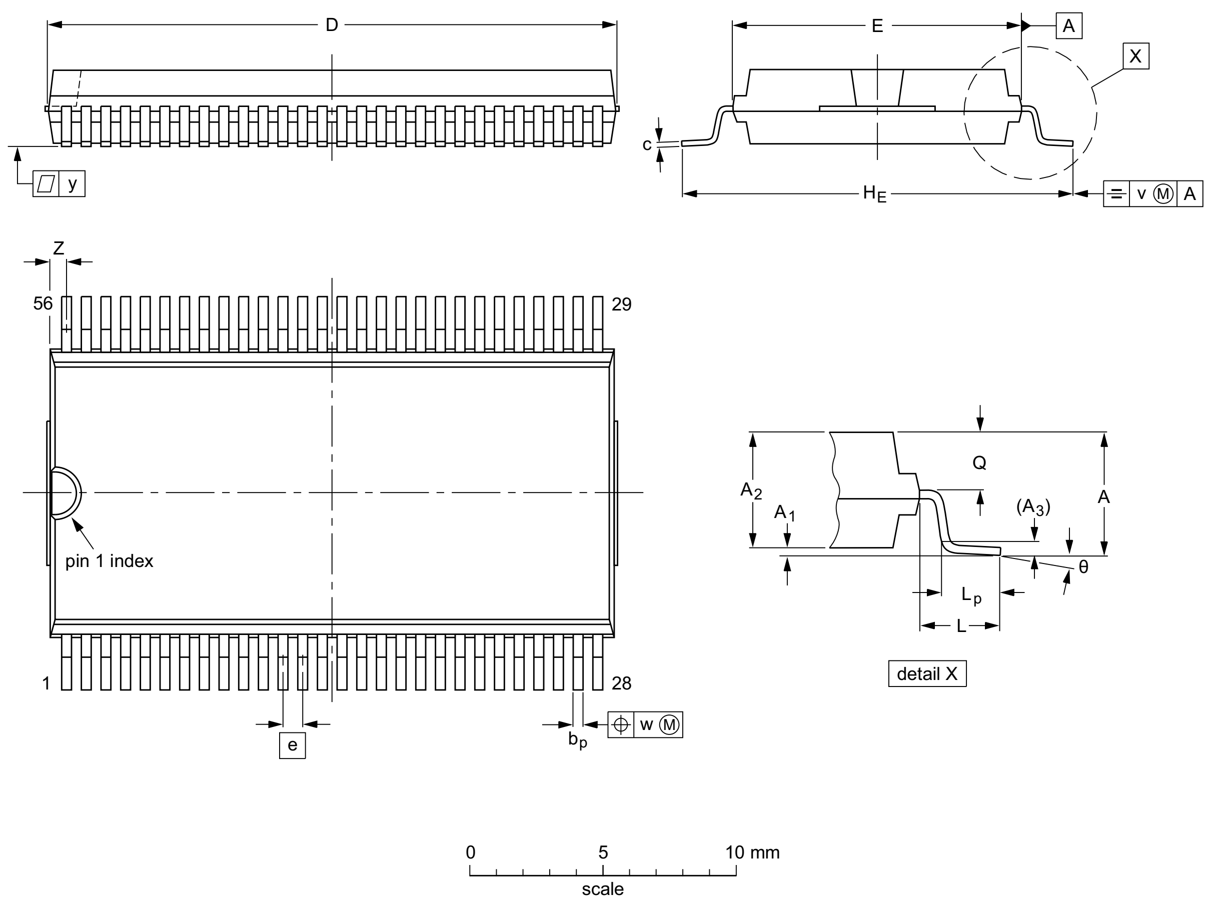
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT314-2	136E10	MS-026				~~00-01-19~~ 03-02-25

Fig 33. Package outline SOT314-2 (LQFP64) of PCF8576CHL/1

VSO56: plastic very small outline package; 56 leads **SOT190-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	3.3	0.3 0.1	3.0 2.8	0.25	0.42 0.30	0.22 0.14	21.65 21.35	11.1 11.0	0.75	15.8 15.2	2.25	1.6 1.4	1.45 1.30	0.2	0.1	0.1	0.90 0.55	7° 0°
inches	0.13	0.012 0.004	0.12 0.11	0.01	0.017 0.012	0.0087 0.0055	0.85 0.84	0.44 0.43	0.0295	0.62 0.60	0.089	0.063 0.055	0.057 0.051	0.008	0.004	0.004	0.035 0.022	

Notes

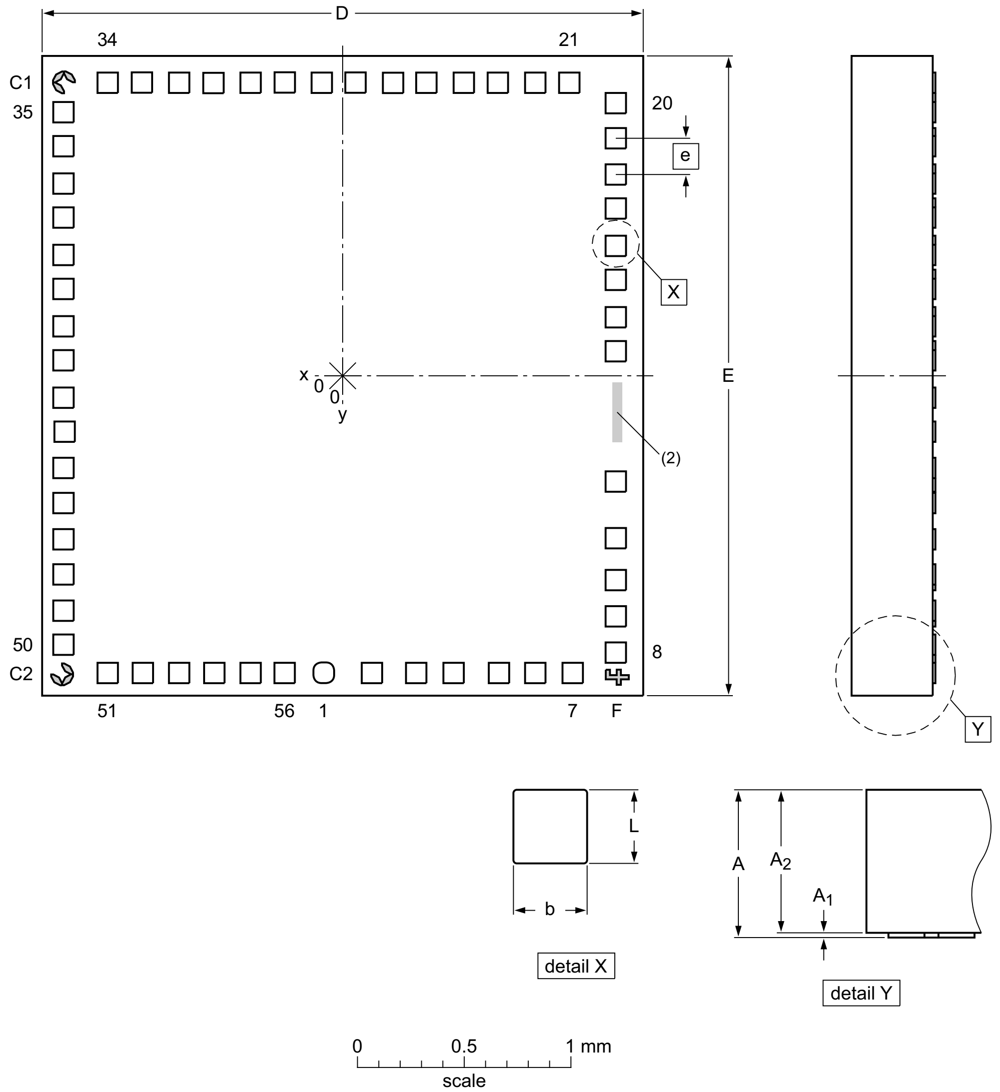
1. Plastic or metal protrusions of 0.3 mm (0.012 inch) maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT190-1						~~97-08-11~~ 03-02-19

Fig 34. Package outline SOT190-1 (VSO56) of PCF8576CT/1

15. Bare die outline

Bare die; 56 bumps; 3.2 x 2.92 x 0.40 mm **PCF8576CU/2**



Dimensions

Unit		A	A_1	A_2	b	D	E	e(1)	L
mm	max							0.610	
	nom	0.398	0.0175	0.380	0.094	2.92	3.2		0.094
	min							0.096	

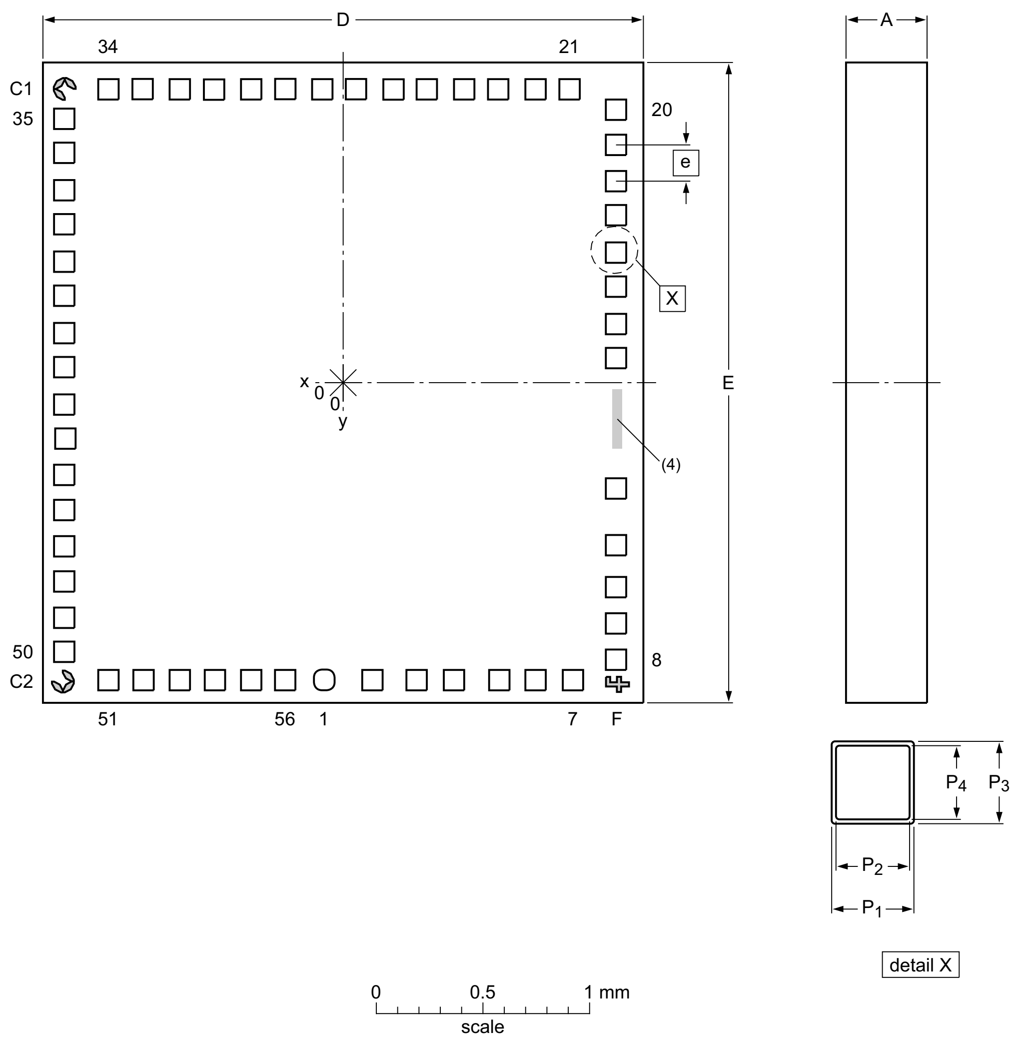
Note
1. Dimension not drawn to scale
2. Marking code: PC8576C-2

pcf8576cu_2_do

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
PCF8576CU/2						~~09-06-02~~ 12-03-22

Fig 35. Bare die outline of PCF8576CU/2/F2

Wire bond die; 56 bonding pads; 3.2 x 2.92 x 0.38 mm **PCF8576CU**



Dimensions

Unit		A	D	E	e(3)	P1(1)	P2(2)	P3(1)	P4(2)
mm	max				0.610				
	nom	0.38	2.92	3.2		0.110	0.097	0.110	0.097
	min				0.096				

Note
1. Pad size
2. Passivation opening
3. Dimension not drawn to scale
4. Marking code: PC8576C-1

pcf8576cu_do

Outline version	References: IEC	JEDEC	JEITA		European projection	Issue date
PCF8576CU						~~09-06-02~~ 12-03-22

Fig 36. Bare die outline of PCF8576CU/F1

Table 19. Pad and bump description for PCF8576CU

All x/y coordinates represent the position of the center of each pad with respect to the center (x/y = 0) of the chip.

Symbol	Pad	X (μm)	Y (μm)	Description
SDA	1	–74	–1380	I^{2}C-bus serial data input/output
SCL	2	148	–1380	I^{2}C-bus serial clock input
$\overline{SYNC}$	3	355	–1380	cascade synchronization input/output
CLK	4	534	–1380	external clock input/output
V_{DD}	5	742	–1380	supply voltage
OSC	6	913	–1380	internal oscillator enable input
A0	7	1087	–1380	subaddress input
A1	8	1290	–1284	subaddress input
A2	9	1290	–1116	subaddress input
SA0	10	1290	–945	subaddress input
V_{SS}	11	1290	–751	logic ground
V_{LCD}	12	1290	–485	LCD supply voltage
BP0	13	1290	125	LCD backplane output
BP2	14	1290	285	LCD backplane output
BP1	15	1290	458	LCD backplane output
BP3	16	1290	618	LCD backplane output
S0	17	1290	791	LCD segment output
S1	18	1290	951	LCD segment output
S2	19	1290	1124	LCD segment output
S3	20	1290	1284	LCD segment output
S4	21	1074	1380	LCD segment output
S5	22	914	1380	LCD segment output
S6	23	741	1380	LCD segment output
S7	24	581	1380	LCD segment output
S8	25	408	1380	LCD segment output
S9	26	248	1380	LCD segment output
S10	27	75	1380	LCD segment output
S11	28	–85	1380	LCD segment output
S12	29	–258	1380	LCD segment output
S13	30	–418	1380	LCD segment output
S14	31	–591	1380	LCD segment output
S15	32	–751	1380	LCD segment output
S16	33	–924	1380	LCD segment output
S17	34	–1084	1380	LCD segment output
S18	35	–1290	1243	LCD segment output
S19	36	–1290	1083	LCD segment output
S20	37	–1290	910	LCD segment output
S21	38	–1290	750	LCD segment output
S22	39	–1290	577	LCD segment output

Table 19. Pad and bump description for PCF8576CU

All x/y coordinates represent the position of the center of each pad with respect to the center (x/y = 0) of the chip.

Symbol	Pad	X (μm)	Y (μm)	Description
S23	40	−1290	417	LCD segment output
S24	41	−1290	244	LCD segment output
S25	42	−1290	84	LCD segment output
S26	43	−1290	−89	LCD segment output
S27	44	−1290	−249	LCD segment output
S28	45	−1290	−422	LCD segment output
S29	46	−1290	−582	LCD segment output
S30	47	−1290	−755	LCD segment output
S31	48	−1290	−915	LCD segment output
S32	49	−1290	−1088	LCD segment output
S33	50	−1290	−1248	LCD segment output
S34	51	−1083	−1380	LCD segment output
S35	52	−923	−1380	LCD segment output
S36	53	−750	−1380	LCD segment output
S37	54	−590	−1380	LCD segment output
S38	55	−417	−1380	LCD segment output
S39	56	−257	−1380	LCD segment output

Table 20. Alignment marks

Symbol	X (μm)	Y (μm)
C1	−1290	1385
C2	−1295	−1385
F	1305	−1405

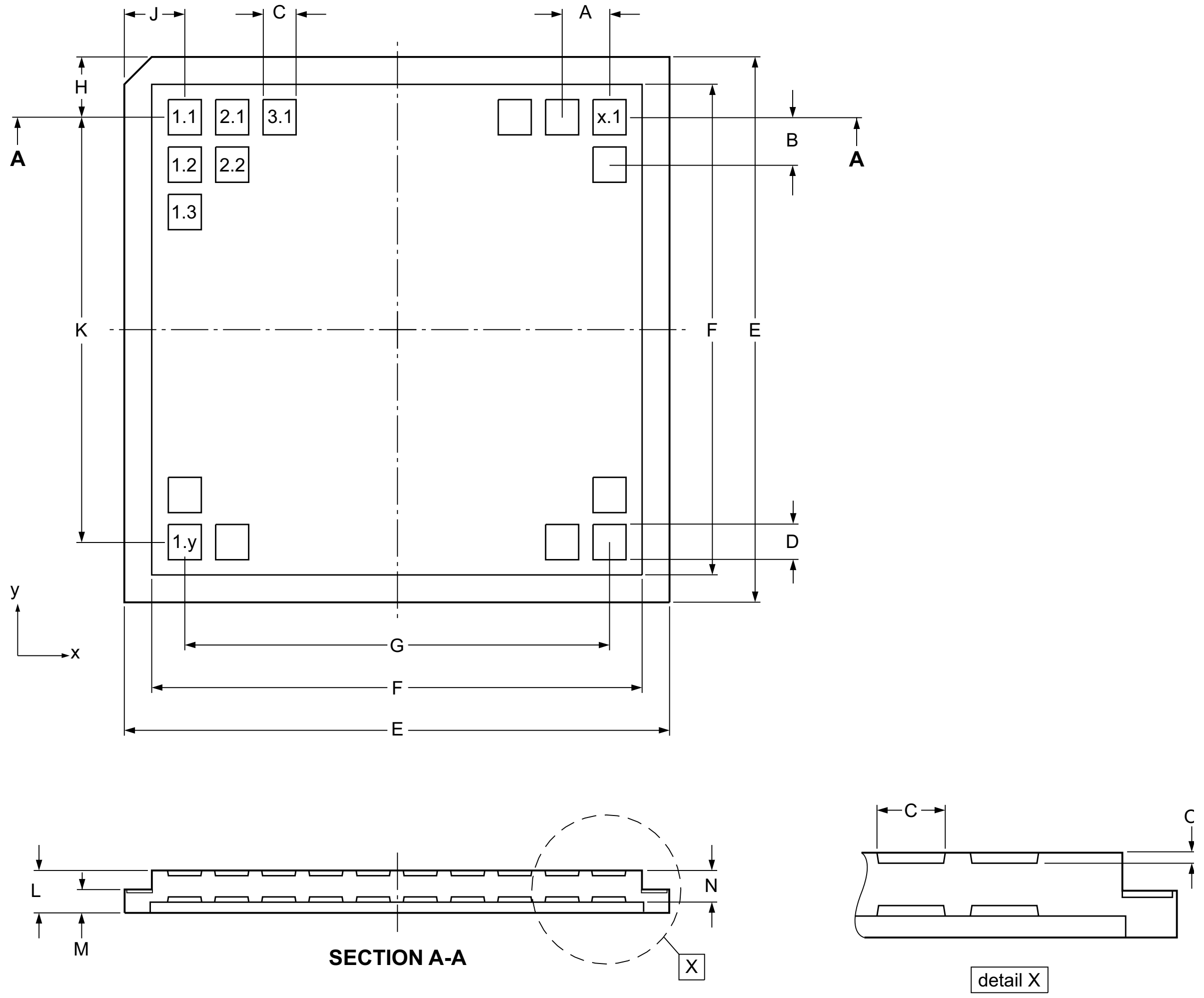
16. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling Metal-Oxide Semiconductor (MOS) devices ensure that all normal precautions are taken as described in *JESD625-A*, *IEC 61340-5* or equivalent standards.

17. Packing information

17.1 Tray information

Tray information for the PCF8576CU/F1 and PCF8576CU/2/F2 is shown in Figure 37, Figure 38 and Table 21.



Dimensions in mm

aaa-0033

Fig 37. Tray details

Table 21. Description of tray details

Tray details are shown in Figure 37.

Tray details														
Dimensions														
A	B	C	D	E	F	G	H	J	K	L	M	N	O	Unit
4.4	4.4	3.02	3.3	50.8	45.72	39.6	5.6	5.6	39.6	3.96	2.18	2.49	0.5	mm
Number of pockets														
x direction							y direction							
10							10							

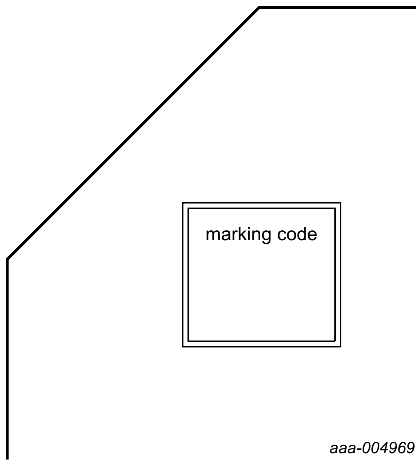


Fig 38. Tray alignment

18. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 “Surface mount reflow soldering description”*.

18.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

18.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

18.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

18.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 39) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 22 and 23

Table 22. SnPb eutectic process (from J-STD-020D)

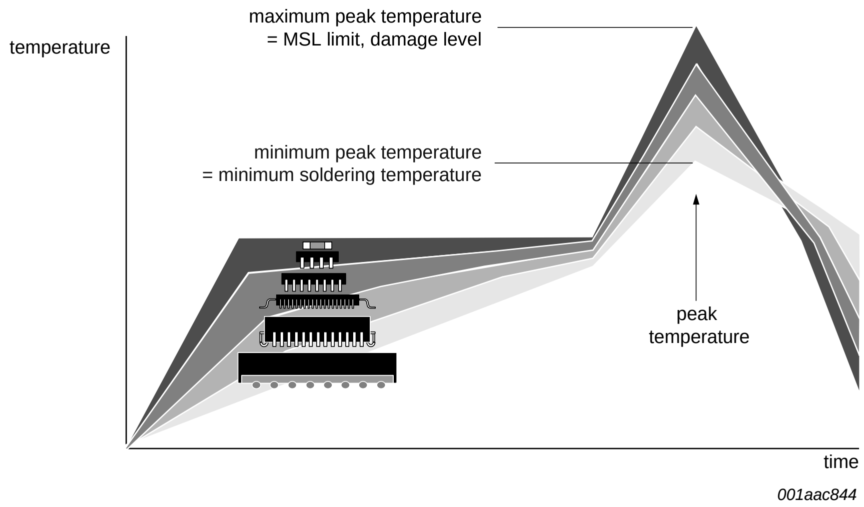
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 23. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 39.



MSL: Moisture Sensitivity Level

Fig 39. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

19. Appendix

19.1 LCD segment driver selection

Table 24. Selection of LCD segment drivers

Type name	Number of elements at MUX							V_{DD} (V)	V_{LCD} (V)	f_{fr} (Hz)	V_{LCD} (V) charge pump	V_{LCD} (V) temperature compensat.	T_{amb} (°C)	Interface	Package	AEC-Q100
	1:1	1:2	1:3	1:4	1:6	1:8	1:9									
PCA8561AHN[5]	18	36	54	72	-	-	-	1.8 to 5.5	1.8 to 5.5	32 to 256[1]	N	N	–40 to 105	I^2C	HVQFN32	Y
PCA8561BHN[5]	18	36	54	72	-	-	-	1.8 to 5.5	1.8 to 5.5	32 to 256[1]	N	N	–40 to 105	SPI	HVQFN32	Y
PCF8566TS	24	48	72	96	-	-	-	2.5 to 6	2.5 to 6	69	N	N	–40 to 85	I^2C	VSO40	N
PCF85162T	32	64	96	128	-	-	-	1.8 to 5.5	2.5 to 6.5	82	N	N	–40 to 85	I^2C	TSSOP48	N
PCA85162T	32	64	96	128	-	-	-	1.8 to 5.5	2.5 to 8	110	N	N	–40 to 95	I^2C	TSSOP48	Y
PCA85262ATT	32	64	96	128	-	-	-	1.8 to 5.5	2.5 to 8	200	N	N	–40 to 105	I^2C	TSSOP48	Y
PCF8551ATT[5]	36	72	108	144	-	-	-	1.8 to 5.5	1.8 to 5.5	32 to 128[1]	N	N	–40 to 85	I^2C	TSSOP48	N
PCF8551BTT[5]	36	72	108	144	-	-	-	1.8 to 5.5	1.8 to 5.5	32 to 128[1]	N	N	–40 to 85	SPI	TSSOP48	N
PCA8551ATT[5]	36	72	108	144	-	-	-	1.8 to 5.5	1.8 to 5.5	32 to 256[1]	N	N	–40 to 105	I^2C	TSSOP48	Y
PCA8551BTT[5]	36	72	108	144	-	-	-	1.8 to 5.5	1.8 to 5.5	32 to 256[1]	N	N	–40 to 105	SPI	TSSOP48	Y
PCF85176T	40	80	120	160	-	-	-	1.8 to 5.5	2.5 to 6.5	82	N	N	–40 to 85	I^2C	TSSOP56	N
PCA85176T	40	80	120	160	-	-	-	1.8 to 5.5	2.5 to 8	110	N	N	–40 to 95	I^2C	TSSOP56	Y
PCA85276ATT	40	80	120	160	-	-	-	1.8 to 5.5	2.5 to 8	200	N	N	–40 to 105	I^2C	TSSOP56	Y
PCF85176H	40	80	120	160	-	-	-	1.8 to 5.5	2.5 to 6.5	82	N	N	–40 to 85	I^2C	TQFP64	N
PCA85176H	40	80	120	160	-	-	-	1.8 to 5.5	2.5 to 8	82	N	N	–40 to 95	I^2C	TQFP64	Y
PCF8553ATT[5]	40	80	120	160	-	-	-	1.8 to 5.5	1.8 to 5.5	32 to 128[1]	N	N	–40 to 85	I^2C	TSSOP56	N
PCF8553BTT[5]	40	80	120	160	-	-	-	1.8 to 5.5	1.8 to 5.5	32 to 128[1]	N	N	–40 to 85	SPI	TSSOP56	N
PCA8553ATT[5]	40	80	120	160	-	-	-	1.8 to 5.5	1.8 to 5.5	32 to 256[1]	N	N	–40 to 105	I^2C	TSSOP56	Y
PCA8553BTT[5]	40	80	120	160	-	-	-	1.8 to 5.5	1.8 to 5.5	32 to 256[1]	N	N	–40 to 105	SPI	TSSOP56	Y
PCA8546ATT	-	-	-	176	-	-	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	N	N	–40 to 95	I^2C	TSSOP56	Y
PCA8546BTT	-	-	-	176	-	-	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	N	N	–40 to 95	SPI	TSSOP56	Y
PCA8547AHT[5]	44	88	-	176	-	-	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	Y	Y[3]	–40 to 95	I^2C	TQFP64	Y
PCA8547BHT[5]	44	88	-	176	-	-	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	Y	Y[3]	–40 to 95	SPI	TQFP64	Y
PCF85134HL	60	120	180	240	-	-	-	1.8 to 5.5	2.5 to 6.5	82	N	N	–40 to 85	I^2C	LQFP80	N
PCA85134H	60	120	180	240	-	-	-	1.8 to 5.5	2.5 to 8	82	N	N	–40 to 95	I^2C	LQFP80	Y

Table 24. Selection of LCD segment drivers *…continued*

Type name	Number of elements at MUX							V_{DD} (V)	V_{LCD} (V)	f_{fr} (Hz)	V_{LCD} (V) charge pump	V_{LCD} (V) temperature compensat.	T_{amb} (°C)	Interface	Package	AEC-Q100
	1:1	1:2	1:3	1:4	1:6	1:8	1:9									
PCA8543AHL	60	120	-	240	-	-	-	2.5 to 5.5	2.5 to 9	60 to 300[1]	Y	Y	–40 to 105	I^{2}C	LQFP80	Y
PCF8545ATT	-	-	-	176	252	320	-	1.8 to 5.5	2.5 to 5.5	60 to 300[1]	N	N	–40 to 85	I^{2}C	TSSOP56	N
PCF8545BTT	-	-	-	176	252	320	-	1.8 to 5.5	2.5 to 5.5	60 to 300[1]	N	N	–40 to 85	SPI	TSSOP56	N
PCF8536AT[4]	-	-	-	176	252	320	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	N	N	–40 to 85	I^{2}C	TSSOP56	N
PCF8536BT[4]	-	-	-	176	252	320	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	N	N	–40 to 85	SPI	TSSOP56	N
PCA8536AT[4]	-	-	-	176	252	320	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	N	N	–40 to 95	I^{2}C	TSSOP56	Y
PCA8536BT[4]	-	-	-	176	252	320	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	N	N	–40 to 95	SPI	TSSOP56	Y
PCF8537AH	44	88	-	176	276	352	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	Y	Y[3]	–40 to 85	I^{2}C	TQFP64	N
PCF8537BH	44	88	-	176	276	352	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	Y	Y[3]	–40 to 85	SPI	TQFP64	N
PCA8537AH	44	88	-	176	276	352	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	Y	Y[3]	–40 to 95	I^{2}C	TQFP64	Y
PCA8537BH	44	88	-	176	276	352	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	Y	Y[3]	–40 to 95	SPI	TQFP64	Y
PCA9620H	60	120	-	240	320	480	-	2.5 to 5.5	2.5 to 9	60 to 300[1]	Y	Y[3]	–40 to 105	I^{2}C	LQFP80	Y
PCA9620U	60	120	-	240	320	480	-	2.5 to 5.5	2.5 to 9	60 to 300[1]	Y	Y[3]	–40 to 105	I^{2}C	bare die	Y
PCF8552DUG[5]	36	72	108	144	-	-	-	1.8 to 5.5	1.8 to 5.5	32 to 128[1]	N	N	–40 to 85	I^{2}C, SPI	bare die	N
PCA8552DUG[5]	36	72	108	144	-	-	-	1.8 to 5.5	1.8 to 5.5	32 to 256[1]	N	N	–40 to 105	I^{2}C, SPI	bare die	Y
PCF8576DU	40	80	120	160	-	-	-	1.8 to 5.5	2.5 to 6.5	77	N	N	–40 to 85	I^{2}C	bare die	N
PCF8576EUG	40	80	120	160	-	-	-	1.8 to 5.5	2.5 to 6.5	77	N	N	–40 to 85	I^{2}C	bare die	N
PCA8576FUG	40	80	120	160	-	-	-	1.8 to 5.5	2.5 to 8	200	N	N	–40 to 105	I^{2}C	bare die	Y
PCF85133U	80	160	240	320	-	-	-	1.8 to 5.5	2.5 to 6.5	82, 110[2]	N	N	–40 to 85	I^{2}C	bare die	N
PCA85133U	80	160	240	320	-	-	-	1.8 to 5.5	2.5 to 8	82, 110[2]	N	N	–40 to 95	I^{2}C	bare die	Y
PCA85233U	80	160	240	320	-	-	-	1.8 to 5.5	2.5 to 8	150, 220[2]	N	N	–40 to 105	I^{2}C	bare die	Y
PCA8530DUG[5]	102	204	-	408	-	-	-	2.5 to 5.5	4 to 12	45 to 300[1]	Y	Y[3]	–40 to 105	I^{2}C, SPI	bare die	Y
PCF85132U	160	320	480	640	-	-	-	1.8 to 5.5	1.8 to 8	60 to 90[1]	N	N	–40 to 85	I^{2}C	bare die	N
PCA85132U	160	320	480	640	-	-	-	1.8 to 5.5	1.8 to 8	60 to 90[1]	N	N	–40 to 95	I^{2}C	bare die	Y
PCA85232U	160	320	480	640	-	-	-	1.8 to 5.5	1.8 to 8	117 to 176[1]	N	N	–40 to 95	I^{2}C	bare die	Y
PCF8538UG	102	204	-	408	612	816	918	2.5 to 5.5	4 to 12	45 to 300[1]	Y	Y[3]	–40 to 85	I^{2}C, SPI[2]	bare die	N
PCA8538UG	102	204	-	408	612	816	918	2.5 to 5.5	4 to 12	45 to 300[1]	Y	Y[3]	–40 to 105	I^{2}C, SPI[2]	bare die	Y

[1] Can be selected by command.

[2] Can be selected by pin configuration.

[3] Extra feature: Temperature sensor.

[4] Extra feature: 6 PWM channels.

[5] In development.

20. Abbreviations

Table 25. Abbreviations

Acronym	Description
CDM	Charged-Device Model
DC	Direct Current
HBM	Human Body Model
I^2C	Inter-Integrated Circuit
IC	Integrated Circuit
LCD	Liquid Crystal Display
LSB	Least Significant Bit
MM	Machine Model
MOS	Metal-Oxide Semiconductor
MSB	Most Significant Bit
MSL	Moisture Sensitivity Level
PCB	Printed-Circuit Board
POR	Power-On Reset
RC	Resistance-Capacitance
RAM	Random Access Memory
RMS	Root Mean Square
SCL	Serial CLock line
SDA	Serial DAta line
SMD	Surface-Mount Device

21. References

[1] **AN10170 —** Design guidelines for COG modules with NXP monochrome LCD drivers

[2] **AN10365 —** Surface mount reflow soldering description

[3] **AN10706 —** Handling bare die

[4] **AN11267 —** EMC and system level ESD design guidelines for LCD drivers

[5] **IEC 60134 —** Rating systems for electronic tubes and valves and analogous semiconductor devices

[6] **IEC 61340-5 —** Protection of electronic devices from electrostatic phenomena

[7] **IPC/JEDEC J-STD-020D —** Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices

[8] **JESD22-A114 —** Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)

[9] **JESD22-A115 —** Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM)

[10] **JESD22-C101 —** Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components

[11] **JESD78 —** IC Latch-Up Test

[12] **UM10204 —** I^2C-bus specification and user manual

[13] **UM10569 —** Store and transport requirements

22. Revision history

Table 26. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCF8576C v.13	20131216	Product data sheet	-	PCF8576C v.12
Modifications:	• Changed product ordering information • Enhanced the description of connecting segment and backplane outputs in a cascade (Section 13)			
PCF8576C v.12	20130716	Product data sheet	-	PCF8576C v.11
PCF8576C v.11	20120330	Product data sheet	-	PCF8576C v.10
PCF8576C v.10	20100722	Product data sheet	-	PCF8576C v.9
PCF8576C v.9	20090709	Product data sheet	-	PCF8576C v.8
PCF8576C v.8	20041122	Product specification	-	PCF8576C v.7
PCF8576C v.7	20011002	Product specification	-	PCF8576C v.6
PCF8576C v.6	19980730	Product specification	-	PCF8576C v.5
PCF8576C v.5	19971114	Product specification	-	PCF8576C v.4
PCF8576C v.4	19970402	Product specification	-	PCF8576C v.3
PCF8576C v.3	19970203	Product specification	-	PCF8576C v.2
PCF8576C v.2	19961209	Product specification	-	PCF8576C v.1
PCF8576C v.1	19950630	Product specification	-	-

23. Legal information

23.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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25. Tables

26. Figures

27. Contents

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