

BOTTOM VIEW

PMZ270XN

N-channel TrenchMOS extremely low level FET

Rev. 01. — 21 February 2008

Product data sheet

1. Product profile

1.1 General description

N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology.

1.2 Features

- Profile 55 % lower than SOT23
- Low on-state resistance
- Leadless package
- Footprint 90 % smaller than SOT23
- Low threshold voltage
- Fast switching

1.3 Applications

- Driver circuits
- DC-to-DC converters
- Load switching in portable appliances

1.4 Quick reference data

- $V_{DS} \leq 20 \text{ V}$
- $R_{DSon} \leq 340 \text{ m}\Omega$
- $I_D \leq 2.15 \text{ A}$
- $P_{tot} \leq 2.50 \text{ W}$

2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline	Symbol
1	gate (G)	<p>Transparent top view</p> <p>SOT883 (SC-101)</p>	<p>mbb076</p>
2	source (S)		
3	drain (D)		

3. Ordering information

Table 2. Ordering information

Type number	Package		Version
	Name	Description	
PMZ270XN	SC-101	leadless ultra small plastic package; 3 solder lands; body 1.0 × 0.6 × 0.5 mm	SOT883

4. Limiting values

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

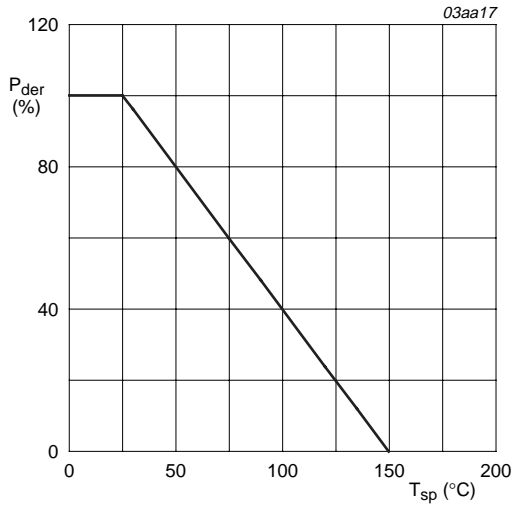
Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	20	V
V_{DGR}	drain-gate voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	20	V
V_{GS}	gate-source voltage		-	±12	V
I_D	drain current	$T_{sp} = 25\text{ °C}$; $V_{GS} = 4.5\text{ V}$; see Figure 2 and 3	-	2.15	A
		$T_{sp} = 100\text{ °C}$; $V_{GS} = 4.5\text{ V}$; see Figure 2	-	1.36	A
I_{DM}	peak drain current	$T_{sp} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; see Figure 3	-	4.30	A
P_{tot}	total power dissipation	$T_{sp} = 25\text{ °C}$; see Figure 1	-	2.50	W
T_{stg}	storage temperature	-	-55	+150	°C
T_j	junction temperature	-	-55	+150	°C

Source-drain diode

I_S	source current	$T_{sp} = 25\text{ °C}$	-	2.15	A
I_{SM}	peak source current	$T_{sp} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	4.30	A

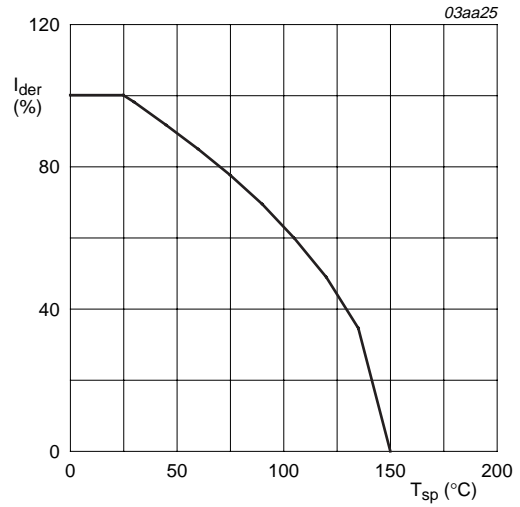
Electrostatic discharge

V_{esd}	electrostatic discharge voltage	all pins			
		human body model; $C = 100\text{ pF}$; $R = 1.5\text{ k}\Omega$	-	65	V
		machine model; $C = 200\text{ pF}$	-	35	V



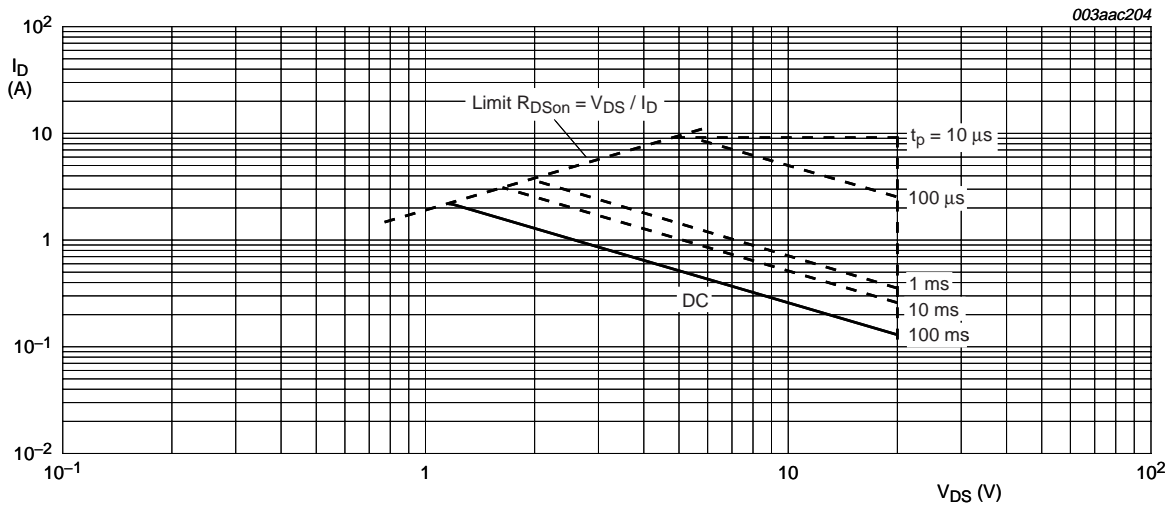
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of solder point temperature



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of solder point temperature



T_{sp} = 25 °C; I_{DM} is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	see Figure 4	-	-	50	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint	[1]	-	670	K/W

[1] Mounted on a printed-circuit board; vertical in still air.

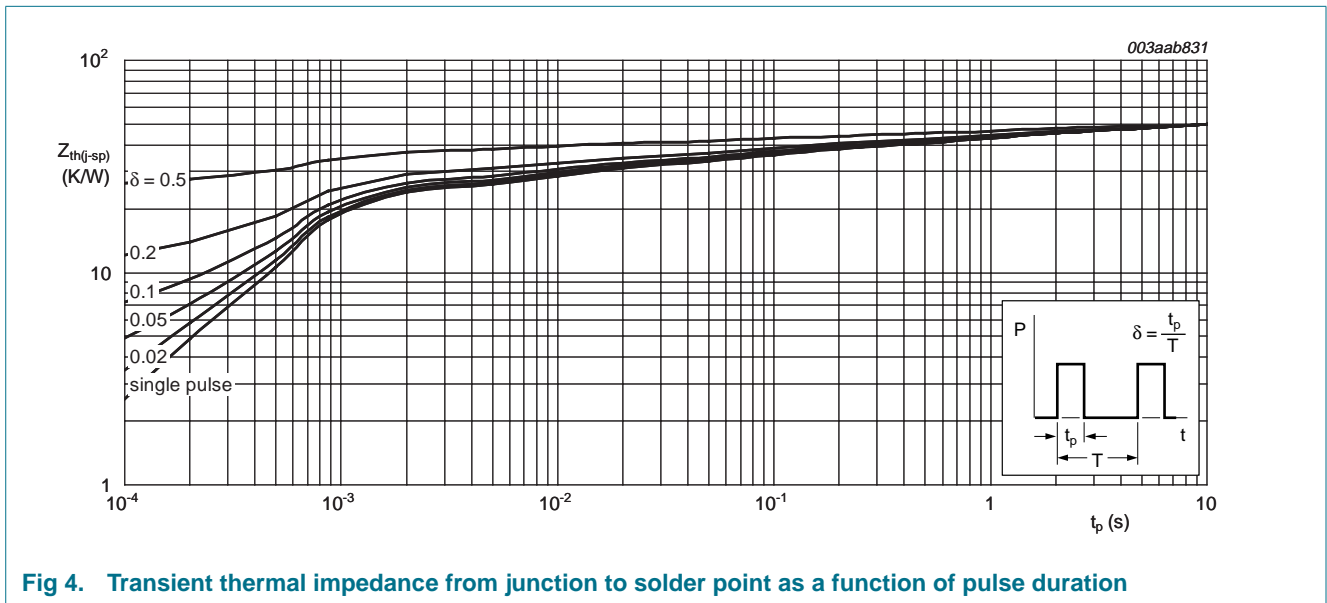
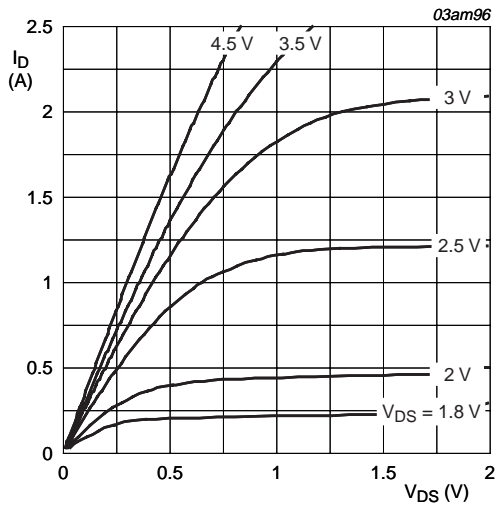


Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration

6. Characteristics

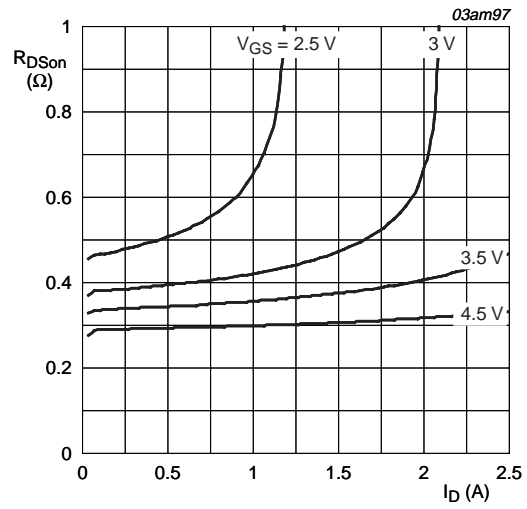
Table 5. Characteristics
T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 10 μA; V _{GS} = 0 V				
		T _j = 25 °C	20	-	-	V
		T _j = -55 °C	18	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 0.25 mA; V _{DS} = V _{GS} ; see Figure 9 and 10				
		T _j = 25 °C	0.5	1	1.5	V
		T _j = 150 °C	0.35	-	-	V
		T _j = -55 °C	-	-	1.8	V
I _{DSS}	drain leakage current	V _{DS} = 20 V; V _{GS} = 0 V				
		T _j = 25 °C	-	-	1	μA
		T _j = 150 °C	-	-	100	μA
I _{GSS}	gate leakage current	V _{GS} = ±12 V; V _{DS} = 0 V	-	10	100	nA
R _{DS(on)}	drain-source on-state resistance	V _{GS} = 4.5 V; I _D = 0.2 A; see Figure 6 and 8				
		T _j = 25 °C	-	270	340	mΩ
		T _j = 150 °C	-	430	540	mΩ
		V _{GS} = 2.5 V; I _D = 0.1 A; see Figure 6 and 8	-	440	520	mΩ
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = 1 A; V _{DS} = 10 V; V _{GS} = 4.5 V; see Figure 11 and 12	-	0.72	-	nC
Q _{GS}	gate-source charge		-	0.18	-	nC
Q _{GD}	gate-drain charge		-	0.18	-	nC
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 20 V; f = 1 MHz; see Figure 14	-	34	-	pF
C _{oss}	output capacitance		-	12	-	pF
C _{rss}	reverse transfer capacitance		-	8	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = 10 V; R _L = 10 Ω; V _{GS} = 4.5 V; R _G = 6 Ω	-	5	-	ns
t _r	rise time		-	11	-	ns
t _{d(off)}	turn-off delay time		-	11	-	ns
t _f	fall time		-	6	-	ns
Source-drain diode						
V _{SD}	source-drain voltage	I _S = 0.3 A; V _{GS} = 0 V; see Figure 13	-	0.8	1.2	V



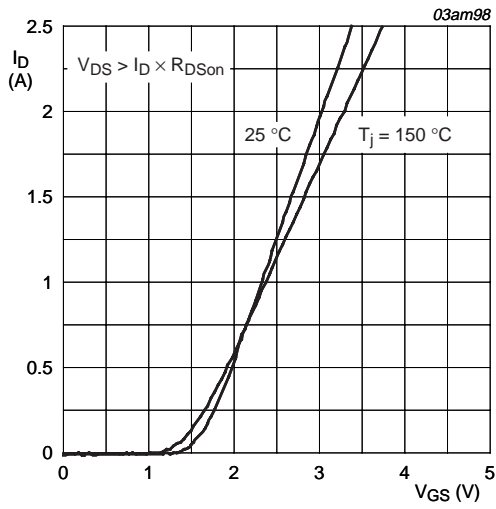
$T_j = 25\text{ }^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



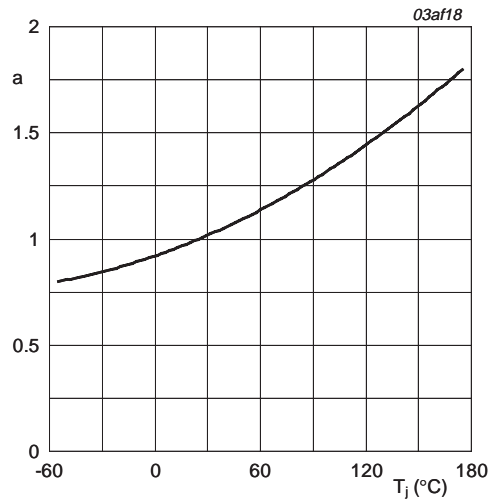
$T_j = 25\text{ }^\circ\text{C}$

Fig 6. Drain-source on-state resistance as a function of drain current; typical values



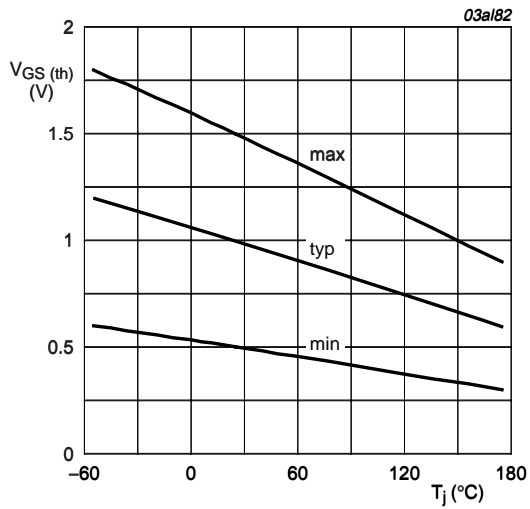
$T_j = 25\text{ }^\circ\text{C}$ and $150\text{ }^\circ\text{C}$; $V_{DS} > I_D \times R_{DSon}$

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values



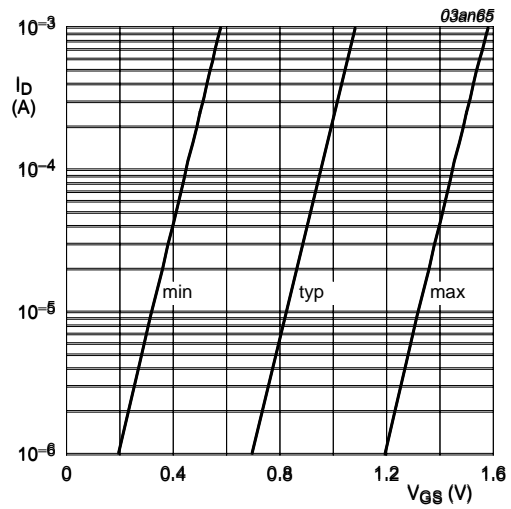
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature



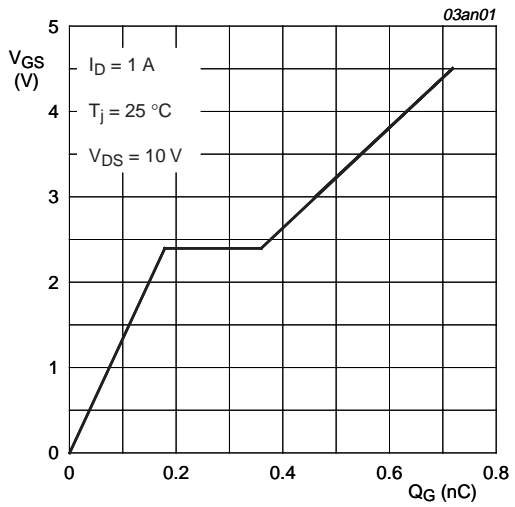
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature



$T_j = 25 \text{ }^{\circ}C; V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



$I_D = 1 \text{ A}; V_{DS} = 10 \text{ V}$

Fig 11. Gate-source voltage as a function of gate charge; typical values

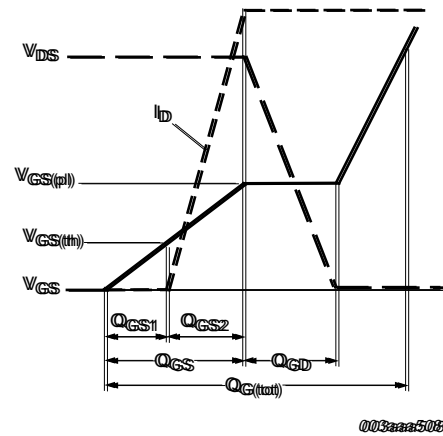
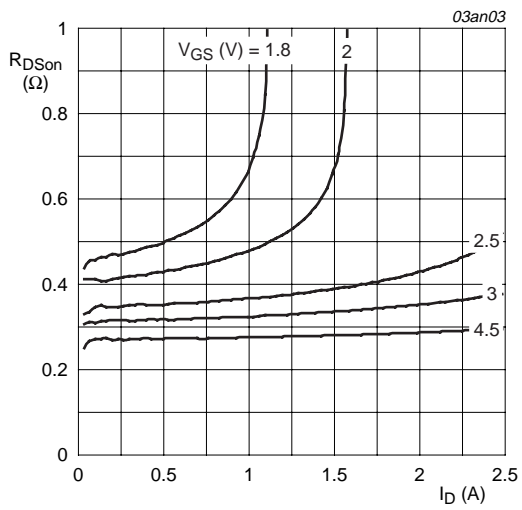
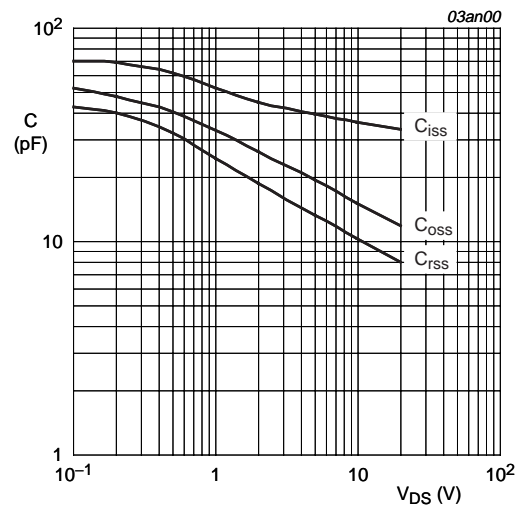


Fig 12. Gate charge waveform definitions



$T_j = 25\text{ }^\circ\text{C}$ and $150\text{ }^\circ\text{C}$; $V_{GS} = 0\text{ V}$

Fig 13. Source current as a function of source-drain voltage; typical values



$V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$

Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

7. Package outline

Leadless ultra small plastic package; 3 solder lands; body 1.0 x 0.6 x 0.5 mm

SOT883

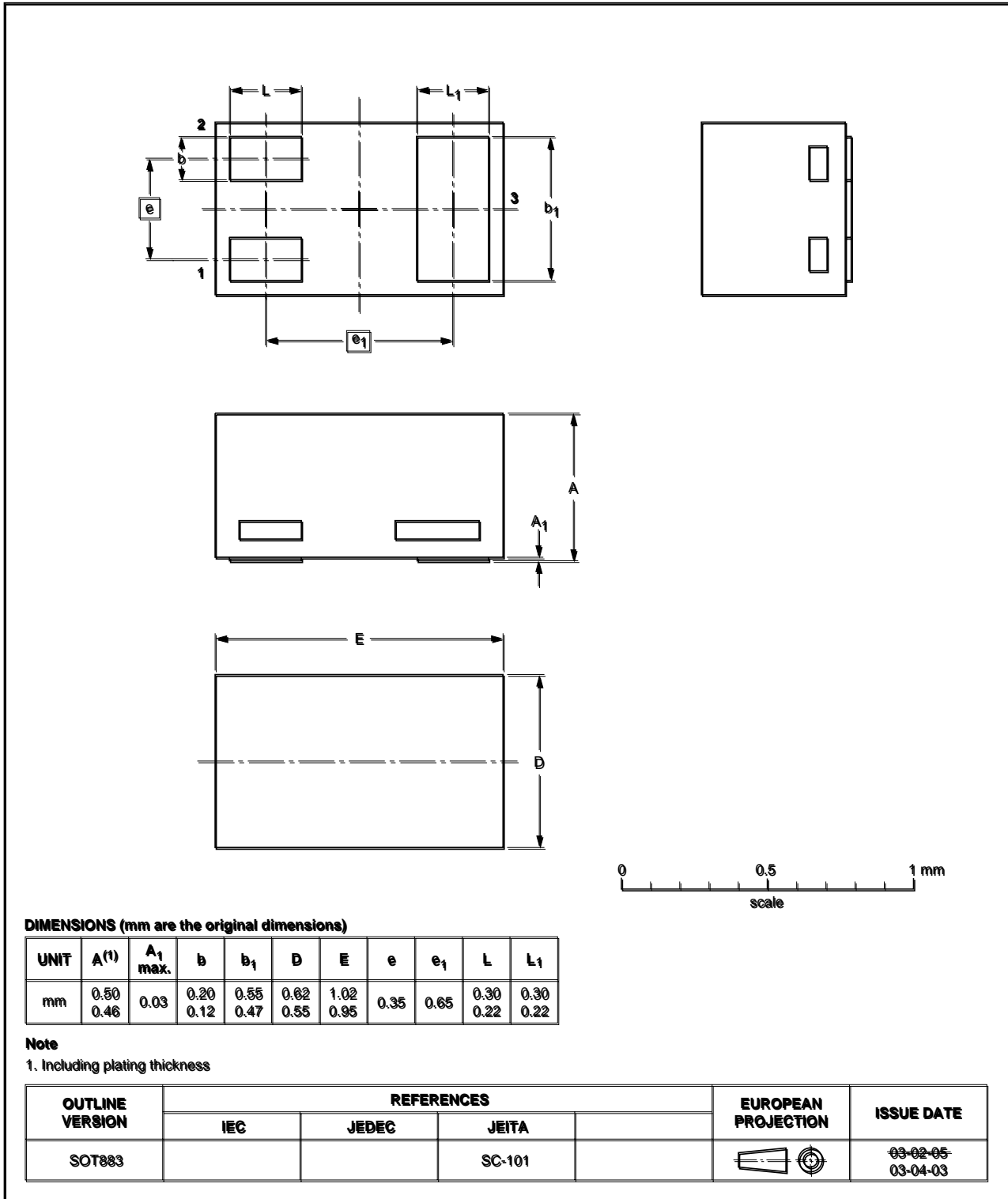
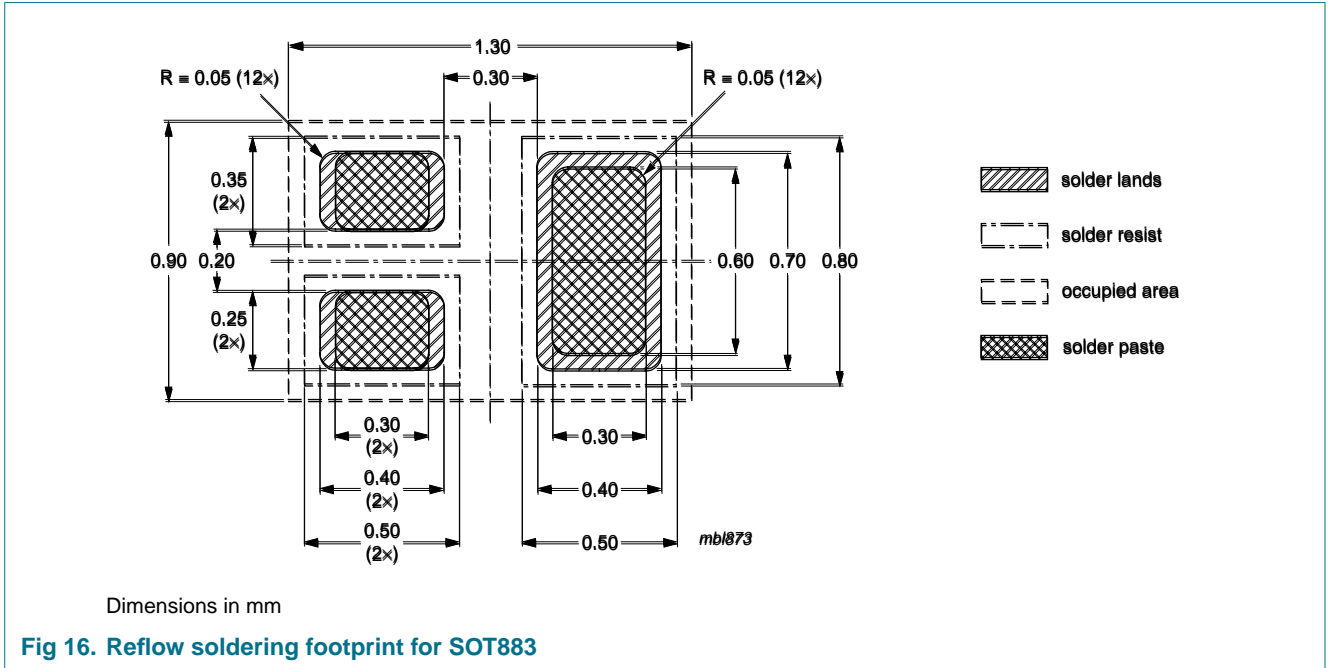


Fig 15. Package outline SOT883 (SC-101)

8. Soldering



9. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PMZ270XN_1	20080221	Product data sheet	-	-

10. Legal information

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Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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