74ABT374A

Octal D-type flip-flop; positive-edge trigger; 3-state Rev. 2 — 18 December 2012 Production

Product data sheet

General description 1.

The 74ABT374A high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT374A is an 8-bit, edge triggered register coupled to eight 3-state output buffers. The two sections of the device are controlled independently by the clock input (CP) and output enable input (\overline{OE}) control gates.

The register is fully edge-triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

The 3-state output buffers are designed to drive heavily loaded 3-state buses, MOS memories, or MOS microprocessors. The active LOW output enable (OE) controls all eight 3-state buffers independent of the clock operation.

When OE is LOW, the stored data appears at the outputs. When OE is HIGH, the outputs are in the high-impedance "OFF" state, which means they will neither drive nor load the bus.

Features and benefits 2.

- 8-bit positive edge triggered register
- 3-state output buffers
- Power-on 3-state
- Power-on reset
- Output capability: +64 mA/–32 mA
- Latch-up protection exceeds 500 mA per JESD78B class II level A
- ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
- Live insertion/extraction permitted



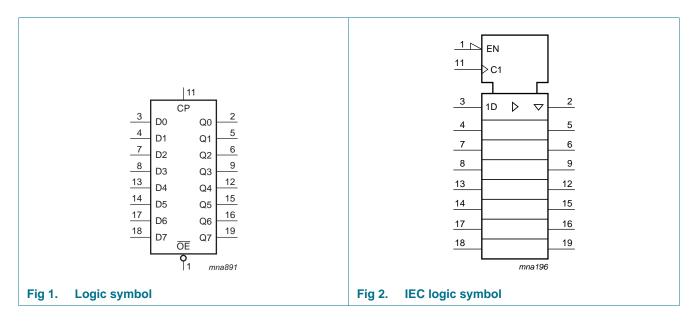
Octal D-type flip-flop; positive-edge trigger; 3-state

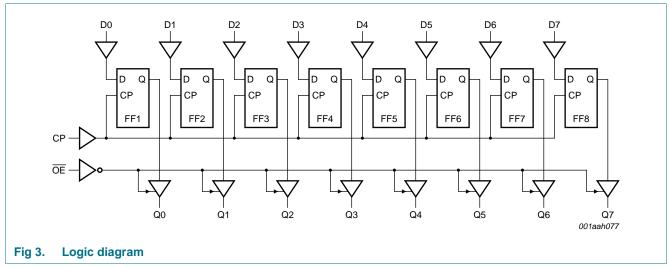
3. Ordering information

Table 1. Ordering information

Type number	Package									
	Temperature range	Name	Description	Version						
74ABT374AN	–40 °C to +85 °C	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1						
74ABT374AD	–40 °C to +85 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1						
74ABT374ADB	–40 °C to +85 °C	SSOP20	plastic shrink small outline package; 20 leads; body width 5.3 mm	SOT339-1						
74ABT374APW	–40 °C to +85 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1						

4. Functional diagram

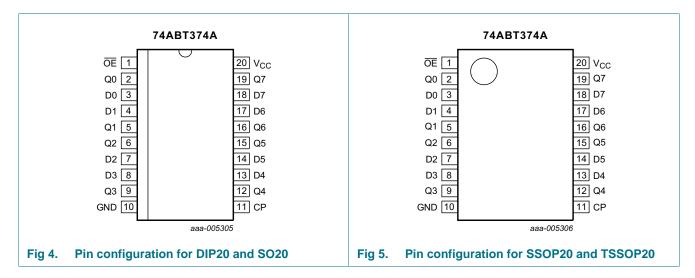




Octal D-type flip-flop; positive-edge trigger; 3-state

5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
ŌE	1	3-state output enable input (active LOW)
D0, D1, D2, D3, D4, D5, D6, D7	3, 4, 7, 8, 13, 14, 17, 18	data input
GND	10	ground (0 V)
СР	11	clock pulse input (active rising edge)
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	2, 5, 6, 9, 12, 15, 16, 19	3-state flip-flop output
V _{CC}	20	supply voltage

6. Functional description

Table 3. Function table [1]

Operating mode	Input		Internal	Output	
	OE	СР	Dn	flip-flop	Qn
Load and read register	L	\uparrow	1	L	L
	L	↑	h	Н	Н
Load register and disable output	Н	↑	I	L	Z
	Н	\uparrow	h	Н	Z

^[1] H = HIGH voltage level

h = HIGH voltage level one setup time prior to the LOW-to-HIGH CP transition

I = LOW voltage level one setup time prior to the LOW-to-HIGH CP transition

L = LOW voltage level

Z = high-impedance OFF-state

^{↑ =} LOW-to-HIGH clock transition

Octal D-type flip-flop; positive-edge trigger; 3-state

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
VI	input voltage		[<u>1</u>] -1.2	+7.0	V
Vo	output voltage	output in OFF-state or HIGH-state	[<u>1]</u> -0.5	+5.5	V
I _{IK}	input clamping current	V _I < 0 V	-18	-	mA
I _{OK}	output clamping current	V _O < 0 V	-50	-	mA
I _O	output current	output in LOW-state	-	128	mA
Tj	junction temperature		[2] _	150	°C
T _{stg}	storage temperature		-65	+150	°C

^[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

8. Recommended operating conditions

Table 5. Operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{CC}	supply voltage		4.5	-	5.5	V
VI	input voltage		0	-	V_{CC}	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
I _{OH}	HIGH-level output current		-32	-	-	mA
I _{OL}	LOW-level output current		-	-	64	mA
$\Delta t / \Delta V$	input transition rise and fall rate		0	-	10	ns/V
T _{amb}	ambient temperature	in free air	-40	-	+85	°C

9. Static characteristics

Table 6. Static characteristics

Symbol	Parameter	Conditions		25 °C			-40 °C to +85 °C		
				Тур	Max	Min	Max		
V_{IK}	input clamping voltage	$V_{CC} = 4.5 \text{ V}; I_{IK} = -18 \text{ mA}$	-1.2	-0.9	-	-1.2	-	V	
V _{OH} HIGH-level output		$V_I = V_{IL} \text{ or } V_{IH}$							
	voltage	$V_{CC} = 4.5 \text{ V}; I_{OH} = -3 \text{ mA}$	2.5	2.9	-	2.5	-	V	
		$V_{CC} = 5.0 \text{ V}; I_{OH} = -3 \text{ mA}$	3.0	3.4	-	3.0	-	V	
		$V_{CC} = 4.5 \text{ V}; I_{OH} = -32 \text{ mA}$	2.0	2.4	-	2.0	-	V	
V _{OL}	LOW-level output voltage	V_{CC} = 4.5 V; I_{OL} = 64 mA; V_I = V_{IL} or V_{IH}	-	0.42	0.55	-	0.55	V	

^[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

Octal D-type flip-flop; positive-edge trigger; 3-state

Table 6. Static characteristics ...continued

Symbol	Parameter	Conditions			25 °C		-40 °C t	Unit	
				Min	Тур	Max	Min	Max	
$V_{OL(pu)}$	power-up LOW-level output voltage	V_{CC} = 5.5 V; I_O = 1 mA; V_I = GND or V_{CC}	<u>[1]</u>	-	0.13	0.55	-	0.55	V
I _I	input leakage current	V_{CC} = 5.5 V; V_I = V_{CC} or GND		-	±0.01	±1.0	-	±1.0	μΑ
I _{OFF}	power-off leakage current	V_{CC} = 0 V; V_{I} or $V_{O} \le 4.5$ V		-	±5.0	±100	-	±100	μΑ
I _{O(pu/pd)}	power-up/power-down output current	$V_{CC} = 2.0 \text{ V}; V_O = \underline{0.5} \text{ V};$ $V_I = \text{GND or } V_{CC}; \overline{\text{OE}} \text{ HIGH}$	[2]	-	±5.0	±50	-	±50	μΑ
I_{OZ}	OFF-state output	V_{CC} = 5.5 V; V_I = V_{IL} or V_{IH}							
	current	$V_0 = 2.7 \text{ V}$		-	5.0	50	-	50	μΑ
		$V_0 = 0.5 V$		-50	-5.0	-	-50	-	μΑ
I_{LO}	output leakage current	HIGH-state; $V_O = 5.5 \text{ V}$; $V_{CC} = 5.5 \text{ V}$; $V_I = \text{GND or } V_{CC}$		-	5.0	50	-	50	μΑ
I _O	output current	$V_{CC} = 5.5 \text{ V}; V_{O} = 2.5 \text{ V}$	<u>[3]</u>	-180	-100	-50	-180	-50	mA
I_{CC}	supply current	V_{CC} = 5.5 V; V_I = GND or V_{CC}							
		outputs HIGH-state		-	110	250	-	250	μΑ
		outputs LOW-state		-	24	30	-	30	mA
		outputs disabled		-	110	250	-	250	μΑ
Δl _{CC}	additional supply current	per input pin; V_{CC} = 5.5 V; one input at 3.4 V; other inputs at V_{CC} or GND	[4]	-	0.5	1.5	-	1.5	mA
C _I	input capacitance	$V_I = 0 \text{ V or } V_{CC}$		-	4	-	-	-	pF
Co	output capacitance	outputs disabled; $V_O = 0 \text{ V or } V_{CC}$		-	7	-	-	-	pF

^[1] For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.

10. Dynamic characteristics

Table 7. Dynamic characteristics GND = 0 *V; for test circuit, see Figure 9.*

Symbol	Parameter	Conditions	25 °C; V _{CC} = 5.0 V			-40 °C to V _{CC} = 5.0	Unit	
			Min	Тур	Max	Min	Max	
f _{max}	maximum frequency	see Figure 6	200	300	-	200	-	MHz
t _{PLH}	LOW to HIGH propagation delay	CP to Qn; see Figure 6	1.7	3.4	4.5	1.7	5.1	ns
t _{PHL}	HIGH to LOW propagation delay	CP to Qn; see Figure 6	2.0	3.8	4.9	2.0	5.2	ns
t _{PZH}	OFF-state to HIGH propagation delay	OE to Qn; see Figure 8	1.2	3.5	4.5	1.2	5.4	ns

74ABT374A

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^[2] This parameter is valid for any V_{CC} between 0 V and 2.1 V, with a transition time of up to 10 ms. From V_{CC} = 2.1 V to V_{CC} = 5 V \pm 10 % a transition time of up to 100 μ s is permitted.

^[3] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

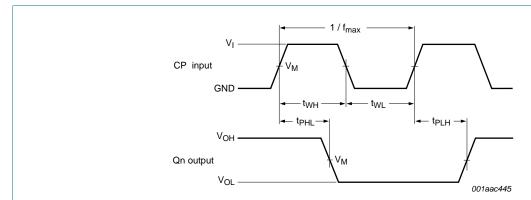
^[4] This is the increase in supply current for each input at 3.4 V.

Octal D-type flip-flop; positive-edge trigger; 3-state

Table 7. Dynamic characteristics ...continued GND = 0 V; for test circuit, see <u>Figure 9</u>.

Symbol	Parameter	Conditions	25 °C	; V _{CC} =	5.0 V	-40 °C to V _{CC} = 5.0	Unit	
			Min	Тур	Max	Min	Max	
t _{PZL}	OFF-state to LOW propagation delay	OE to Qn; see Figure 8	2.2	4.3	5.4	2.2	6.2	ns
t _{PHZ}	HIGH to OFF-state propagation delay	OE to Qn; see Figure 8	1.8	3.6	4.7	1.8	5.2	ns
t _{PLZ}	LOW to OFF-state propagation delay	OE to Qn; see Figure 8	1.5	3.0	4.1	1.5	4.3	ns
$t_{su(H)}$	set-up time HIGH	Dn to CP; see Figure 7	1.5	0.6	-	1.5	-	ns
$t_{su(L)}$	set-up time LOW	Dn to CP; see Figure 7	1.2	0.3	-	1.2	-	ns
t _{h(H)}	hold time HIGH	CP to Dn; see Figure 7	1.0	-0.3	-	1.0	-	ns
t _{h(L)}	hold time LOW	CP to Dn; see Figure 7	1.0	-0.5	-	1.0	-	ns
t_{WH}	pulse width HIGH	CP; see Figure 6	2.0	0.8	-	2.0	-	ns
t _{WL}	pulse width LOW	CP; see Figure 6	2.8	1.0	-	2.8	-	ns

11. Waveforms

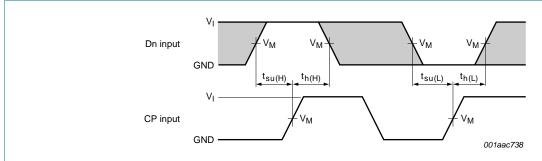


 $V_{M} = 1.5 V$

 $V_{\mbox{\scriptsize OL}}$ and $V_{\mbox{\scriptsize OH}}$ are typical output voltage levels that occur with the output load.

Fig 6. Propagation delay clock input (CP) to output (Qn), clock pulse (CP) width and maximum clock (CP) frequency

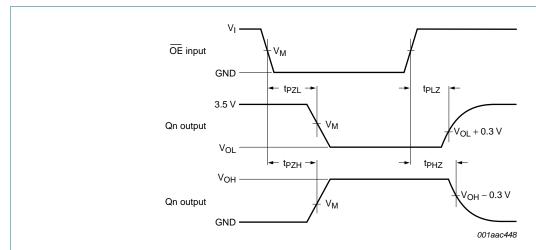
Octal D-type flip-flop; positive-edge trigger; 3-state



 $V_{M} = 1.5 V$

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig 7. Set-up and hold times data output (Dn) to clock (CP)

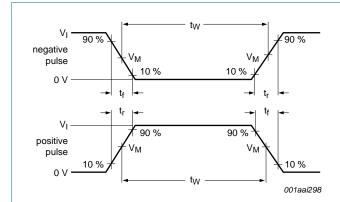


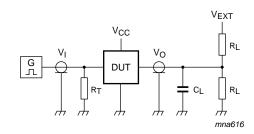
 $V_{M} = 1.5 \ V$

 V_{OL} and V_{OH} are typical output voltage levels that occur with the output load

Fig 8. 3-state output (Qn) enable and disable times

Octal D-type flip-flop; positive-edge trigger; 3-state





a. Input pulse definition

b. Test circuit

Test data is given in Table 8.

 R_L = Load resistance.

 C_L = Load capacitance including jig and probe capacitance.

 R_T = Termination resistance should be equal to output impedance Z_0 of the pulse generator.

 V_{EXT} = External voltage for measuring switching times.

Fig 9. Test circuit for measuring switching times

Table 8. Test data

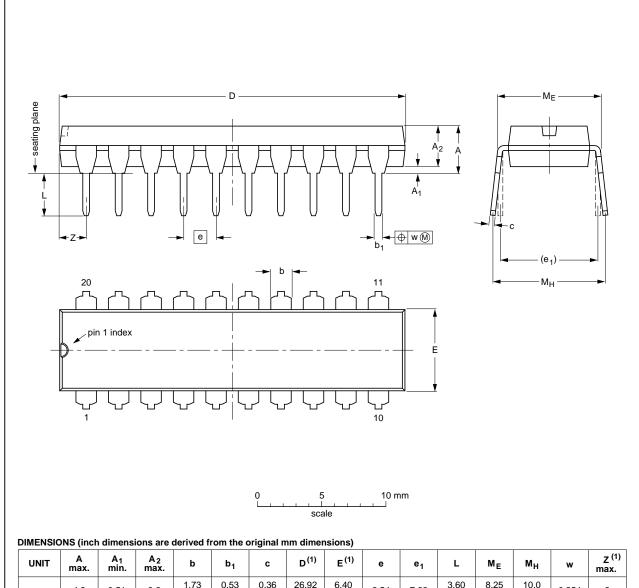
Input				Load		V _{EXT}			
VI	f_i t_W t_r, t_f C_L		CL	R _L t _{PHL} , t _{PLH} t _{PZH} , t _{PHZ}		t _{PZL} , t _{PLZ}			
3.0 V	1 MHz	500 ns	\leq 2.5 ns	50 pF	500Ω	open	open	7.0 V	

Octal D-type flip-flop; positive-edge trigger; 3-state

12. Package outline

DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1



UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	С	D ⁽¹⁾	E ⁽¹⁾	е	e ₁	L	ME	Мн	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

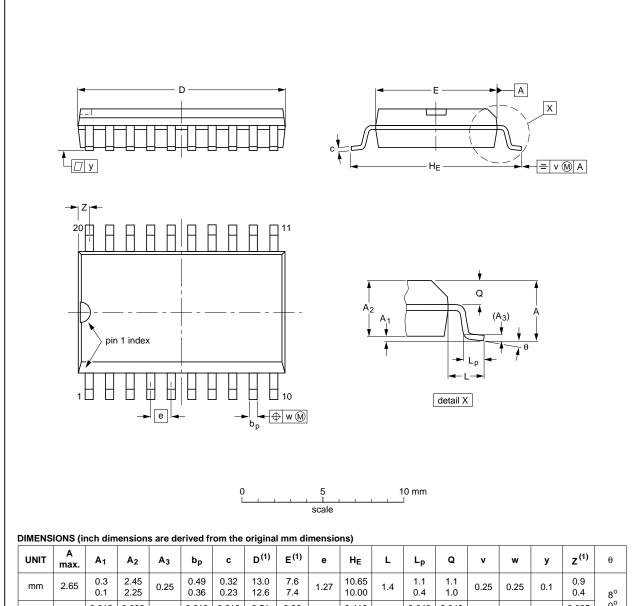
OUTLINE		EUROPEAN	ISSUE DATE		
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE
SOT146-1		MS-001	SC-603		99-12-27 03-02-13

Fig 10. Package outline SOT146-1 (DIP20)

74ABT374

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



UNIT	A max.	A ₁	A ₂	А3	bp	С	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Q	٧	w	у	z ⁽¹⁾	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	0°

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE	
SOT163-1	075E04	MS-013				99-12-27 03-02-19	

Fig 11. Package outline SOT163-1 (SO20)

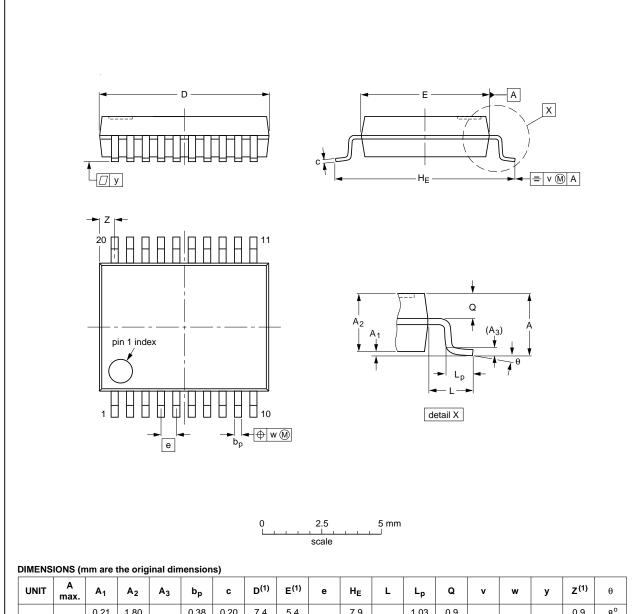
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SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1



_																			
	UNIT	A max.	A ₁	A ₂	A ₃	bp	C	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
	mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8° 0°

Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE	
SOT339-1		MO-150				99-12-27 03-02-19	

Fig 12. Package outline SOT339-1 (SSOP20)

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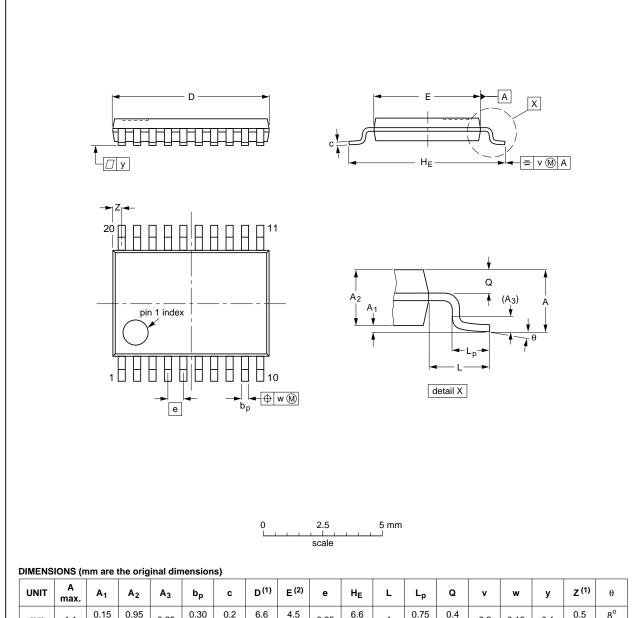
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TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



UNIT	A max.	A ₁	A ₂	A ₃	b _p	С	D ⁽¹⁾	E ⁽²⁾	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE		
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT360-1		MO-153				99-12-27 03-02-19

Fig 13. Package outline SOT360-1 (TSSOP20)

Octal D-type flip-flop; positive-edge trigger; 3-state

13. Abbreviations

Table 9. Abbreviations

Acronym	Description
BiCMOS	Bipolar Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MM	Machine Model

14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes				
74ABT374A v.2	20121218	Product data sheet	-	74ABT374A v.1				
Modifications:	 The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. 							
	 Legal texts 	have been adapted to the	new company name whe	ere appropriate.				
74ABT374A v.1	19950906	Product specification	-	-				

Octal D-type flip-flop; positive-edge trigger; 3-state

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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74ABT374A NXP Semiconductors

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17. Contents

1	General description 1
2	Features and benefits
3	Ordering information 2
4	Functional diagram 2
5	Pinning information 3
5.1	Pinning
5.2	Pin description
6	Functional description 3
7	Limiting values 4
8	Recommended operating conditions 4
9	Static characteristics 4
10	Dynamic characteristics 5
11	Waveforms 6
12	Package outline
13	Abbreviations
14	Revision history
15	Legal information14
15.1	Data sheet status
15.2	Definitions
15.3	Disclaimers
15.4	Trademarks
16	Contact information 15
17	Contents

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