

# 74ABT162244

16-bit buffer/line driver with 30  $\Omega$  series termination resistors;  
3-state

Rev. 6 — 3 November 2011

Product data sheet

## 1. General description

The 74ABT162244 high-performance Bipolar CMOS (BiCMOS) device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT162244 is a 16-bit buffer that is ideal for driving bus lines. The device features four output enable inputs ( $1\overline{OE}$ ,  $2\overline{OE}$ ,  $3\overline{OE}$ ,  $4\overline{OE}$ ), each controlling four of the 3-state outputs.

The 74ABT162244 is designed with 30  $\Omega$  series resistance in both the upper and lower output structures. This design reduces line noise in applications such as memory address drivers, clock drivers and bus receivers/transmitters.

## 2. Features and benefits

- 16-bit bus interface
- Multiple  $V_{CC}$  and GND pins minimize switching noise
- Power-up 3-state
- 3-state buffers
- Output capability: +12 mA and -32 mA
- Live insertion and extraction permitted
- Latch-up performance: JESD 78 Class II
- ESD protection:
  - ◆ HBM JESD-A114E exceeds 2000 V
  - ◆ CDM JESD 22-C101-C exceeds 1000 V

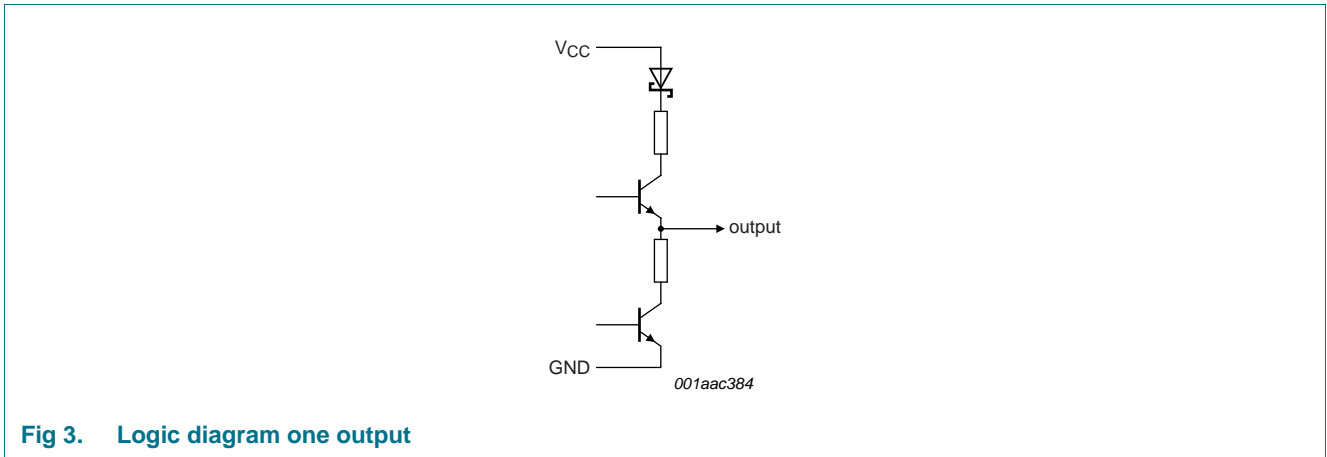
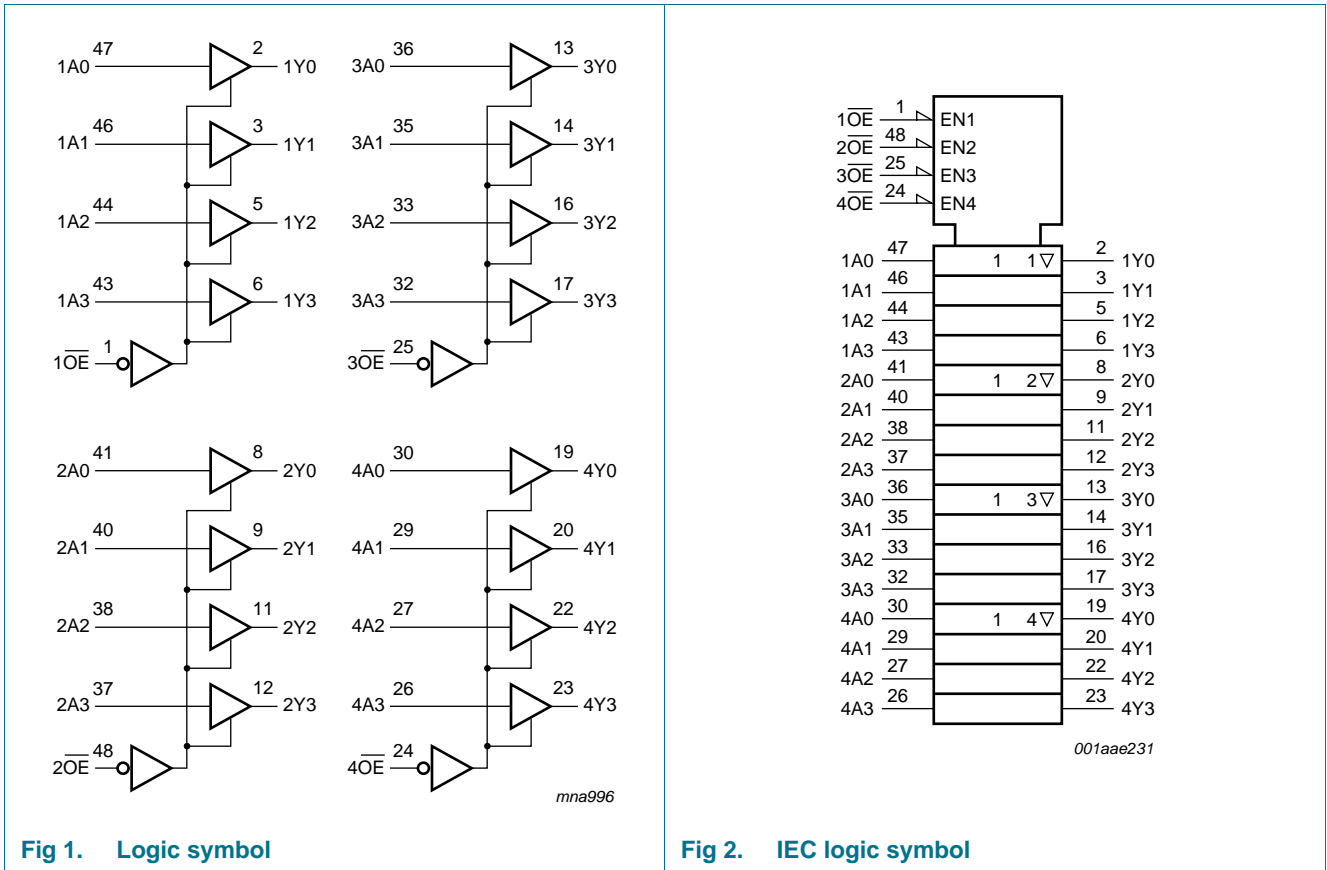
## 3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74ABT162244DGG	-40 °C to +85 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1
74ABT162244DL	-40 °C to +85 °C	SSOP48	plastic shrink small outline package; 48 leads; body width 7.5 mm	SOT370-1



4. Functional diagram



## 5. Pinning information

### 5.1 Pinning

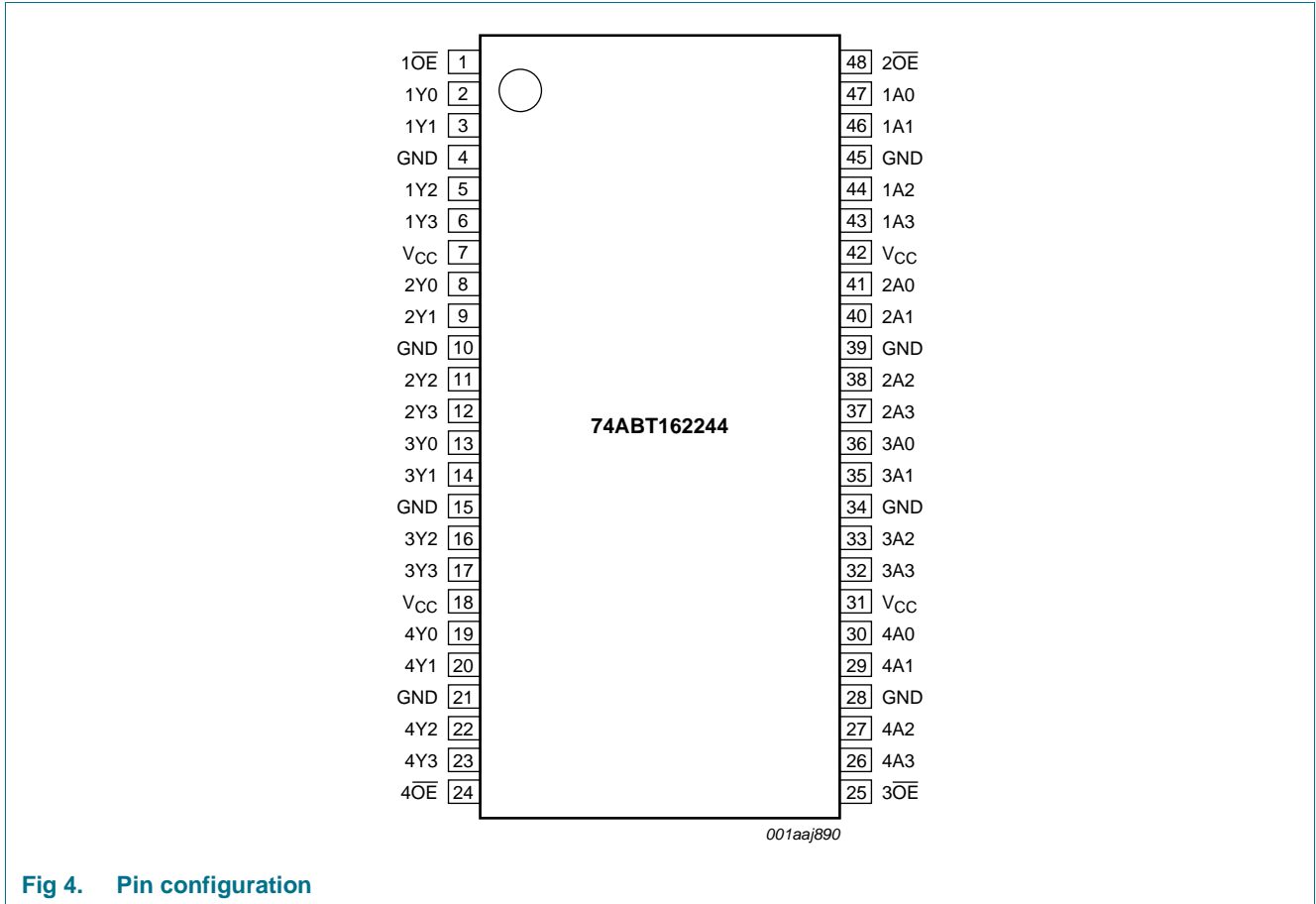


Fig 4. Pin configuration

### 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1OE	1	1 output enable (LOW active)
1Y[0:3]	2, 3, 5, 6	1 data output 0 to output 3
GND	4	ground (0 V)
VCC	7	supply voltage
2Y[0:3]	8, 9, 11, 12	2 data output 0 to output 3
GND	10	ground (0 V)
3Y[0:3]	13, 14, 16, 17	3 data output 0 to output 3
GND	15	ground (0 V)
VCC	18	supply voltage
4Y[0:3]	19, 20, 22, 23	4 data output 0 to output 3
GND	21	ground (0 V)
4OE	24	4 output enable (LOW active)

Table 2. Pin description ...continued

Symbol	Pin	Description
$\overline{3OE}$	25	3 output enable (LOW active)
GND	28	ground (0 V)
4A[0:3]	30, 29, 27, 26	4 data input 0 to input 3
V <sub>CC</sub>	31	supply voltage
GND	34	ground (0 V)
3A[0:3]	36, 35, 33, 32	3 data input 0 to input 3
GND	39	ground (0 V)
2A[0:3]	41, 40, 38, 37	2 data input 0 to input 3
V <sub>CC</sub>	42	supply voltage
GND	45	ground (0 V)
1A[0:3]	47, 46, 44, 43	1 data input 0 to input 3
$\overline{2OE}$	48	2 output enable (LOW active)

## 6. Functional description

Table 3. Function table<sup>[1]</sup>

Control	Input	Output
$\overline{\text{nOE}}$	nAn	nYn
L	L	L
L	H	H
H	X	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7.0	V
$V_I$	input voltage		<sup>[1]</sup> -1.2	+7.0	V
$V_O$	output voltage	output in OFF-state or HIGH-state	<sup>[1]</sup> -0.5	+5.5	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-18	-	mA
$I_{OK}$	output clamping current	$V_O < 0$ V	-50	-	mA
$I_O$	output current	output in LOW-state	-	128	mA
		output in HIGH-state	-	-64	mA
$T_j$	junction temperature		<sup>[2]</sup> -	150	$^{\circ}\text{C}$
$T_{stg}$	storage temperature		-65	+150	$^{\circ}\text{C}$

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

## 8. Recommended operating conditions

Table 5. Operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage		4.5	-	5.5	V
$V_I$	input voltage		0	-	$V_{CC}$	V
$V_{IH}$	HIGH-level input voltage		2.0	-	-	V
$V_{IL}$	LOW-level Input voltage		-	-	0.8	V
$I_{OH}$	HIGH-level output current		-32	-	-	mA
$I_{OL}$	LOW-level output current		-	-	12	mA
$\Delta t/\Delta V$	input transition rise and fall rate		-	-	10	ns/V
$T_{amb}$	ambient temperature	in free air	-40	-	+85	$^{\circ}\text{C}$

## 9. Static characteristics

Table 6. Static characteristics

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		Unit	
			Min	Typ	Max	Min	Max		
V <sub>IK</sub>	input clamping voltage	V <sub>CC</sub> = 4.5 V; I <sub>IK</sub> = -18 mA	-	-0.9	-1.2	-	-1.2	V	
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>							
		V <sub>CC</sub> = 4.5 V; I <sub>OH</sub> = -3 mA	2.5	2.9	-	2.5	-	V	
		V <sub>CC</sub> = 5.0 V; I <sub>OH</sub> = -3 mA	3.0	3.4	-	3.0	-	V	
		V <sub>CC</sub> = 4.5 V; I <sub>OH</sub> = -32 mA	2.0	2.4	-	2.0	-	V	
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>							
		V <sub>CC</sub> = 4.5 V; I <sub>OL</sub> = 8 mA	-	-	0.65	-	0.65	V	
		V <sub>CC</sub> = 4.5 V; I <sub>OL</sub> = 12 mA	-	-	0.80	-	0.80	V	
I <sub>I</sub>	input leakage current	V <sub>CC</sub> = 5.5 V; V <sub>I</sub> = V <sub>CC</sub> or GND	-	±0.01	±1.0	-	±1.0	μA	
I <sub>OFF</sub>	power-off leakage current	V <sub>CC</sub> = 0 V; V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V	-	±5.0	±100	-	±100	μA	
I <sub>O(pu/pd)</sub>	power-up/power-down output current	V <sub>CC</sub> = 2.0 V; V <sub>O</sub> = 0.5 V; V <sub>I</sub> = GND or V <sub>CC</sub> ; nOE = HIGH	[1]	±5.0	±50	-	±50	μA	
I <sub>OZ</sub>	OFF-state output current	V <sub>CC</sub> = 5.5 V; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>							
		output HIGH-state at V <sub>O</sub> = 5.5 V	-	0.1	10	-	10	μA	
		output LOW-state at V <sub>O</sub> = 0 V	-	-0.1	-10	-	-10	μA	
I <sub>LO</sub>	output leakage current	HIGH-state; V <sub>O</sub> = 5.5 V; V <sub>CC</sub> = 5.5 V; V <sub>I</sub> = GND or V <sub>CC</sub>	-	5.0	50	-	50	μA	
I <sub>O</sub>	output current	V <sub>CC</sub> = 5.5 V; V <sub>O</sub> = 2.5 V	[2]	-50	-100	-180	-50	-180	mA
I <sub>CC</sub>	supply current	V <sub>CC</sub> = 5.5 V; V <sub>I</sub> = GND or V <sub>CC</sub>							
		outputs HIGH-state	-	0.50	1.0	-	1.0	mA	
		outputs LOW-state	-	10	19	-	19	mA	
		outputs 3-state	-	0.50	1.0	-	1.0	mA	
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>CC</sub> = 5.5 V; one input at 3.4 V and other inputs at V <sub>CC</sub> or GND	[3][4]	-	100	250	-	250	μA
C <sub>I</sub>	input capacitance	V <sub>I</sub> = 0 V or V <sub>CC</sub>	-	3	-	-	-	pF	
C <sub>I/O</sub>	input/output capacitance	outputs disabled; V <sub>O</sub> = 0 V or V <sub>CC</sub>	-	7	-	-	-	pF	

[1] This parameter is valid for any V<sub>CC</sub> between 0 V and 2.1 V, with a transition time of up to 10 ms. From V<sub>CC</sub> = 2.1 V to V<sub>CC</sub> = 5 V ± 10 %, a transition time of up to 100 μs is permitted.

[2] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

[3] This is the increase in supply current for each input at 3.4 V.

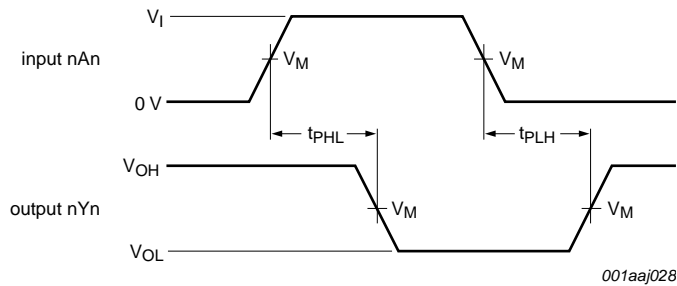
[4] This data sheet limit may vary among suppliers.

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**  
*GND = 0 V. For test circuit, see [Figure 7](#).*

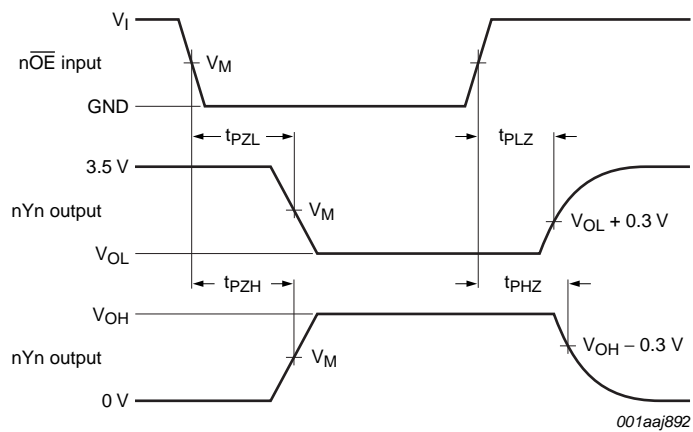
Symbol	Parameter	Conditions	25 °C; V <sub>CC</sub> = 5.0 V			–40 °C to +85 °C; V <sub>CC</sub> = 5.0 V $\pm$ 0.5 V		Unit
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub>	LOW to HIGH propagation delay	nAn to nYn, see <a href="#">Figure 5</a>	1.0	1.8	2.4	1.0	2.7	ns
t <sub>PHL</sub>	HIGH to LOW propagation delay	nAn to nYn, see <a href="#">Figure 5</a>	1.6	3.2	4.0	1.6	4.4	
t <sub>PZH</sub>	OFF-state to HIGH propagation delay	n $\overline{\text{OE}}$ to nYn; see <a href="#">Figure 6</a>	1.2	2.7	3.5	1.2	4.3	ns
t <sub>PZL</sub>	OFF-state to LOW propagation delay	n $\overline{\text{OE}}$ to nYn; see <a href="#">Figure 6</a>	2.6	5.0	6.2	2.6	7.3	ns
t <sub>PHZ</sub>	HIGH to OFF-state propagation delay	n $\overline{\text{OE}}$ to nYn; see <a href="#">Figure 6</a>	1.5	3.0	3.8	1.5	4.5	ns
t <sub>PLZ</sub>	LOW to OFF-state propagation delay	n $\overline{\text{OE}}$ to nYn; see <a href="#">Figure 6</a>	1.3	2.6	3.3	1.3	4.6	ns

11. Waveforms



$V_M = 1.5\text{ V}$   
 $V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig 5. Input (nAn) to output (nYn) propagation delay**

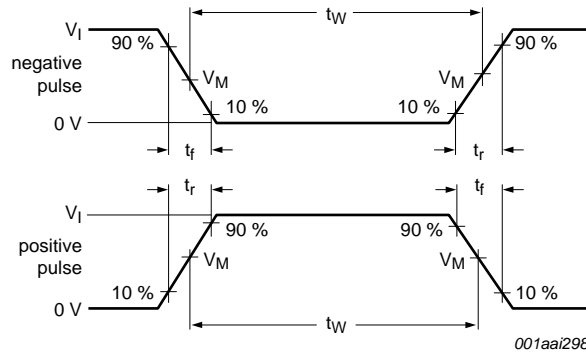


$V_M = 1.5\text{ V}$   
 $V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

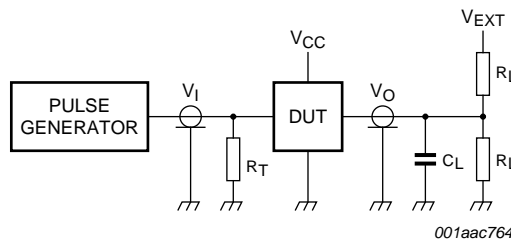
**Fig 6. 3-state output enable and disable times**



12. Test information



$V_M = 1.5\text{ V}$   
 a. Input pulse definition



Test data is given in [Table 8](#).

Definitions test circuit:

$R_L$  = Load resistance.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

b. Test circuit for 3-state outputs

Fig 7. Load circuitry for switching times

Table 8. Test data

Input				Load		$V_{EXT}$		
$V_I$	$f_i$	$t_w$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHZ}, t_{PZH}$	$t_{PLZ}, t_{PZL}$	$t_{PLH}, t_{PHL}$
3.0 V	1 MHz	500 ns	2.5 ns	50 pF	500 Ω	open	7.0 V	open

13. Package outline

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1

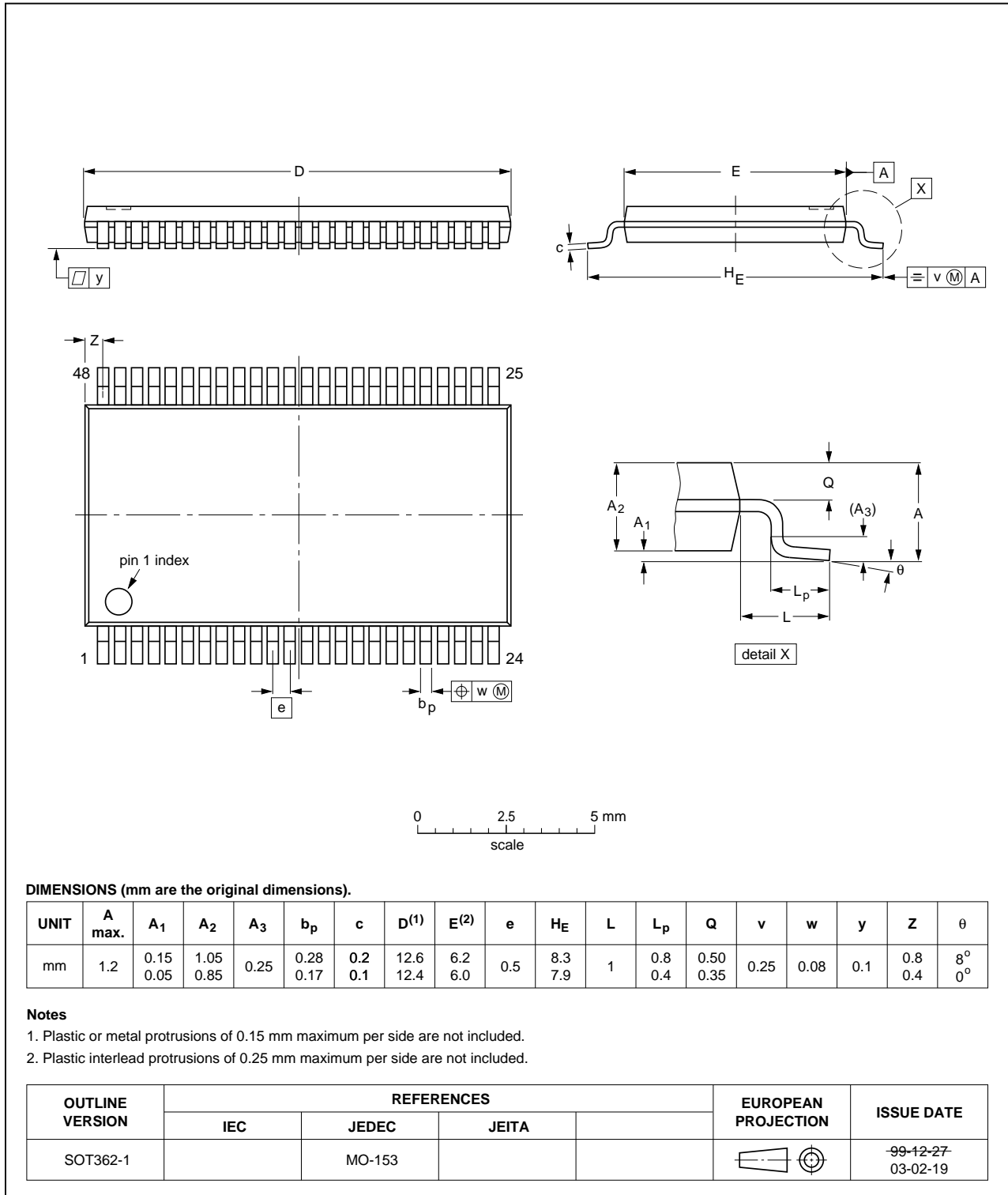


Fig 8. Package outline SOT362-1 (TSSOP48)

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm

SOT370-1

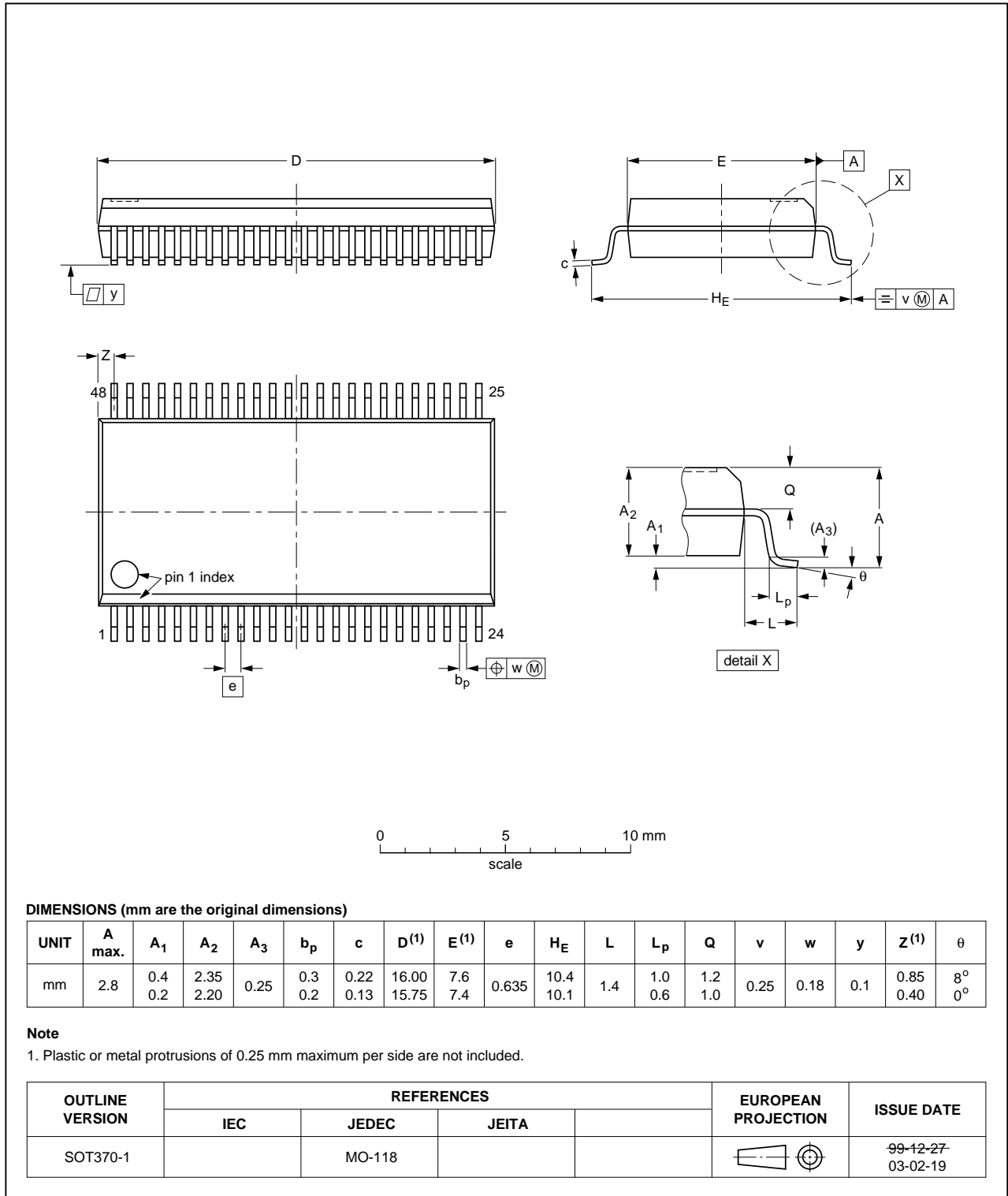


Fig 9. Package outline SOT370-1 (SSOP48)

## 14. Abbreviations

Table 9. Abbreviations

Acronym	Description
CDM	Charged Device Model
ESD	ElectroStatic Discharge
HBM	Human Body Model

## 15. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ABT162244 v.6	20111103	Product data sheet	-	74ABT162244 v.5
Modifications:	<ul style="list-style-type: none"> <li>Legal pages updated</li> </ul>			
74ABT162244 v.5	20100525	Product data sheet	-	74ABT162244 v.4
74ABT162244 v.4	20090409	Product data sheet	-	74ABT_H162244 v.3
74ABT_H162244 v.3	19981022	Product specification	-	74ABT_H162244 v.2
74ABT_H162244 v.2	19980225	Product specification	-	74ABT_H162244 v.1
74ABT_H162244 v.1	19961023	Product specification	-	-

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Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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## 18. Contents

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<b>1</b>	<b>General description</b> .....	<b>1</b>
<b>2</b>	<b>Features and benefits</b> .....	<b>1</b>
<b>3</b>	<b>Ordering information</b> .....	<b>1</b>
<b>4</b>	<b>Functional diagram</b> .....	<b>2</b>
<b>5</b>	<b>Pinning information</b> .....	<b>3</b>
5.1	Pinning .....	3
5.2	Pin description .....	3
<b>6</b>	<b>Functional description</b> .....	<b>5</b>
<b>7</b>	<b>Limiting values</b> .....	<b>5</b>
<b>8</b>	<b>Recommended operating conditions</b> .....	<b>5</b>
<b>9</b>	<b>Static characteristics</b> .....	<b>6</b>
<b>10</b>	<b>Dynamic characteristics</b> .....	<b>7</b>
<b>11</b>	<b>Waveforms</b> .....	<b>8</b>
<b>12</b>	<b>Test information</b> .....	<b>9</b>
<b>13</b>	<b>Package outline</b> .....	<b>10</b>
<b>14</b>	<b>Abbreviations</b> .....	<b>12</b>
<b>15</b>	<b>Revision history</b> .....	<b>12</b>
<b>16</b>	<b>Legal information</b> .....	<b>13</b>
16.1	Data sheet status .....	13
16.2	Definitions .....	13
16.3	Disclaimers .....	13
16.4	Trademarks .....	14
<b>17</b>	<b>Contact information</b> .....	<b>14</b>
<b>18</b>	<b>Contents</b> .....	<b>15</b>

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