

74ABT541

Octal buffer/line driver; 3-state

Rev. 3 — 11 August 2014

Product data sheet

1. General description

The 74ABT541 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT541 device is an octal buffer that is ideal for driving bus lines. The outputs are all capable of sinking 64 mA and sourcing 32 mA. The device features input and outputs on opposite sides of the package to facilitate printed circuit board layout.

2. Features and benefits

- Octal bus interface
- Functions similar to the 74ABT241
- Provides ideal interface and increases fan-out of MOS microprocessors
- Efficient pinout to facilitate PC board layout
- 3-State buffer outputs sink 64 mA and source 32 mA
- Live insertion/extraction permitted
- Power-up 3-state
- Latch-up protection exceeds 500 mA per JESD78 class II level A
- ESD protection:
 - ◆ HBM JESD22-A114E exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V

3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74ABT541N	−40 °C to +85 °C	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
74ABT541D	−40 °C to +85 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74ABT541DB	−40 °C to +85 °C	SSOP20	plastic shrink small outline package; 20 leads; body width 5.3 mm	SOT339-1
74ABT541PW	−40 °C to +85 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1



4. Functional diagram

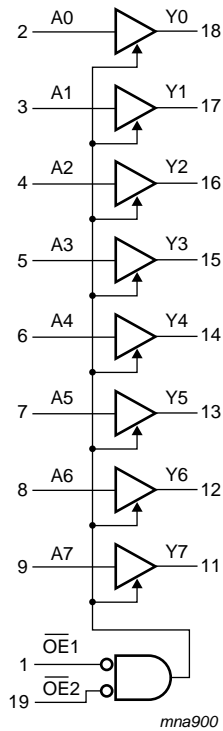


Fig 1. Logic symbol

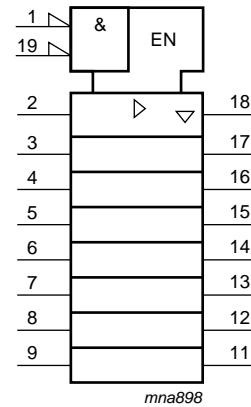


Fig 2. IEC logic symbol

5. Pinning information

5.1 Pinning

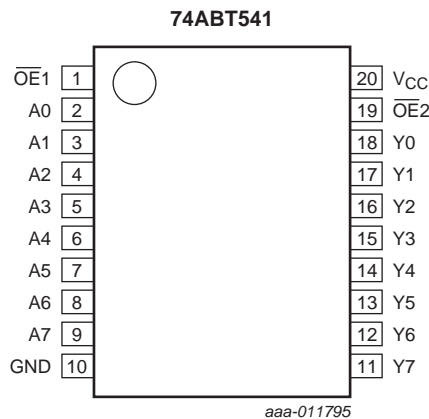


Fig 3. Pin configuration for SO20 and (T)SSOP20

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{OE}1, \overline{OE}2$	1, 19	output enable input (active LOW)
A[0:7]	2, 3, 4, 5, 6, 7, 8, 9	data input
GND	10	ground (0 V)
Y[0:7]	18, 17, 16, 15, 14, 13, 12, 11	data output
V _{CC}	20	supply voltage

6. Functional description

Table 3. Functional table^[1]

Control		Input	Output
$\overline{OE}1$	$\overline{OE}2$	A _n	Y _n
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values^[3]

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7.0	V
V _I	input voltage		^[1] -1.2	+7.0	V
V _O	output voltage	output in OFF-state or HIGH-state	^[2] -0.5	+5.5	V
I _{IK}	input clamping current	V _I < 0 V	-18	-	mA
I _{OK}	output clamping current	V _O < 0 V	-50	-	mA
I _O	output current	output in LOW-state	-	128	mA
T _j	junction temperature		^[3] -	150	°C
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +85 °C	^[4] -	500	mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

[4] For SO20 packages: above 70 °C the value of P_{tot} derates linearly with 8 mW/K.
For (T)SSOP20 packages: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.

8. Recommended operating conditions

Table 5. Operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.5	-	5.5	V
V_I	input voltage		0	-	V_{CC}	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
I_{OH}	HIGH-level output current		-32	-	-	mA
I_{OL}	LOW-level output current		-	-	64	mA
$\Delta t/\Delta V$	input transition rise and fall rate		0	-	5	ns/V
T_{amb}	ambient temperature	in free air	-40	-	+85	°C

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
V_{IK}	input clamping voltage	$V_{CC} = 4.5 \text{ V}$; $I_{IK} = -18 \text{ mA}$	-	-0.9	-1.2	-	-1.2	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IL}$ or V_{IH}						
		$V_{CC} = 4.5 \text{ V}$; $I_{OH} = -3 \text{ mA}$	2.5	2.9	-	2.5	-	V
		$V_{CC} = 5.0 \text{ V}$; $I_{OH} = -3 \text{ mA}$	3.0	3.4	-	3.0	-	V
		$V_{CC} = 4.5 \text{ V}$; $I_{OH} = -32 \text{ mA}$	2.0	2.4	-	2.0	-	V
V_{OL}	LOW-level output voltage	$V_{CC} = 4.5 \text{ V}$; $I_{OL} = 64 \text{ mA}$; $V_I = V_{IL}$ or V_{IH}	-	0.42	0.55	-	0.55	V
I_I	input leakage current	$V_{CC} = 5.5 \text{ V}$; $V_I = \text{GND}$ or 5.5 V	-	± 0.01	± 1.0	-	± 1.0	μA
I_{OFF}	power-off leakage current	$V_{CC} = 0.0 \text{ V}$; V_I or $V_O \leq 4.5 \text{ V}$	-	± 5.0	± 100	-	± 100	μA
$I_{O(pu/pd)}$	power-up/power-down output current	$V_{CC} = 2.0 \text{ V}$; $V_O = 0.5 \text{ V}$; $V_I = \text{GND}$ or V_{CC} ; $\overline{\text{OE}} = \text{don't care}$ ^[1]	-	± 5.0	± 50	-	± 50	μA
I_{OZ}	OFF-state output current	$V_{CC} = 5.5 \text{ V}$; $V_I = V_{IL}$ or V_{IH}						
		$V_O = 2.7 \text{ V}$	-	5.0	50	-	50	μA
		$V_O = 0.5 \text{ V}$	-	-5.0	-50	-	-50	μA
I_{LO}	output leakage current	HIGH-state; $V_O = 5.5 \text{ V}$; $V_{CC} = 5.5 \text{ V}$; $V_I = \text{GND}$ or V_{CC}	-	5.0	50	-	50	μA
I_O	output current	$V_{CC} = 5.5 \text{ V}$; $V_O = 2.5 \text{ V}$ ^[2]	-40	-100	-180	-40	-180	mA
I_{CC}	supply current	$V_{CC} = 5.5 \text{ V}$; $V_I = \text{GND}$ or V_{CC}						
		outputs HIGH-state	-	0.5	250	-	250	μA
		outputs LOW-state	-	24	30	-	30	mA
		outputs disabled	-	0.5	250	-	250	μA

Table 6. Static characteristics ...continued

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
ΔI_{CC}	additional supply current	per input pin; output enabled; $V_{CC} = 5.5\text{ V}$; one input at 3.4 V, other inputs at V_{CC} or GND ^[3]	-	0.5	1.5	-	1.5	mA
		per input pin; output disabled; $V_{CC} = 5.5\text{ V}$; one data input at 3.4 V, other inputs at V_{CC} or GND	-	0.5	50	-	50	μA
		per input pin; output disabled; $V_{CC} = 5.5\text{ V}$; one enable input at 3.4 V, other inputs at V_{CC} or GND	-	0.5	1.5	-	1.5	mA
C_I	input capacitance	$V_I = 0\text{ V}$ or V_{CC}	-	4	-	-	-	pF
C_O	output capacitance	outputs disabled; $V_O = 0\text{ V}$ or V_{CC}	-	7	-	-	-	pF

- [1] This parameter is valid for any V_{CC} between 0 V and 2.1 V, with a transition time of up to 10 ms. From $V_{CC} = 2.1\text{ V}$ to $V_{CC} = 5\text{ V} \pm 10\%$, a transition time of up to 100 μs is permitted.
- [2] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- [3] This is the increase in supply current for each input at 3.4 V.

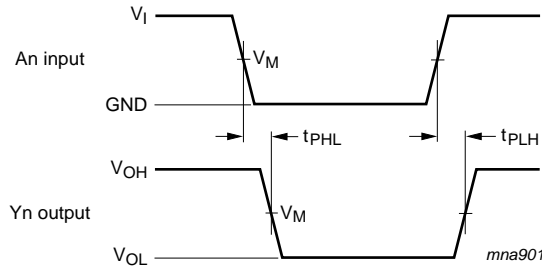
10. Dynamic characteristics

Table 7. Dynamic characteristics

$GND = 0\text{ V}$. Test circuit is shown in [Figure 6](#).

Symbol	Parameter	Conditions	25 °C; $V_{CC} = 5.0\text{ V}$			-40 °C to +85 °C; $V_{CC} = 5.0\text{ V} \pm 0.5\text{ V}$		Unit
			Min	Typ	Max	Min	Max	
t_{PLH}	LOW to HIGH propagation delay	A_n to Y_n , see Figure 4	1.0	2.6	4.1	1.0	4.6	ns
t_{PHL}	HIGH to LOW propagation delay	A_n to Y_n , see Figure 4	1.0	2.9	4.2	1.0	4.6	ns
t_{PZH}	OFF-state to HIGH propagation delay	\overline{OEn} to Y_n ; see Figure 5	1.1	3.1	4.8	1.1	5.3	ns
t_{PZL}	OFF-state to LOW propagation delay	\overline{OEn} to Y_n ; see Figure 5	2.1	4.4	5.9	2.1	6.4	ns
t_{PHZ}	HIGH to OFF-state propagation delay	\overline{OEn} to Y_n ; see Figure 5	2.1	5.1	6.6	2.1	7.1	ns
t_{PLZ}	LOW to OFF-state propagation delay	\overline{OEn} to Y_n ; see Figure 5	1.7	4.7	6.2	1.7	6.7	ns

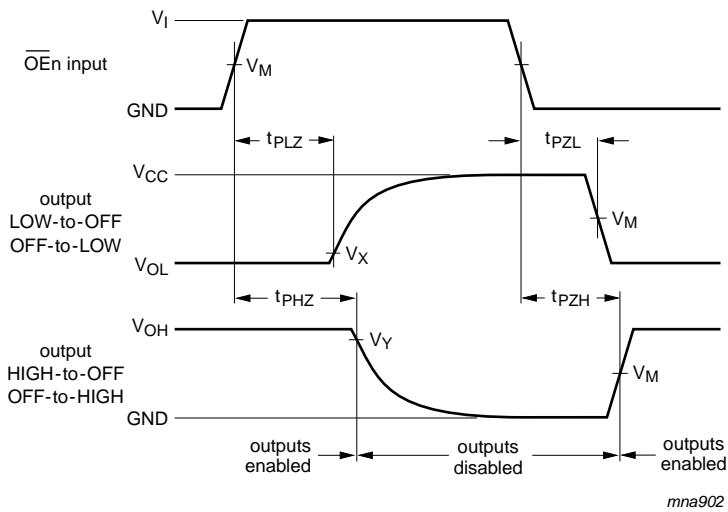
11. AC waveforms



$V_M = 1.5\text{ V}$

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

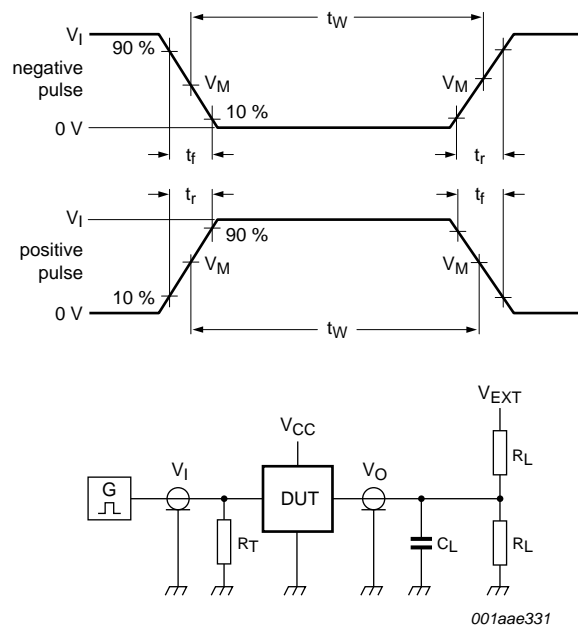
Fig 4. Input (An) to output (Yn) propagation delays



$V_M = 1.5\text{ V}$

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 5. 3-state enable and disable times



Test data is given in [Table 8](#).

Test circuit definitions:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = Test voltage for switching times.

Fig 6. Test circuit for measuring switching times

Table 8. Test data

Input				Load		V_{EXT}		
V_I	f_I	t_W	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
3.0 V	1 MHz	500 ns	≤ 2.5 ns	50 pF	500 Ω	open	open	7.0 V

12. Package outline

DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1

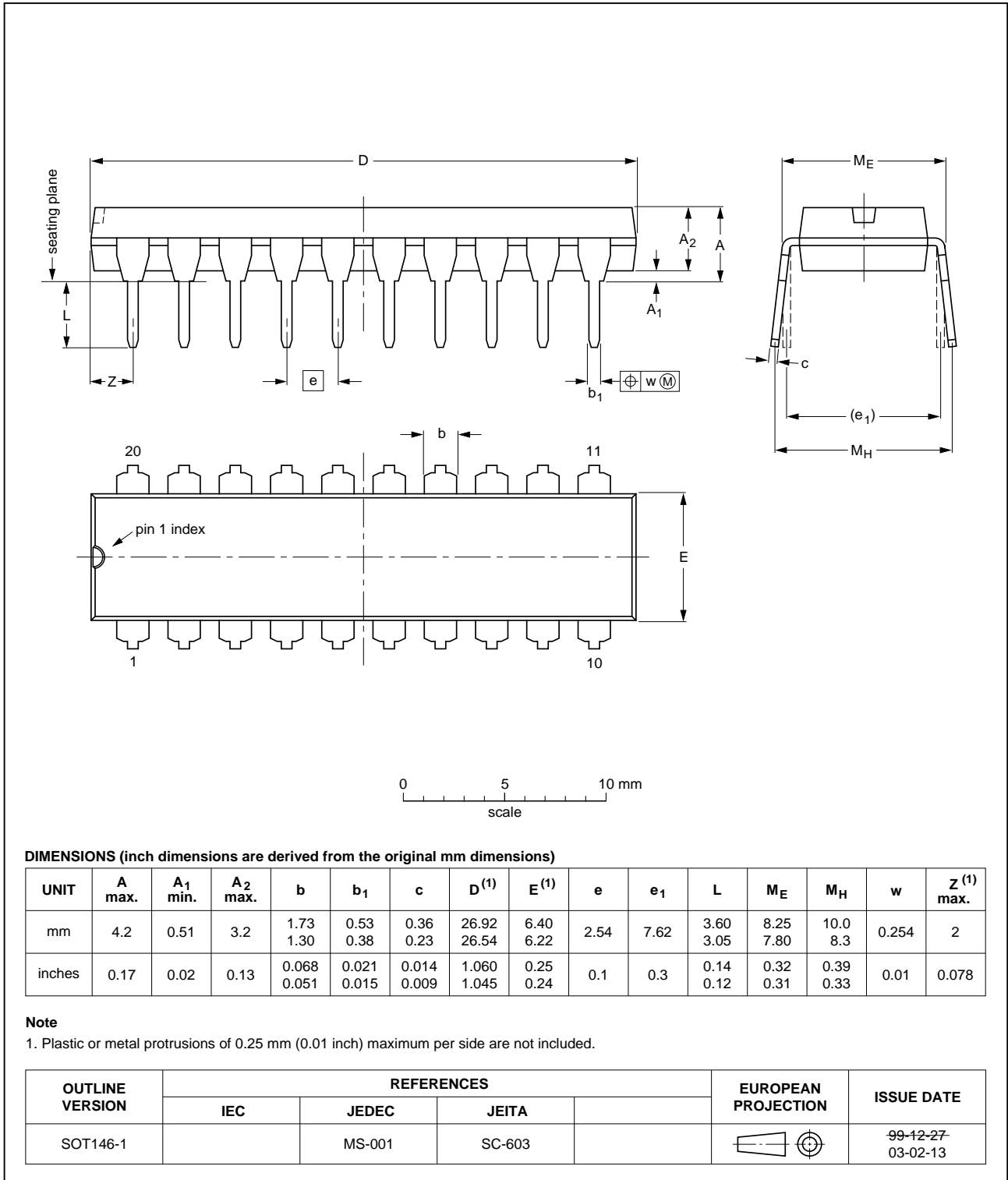


Fig 7. Package outline SOT146-1 (DIP20)

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

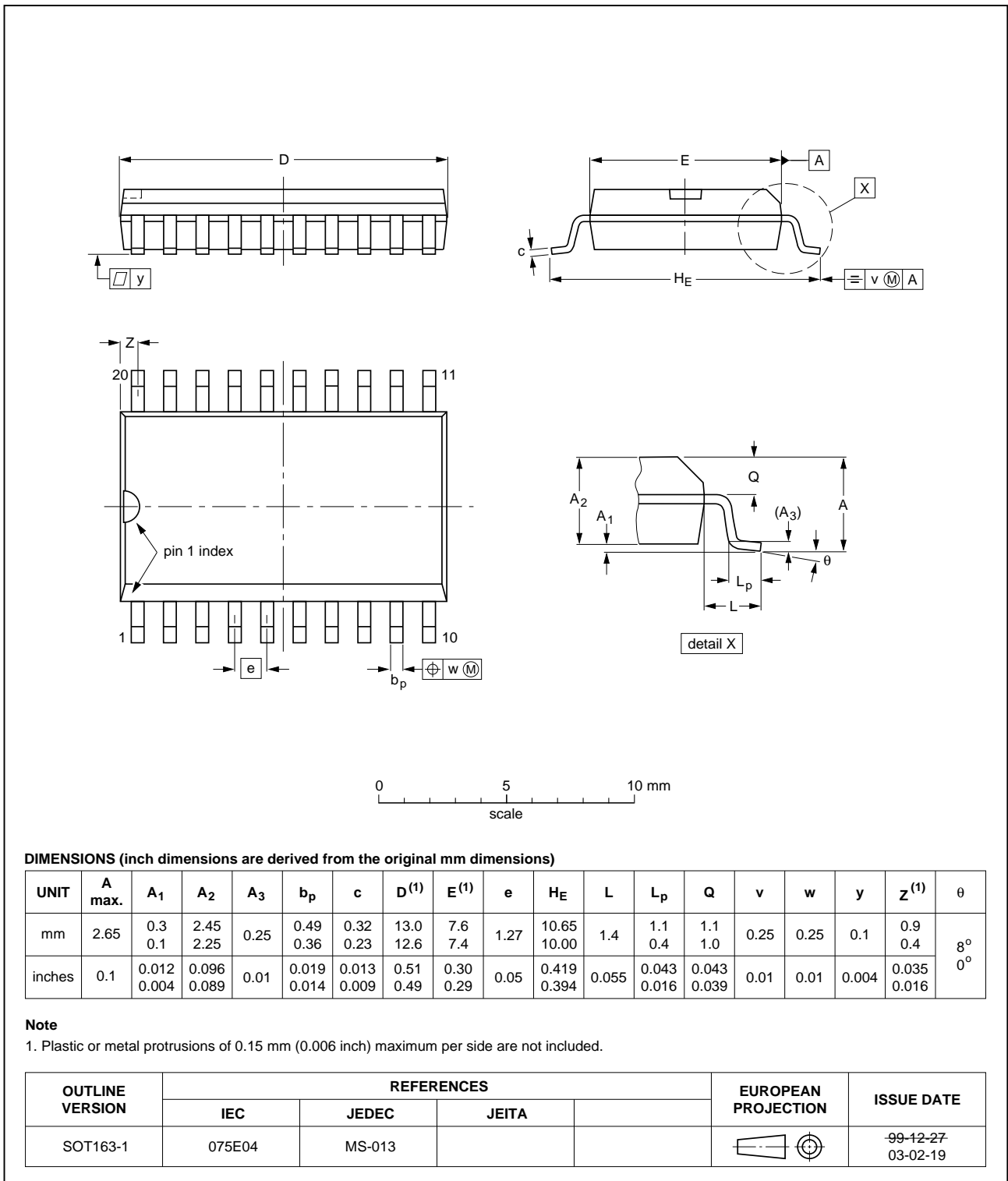


Fig 8. Package outline SOT163-1 (SO20)

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1

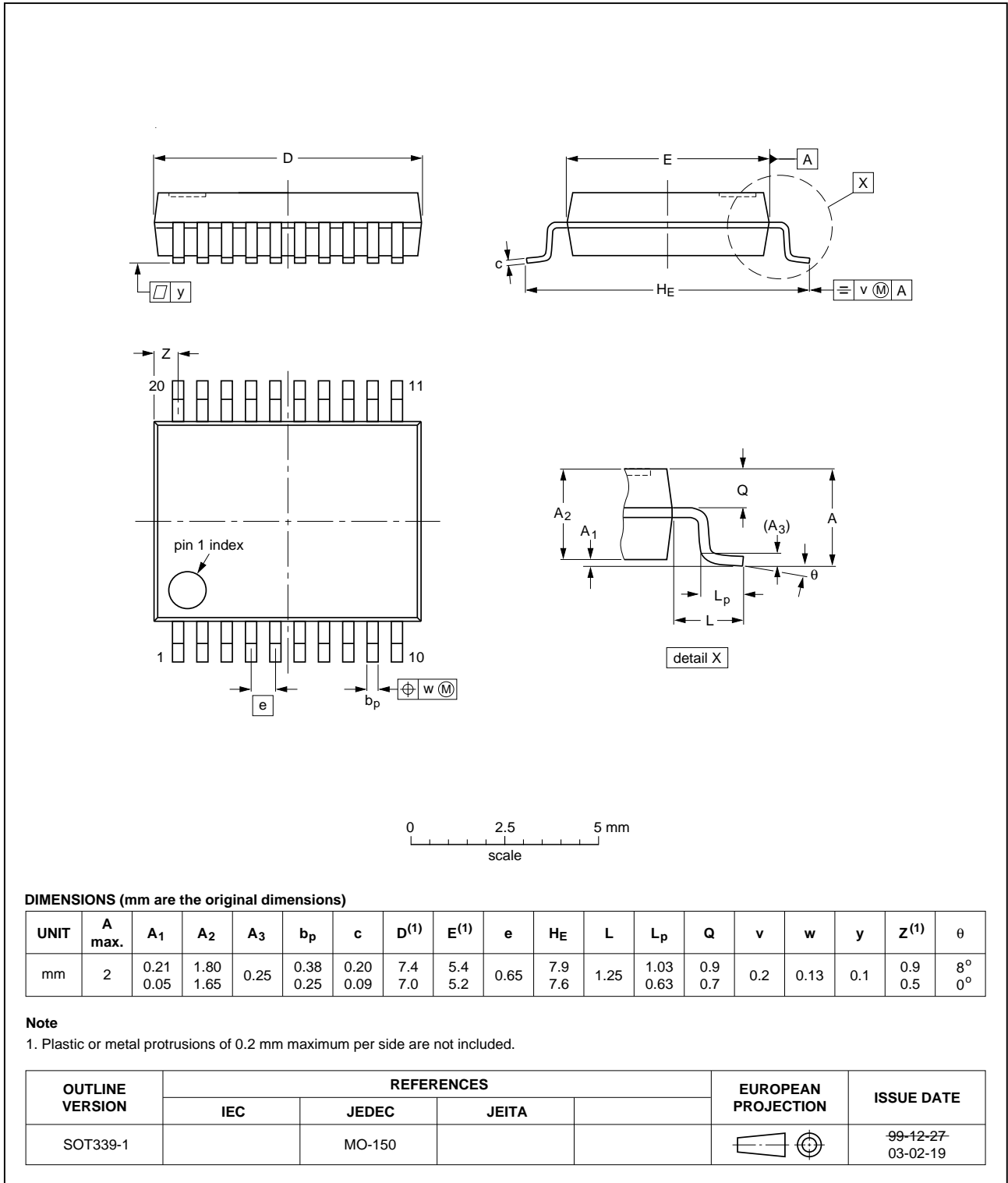


Fig 9. Package outline SOT339-1 (SSOP20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

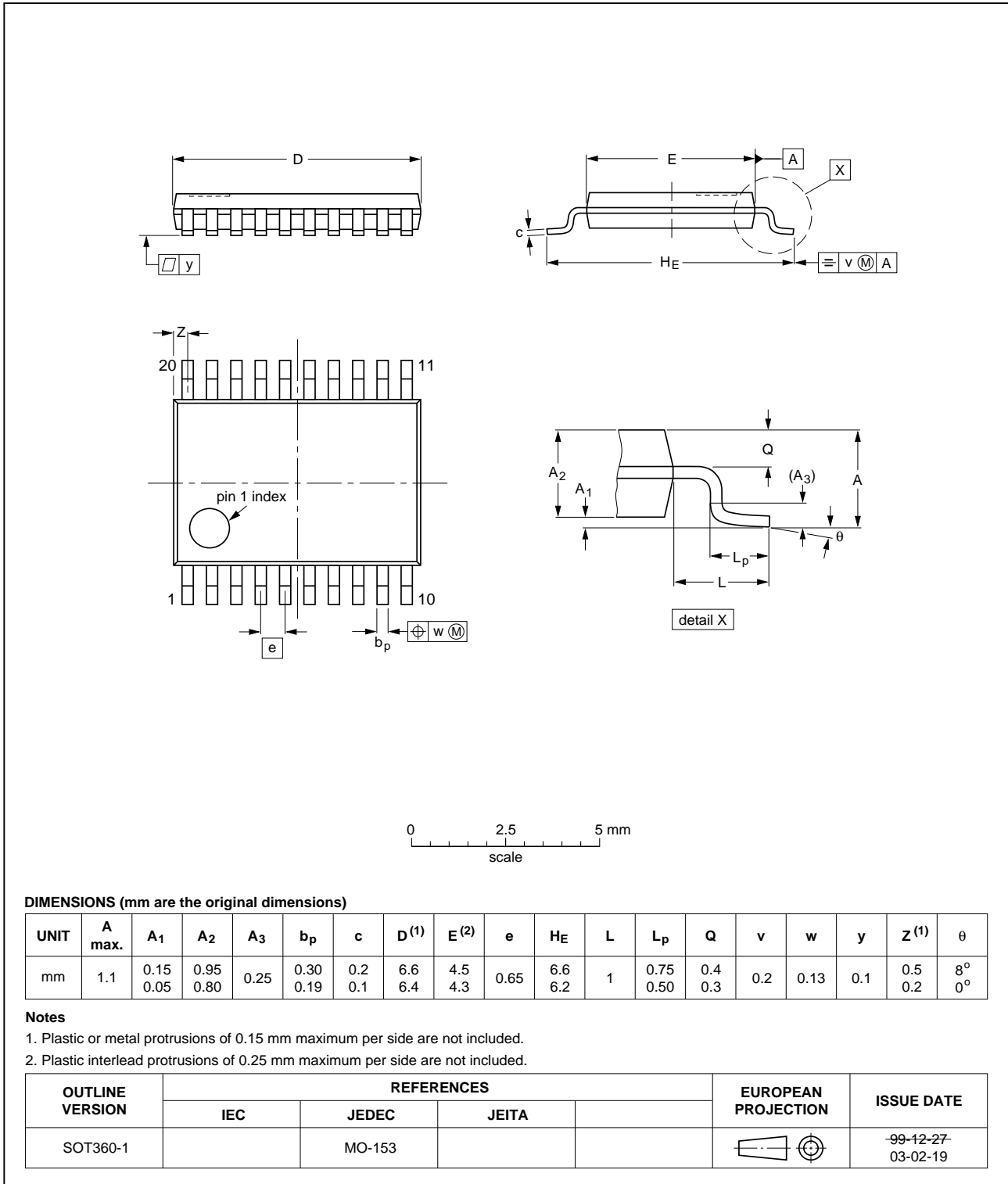


Fig 10. Package outline SOT360-1 (TSSOP20)

13. Abbreviations

Table 9. Abbreviations

Acronym	Description
BiCMOS	Bipolar Complementary Metal-Oxide Semiconductor
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ABT541 v.3	20140811	Product data sheet	-	74ABT541 v.2
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. 			
74ABT541 v.2	19980116	Product specification	-	74ABT541 v.1
74ABT541 v.1	19960110	Product specification	-	-

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Document status ^{[1][2]}	Product status ^[3]	Definition
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Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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