HEF4557B

1-to-64 bit variable length shift register

Rev. 6 — 18 November 2011 **Product data sheet**

1. General description

The HEF4557B is a static clocked serial shift register whose length may be programmed to be any number of bits between 1 and 64. The number of bits selected is equal to the sum of the subscripts of the enabled length control inputs (L1, L2, L4, L8, L16, and L32) plus one. Serial data may be selected from the DA or DB data inputs with the A/$\overline{\text{B}}$ select input. This feature is useful for recirculation purposes. Information on DA or DB is shifted into the first register position and all the data in the register is shifted one position to the right on the LOW to HIGH transition of CP0 while $\overline{\text{CP1}}$ is LOW or on the HIGH to LOW transition of $\overline{\text{CP1}}$ while CP0 is HIGH. A HIGH on master reset (MR) resets the register and forces Q to LOW and $\overline{\text{Q}}$ to HIGH, independent of the other inputs.

It operates over a recommended V_{DD} power supply range of 3 V to 15 V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD}, V_{SS}, or another input.

2. Features and benefits

- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Specified from –40 °C to +85 °C
- Complies with JEDEC standard JESD 13-B

3. Ordering information

Table 1. Ordering information

All types operate from –40 °C to +85 °C

Type number	Package		
	Name	Description	Version
HEF4557BP	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
HEF4557BT	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

4. Functional diagram

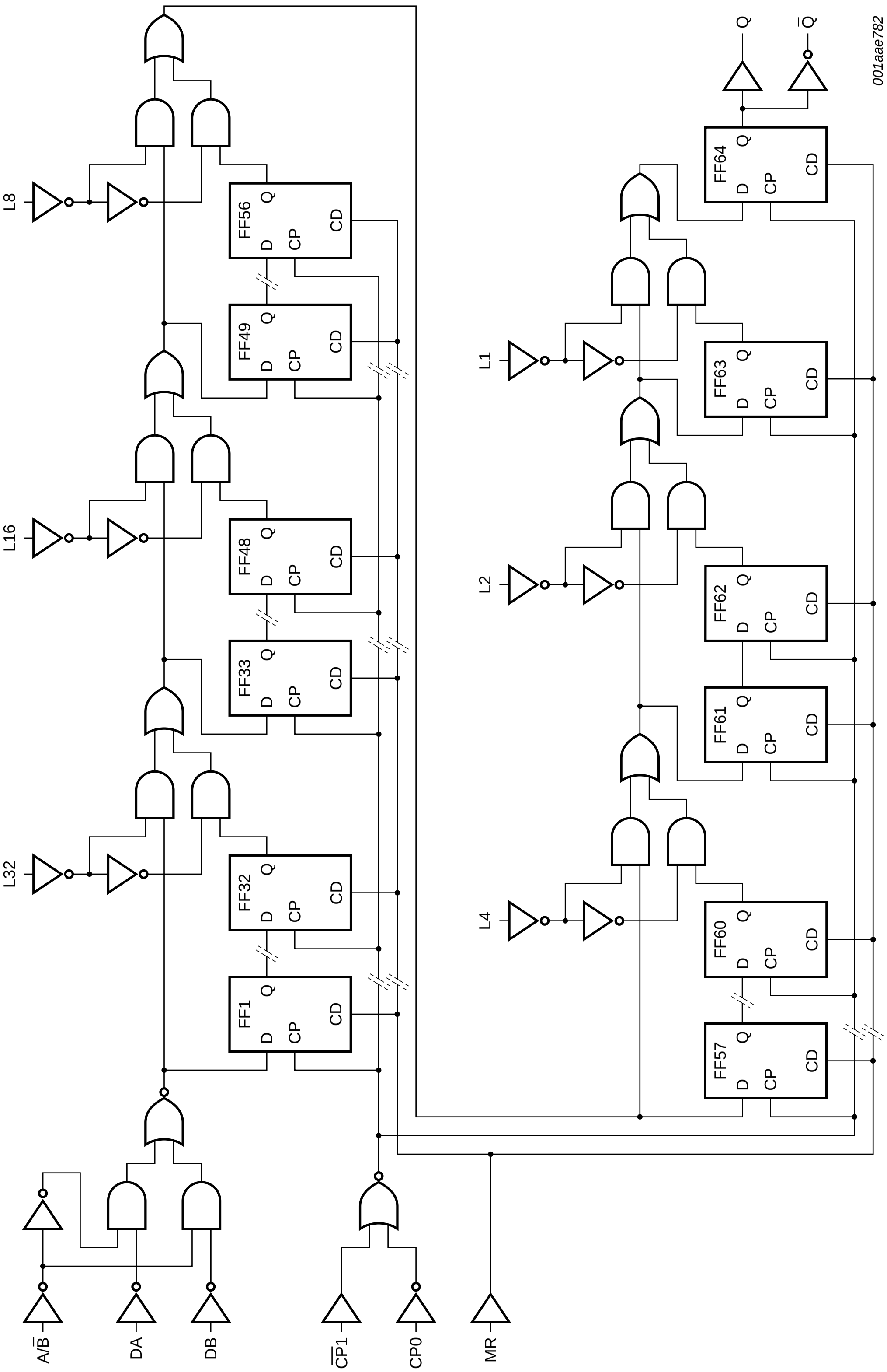


Fig 1. Logic diagram

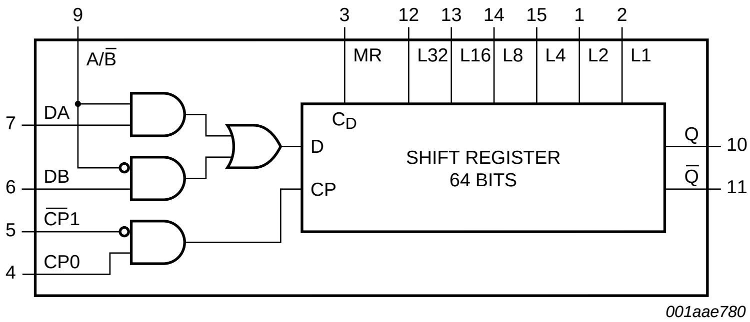


Fig 2. Functional diagram

5. Pinning information

5.1 Pinning

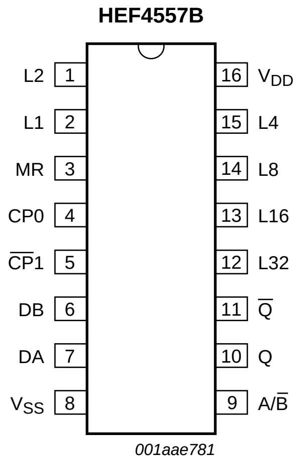


Fig 3. Pin configuration

5.2 Pin description

Table 2. Pin description table

Symbol	Pin	Description
L1, L2, L4, L8, L16, L32	2, 1, 15, 14, 13, 12	bit-length control input
MR	3	asynchronous master reset
CP0	4	clock input
$\overline{CP1}$	5	clock input
DA, DB	7, 6	data input
V_{SS}	8	ground (0 V)
$A/\overline{B}$	9	select data input

Table 2. Pin description table *...continued*

Symbol	Pin	Description
Q	10	buffered output
$\overline{Q}$	11	complementary buffered output
V_{DD}	16	supply voltage

6. Functional description

Table 3. Function table[1]

Inputs						Output
MR	A/$\overline{B}$	DA	DB	CP0	$\overline{CP1}$	Q
L	L	D_1	D_2	↑	L	D_2
L	H	D_1	D_2	↑	L	D_1
L	L	D_1	D_2	H	↓	D_2
L	H	D_1	D_2	H	↓	D_1
H	X	X	X	X	X	L

[1] The moment D_n appears at Q depends on the bit-length shown in Table 4; H = HIGH voltage level; L = LOW voltage level; X = don't care; ↑ = positive-going transition; ↓ = negative-going transition; D_1, D_2 = either HIGH or LOW.

Table 4. Bit-length select function table

L32	L16	L8	L4	L2	L1	Register length
L	L	L	L	L	L	1-bit
L	L	L	L	L	H	2-bits
L	L	L	L	H	L	3-bits
L	L	L	L	H	H	4-bits
L	L	L	H	L	L	5-bits
L	L	L	H	L	H	6-bits
L	L	L	H	H	L	7-bits
L	L	L	H	H	H	8-bits
L1 to L16 continue to increment in a binary count with L32 LOW						
L	H	H	H	H	H	32-bits
H	L	L	L	L	L	33-bits
H	L	L	L	L	H	34-bits
L1 to L16 continue to increment in a binary count with L32 HIGH						
H	H	H	H	L	L	61-bits
H	H	H	H	L	H	62-bits
H	H	H	H	H	L	63-bits
H	H	H	H	H	H	64-bits

7. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			–0.5	+18	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{DD} + 0.5$ V		-	±10	mA
V_I	input voltage			–0.5	V_{DD} + 0.5	V
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{DD} + 0.5$ V		-	±10	mA
$I_{I/O}$	input/output current			-	±10	mA
I_{DD}	supply current			-	50	mA
T_{stg}	storage temperature			–65	+150	°C
T_{amb}	ambient temperature			–40	+85	°C
P_{tot}	total power dissipation	DIP16 package	[1]	-	750	mW
		SO16 package	[2]	-	500	mW
P	power dissipation	per output		-	100	mW

[1] For DIP16 package: P_{tot} derates linearly with 12 mW/K above 70 °C.

[2] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

8. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		3	-	15	V
V_I	input voltage		0	-	V_{DD}	V
T_{amb}	ambient temperature	in free air	–40	-	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{DD} = 5 V	-	-	3.75	μs/V
		V_{DD} = 10 V	-	-	0.5	μs/V
		V_{DD} = 15 V	-	-	0.08	μs/V

9. Static characteristics

Table 7. Static characteristics

V_{SS} = 0 V; V_I = V_{SS} or V_{DD} unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	T_{amb} = −40 °C		T_{amb} = 25 °C		T_{amb} = 85 °C		Unit
				Min	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$\lvert I_O \rvert$ < 1 μA	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
V_{IL}	LOW-level input voltage	$\lvert I_O \rvert$ < 1 μA	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V
V_{OH}	HIGH-level output voltage	$\lvert I_O \rvert$ < 1 μA	5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
V_{OL}	LOW-level output voltage	$\lvert I_O \rvert$ < 1 μA	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V
I_{OH}	HIGH-level output current	V_O = 2.5 V	5 V	-	−1.7	-	−1.4	-	−1.1	mA
		V_O = 4.6 V	5 V	-	−0.52	-	−0.44	-	−0.36	mA
		V_O = 9.5 V	10 V	-	−1.3	-	−1.1	-	−0.9	mA
		V_O = 13.5 V	15 V	-	−3.6	-	−3.0	-	−2.4	mA
I_{OL}	LOW-level output current	V_O = 0.4 V	5 V	0.52	-	0.44	-	0.36	-	mA
		V_O = 0.5 V	10 V	1.3	-	1.1	-	0.9	-	mA
		V_O = 1.5 V	15 V	3.6	-	3.0	-	2.4	-	mA
I_I	input leakage current		15 V	-	±0.3	-	±0.3	-	±1.0	μA
I_{DD}	supply current	I_O = 0 A	5 V	-	50	-	50	-	375	μA
			10 V	-	100	-	100	-	750	μA
			15 V	-	200	-	200	-	1500	μA
C_I	input capacitance		-	-	-	-	7.5	-	-	pF

10. Dynamic characteristics

Table 8. Dynamic characteristics

V_{SS} = 0 V; T_{amb} = 25 °C; for test circuit see Figure 6; unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}		Extrapolation formula	Min	Typ	Max	Unit
t_{PHL}	HIGH to LOW propagation delay	CP0, $\overline{CP1}$ to Q, $\overline{Q}$; see Figure 4	5 V	[1]	213 ns + (0.55 ns/pF)C_L	-	240	480	ns
			10 V		79 ns + (0.23 ns/pF)C_L	-	90	180	ns
			15 V		57 ns + (0.16 ns/pF)C_L	-	65	130	ns
		MR to Q; see Figure 4	5 V		143 ns + (0.55 ns/pF)C_L	-	170	340	ns
			10 V		69 ns + (0.23 ns/pF)C_L	-	80	160	ns
			15 V		52 ns + (0.16 ns/pF)C_L	-	60	120	ns
t_{PLH}	LOW to HIGH propagation delay	CP0, $\overline{CP1}$ to Q, $\overline{Q}$; see Figure 4	5 V	[1]	213 ns + (0.55 ns/pF)C_L	-	240	480	ns
			10 V		79 ns + (0.23 ns/pF)C_L	-	90	180	ns
			15 V		57 ns + (0.16 ns/pF)C_L	-	65	130	ns
		MR to $\overline{Q}$; see Figure 4	5 V		113 ns + (0.55 ns/pF)C_L	-	140	280	ns
			10 V		59 ns + (0.23 ns/pF)C_L	-	70	140	ns
			15 V		47 ns + (0.16 ns/pF)C_L	-	55	110	ns
t_t	transition time	see Figure 4	5 V	[1]	10 ns + (1.00 ns/pF)C_L	-	60	120	ns
			10 V		9 ns + (0.42 ns/pF)C_L	-	30	60	ns
			15 V		6 ns + (0.28 ns/pF)C_L	-	20	40	ns
t_{su}	set-up time	DA, DB, A/$\overline{B}$ to CP0, $\overline{CP1}$; L1 to L32 = LOW; see Figure 5	5 V	[2]		360	180	-	ns
			10 V			140	70	-	ns
			15 V			90	45	-	ns
		DA, DB, A/$\overline{B}$ to CP0, $\overline{CP1}$; L32 = HIGH; see Figure 5	5 V			+40	−20	-	ns
			10 V			+35	−10	-	ns
			15 V			+30	−5	-	ns
t_h	hold time	DA, DB, A/$\overline{B}$ to CP0, $\overline{CP1}$; L1 to L32 = LOW; see Figure 5	5 V	[2]		−40	−110	-	ns
			10 V			−10	−45	-	ns
			15 V			0	−30	-	ns
		DA, DB, A/$\overline{B}$ to CP0, $\overline{CP1}$; L1 to L32 = HIGH; see Figure 5	5 V			90	30	-	ns
			10 V			60	20	-	ns
			15 V			50	15	-	ns
t_W	pulse width	CP0 input LOW; minimum width; see Figure 5	5 V			180	90	-	ns
			10 V			60	30	-	ns
			15 V			40	20	-	ns
		$\overline{CP1}$ input HIGH; minimum width; see Figure 5	5 V			180	90	-	ns
			10 V			60	30	-	ns
			15 V			40	20	-	ns
		MR input HIGH; minimum width; see Figure 5	5 V			150	75	-	ns
			10 V			70	35	-	ns
			15 V			50	25	-	ns

Table 8. Dynamic characteristics *...continued*
V_{SS} = 0 V; T_{amb} = 25 °C; for test circuit see Figure 6; unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	Extrapolation formula	Min	Typ	Max	Unit
t_{rec}	recovery time	MR input; L1 to L32 = LOW; see Figure 5	5 V	[2]	500	250	-	ns
			10 V		250	125	-	ns
			15 V		150	75	-	ns
		MR input; L32 = HIGH	5 V		110	50	-	ns
			10 V		70	30	-	ns
			15 V		60	25	-	ns
f_{max}	maximum frequency	see Figure 5	5 V		2.5	5	-	MHz
			10 V		7	14	-	MHz
			15 V		10	20	-	MHz

[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown (C_L in pF).

[2] The set-up, hold, and recovery times vary with the minimum number of bits selected. For intermediate numbers not specified, interpolate as shown in Table 9.

Table 9. Interpolation table [1]

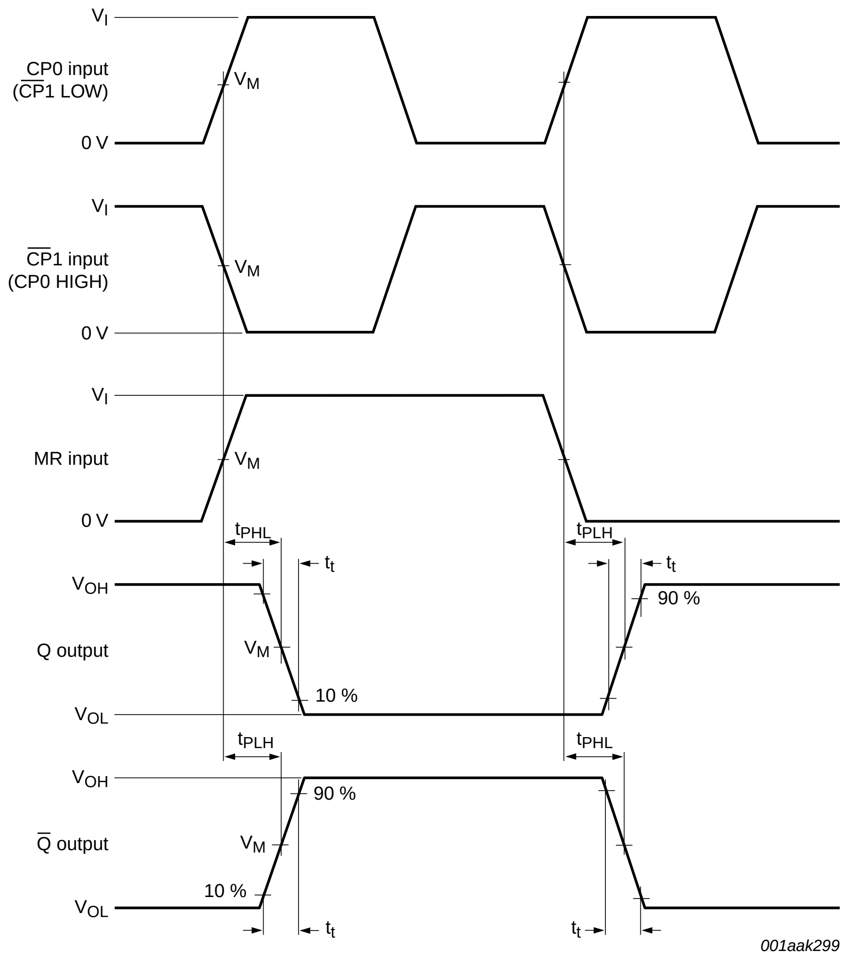
Length control inputs						Minimum number of bits selected	Set-up, hold, and recovery times	Example: t_{rec} minimum, V_{DD} = 5 V
L1	L2	L4	L8	L16	L32			
L	L	L	L	L	L	1	see Table 8	500 ns
H	L	L	L	L	L	2	(interpolate in 6 equal steps)	435 ns
X	H	L	L	L	L	3		370 ns
X	X	H	L	L	L	5		305 ns
X	X	X	H	L	L	9		240 ns
X	X	X	X	H	L	17		175 ns
X	X	X	X	X	H	33	see Table 8	110 ns

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care

Table 10. Dynamic power dissipation P_D
P_D can be calculated from the formulas shown. V_{SS} = 0 V; $t_r = t_f \leq 20$ ns; T_{amb} = 25 °C.

Symbol	Parameter	V_{DD}	Typical formula for P_D (μW)	where:
P_D	dynamic power dissipation	5 V	$P_D = 3500 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	f_i = input frequency in MHz,
		10 V	$P_D = 15000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	f_o = output frequency in MHz,
		15 V	$P_D = 37000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	C_L = output load capacitance in pF,
				V_{DD} = supply voltage in V,
				$\Sigma(f_o \times C_L)$ = sum of the outputs.

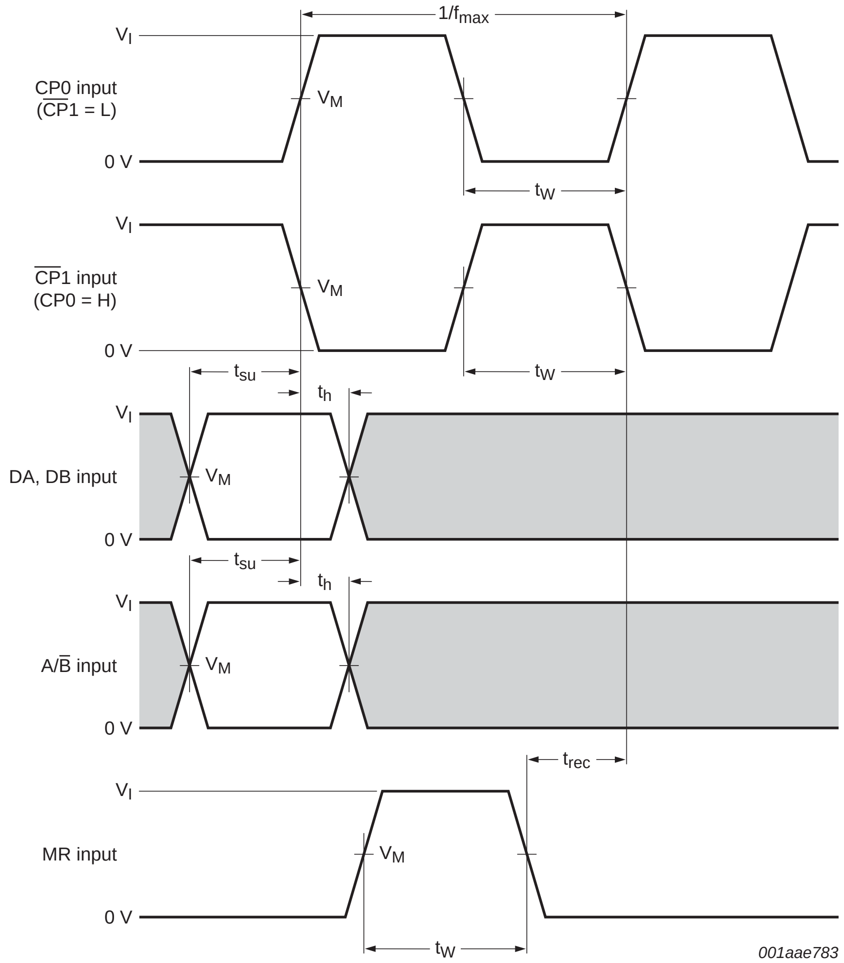
11. Waveforms



For measurement points see Table 11.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 4. Propagation delays

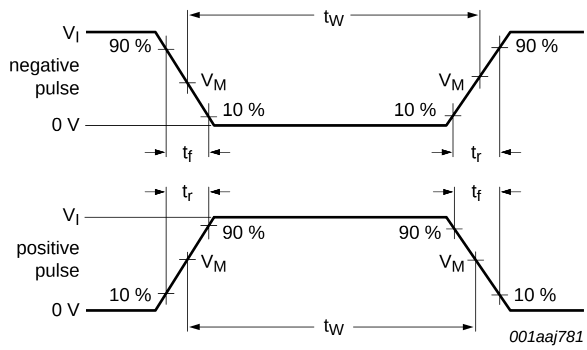


Set-up and hold times are shown as positive values but may be specified as negative values.

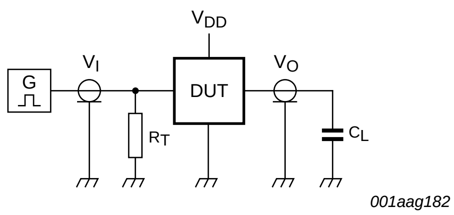
The shaded area indicates where data can change for predictable performance.

For measurement points see Table 11.

Fig 5. Waveforms showing recovery time for MR and minimum CP0, CP1, and MR pulse widths, set-up and hold times for DA, DB, and A/B to CP0 and CP1



a. Input waveforms



b. Test circuit

Test data is given in Table 11.

Definitions for test circuit:

Device Under Test (DUT)

C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

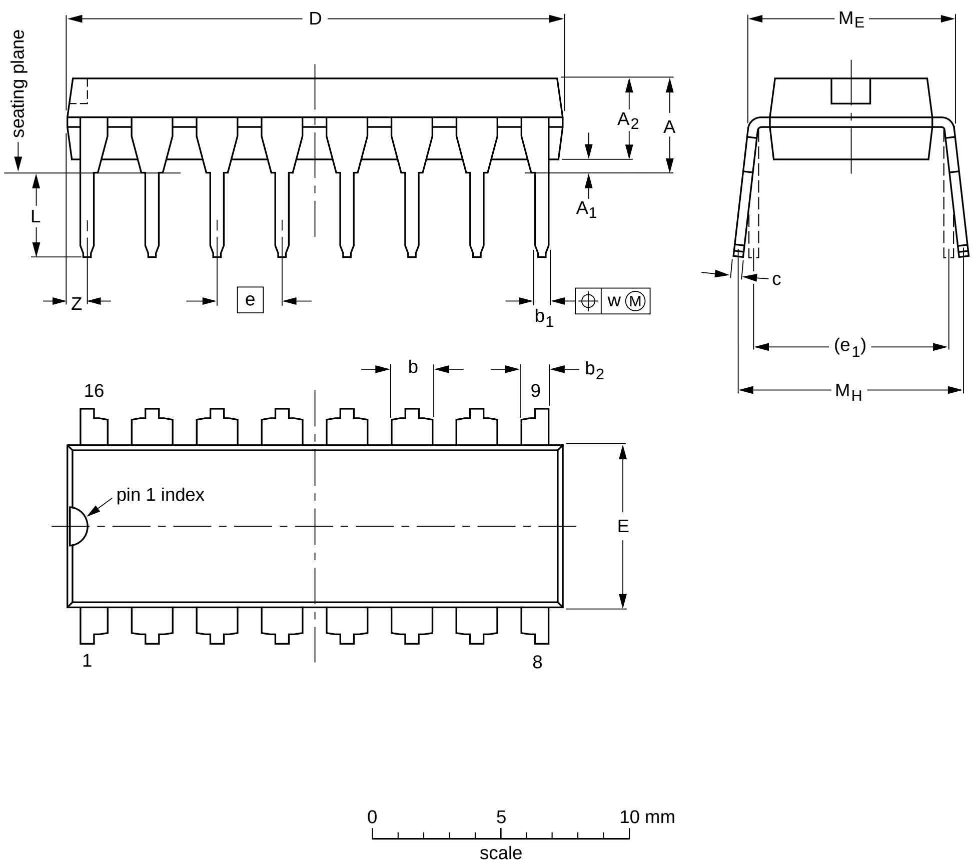
Fig 6. Test circuit for switching times

Table 11. Measurement points and test data

Supply voltage	Input			Load
	V_I	V_M	t_r, t_f	C_L
5 V to 15 V	V_{DD}	$0.5V_I$	≤ 20 ns	50 pF

12. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil) **SOT38-4**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.03

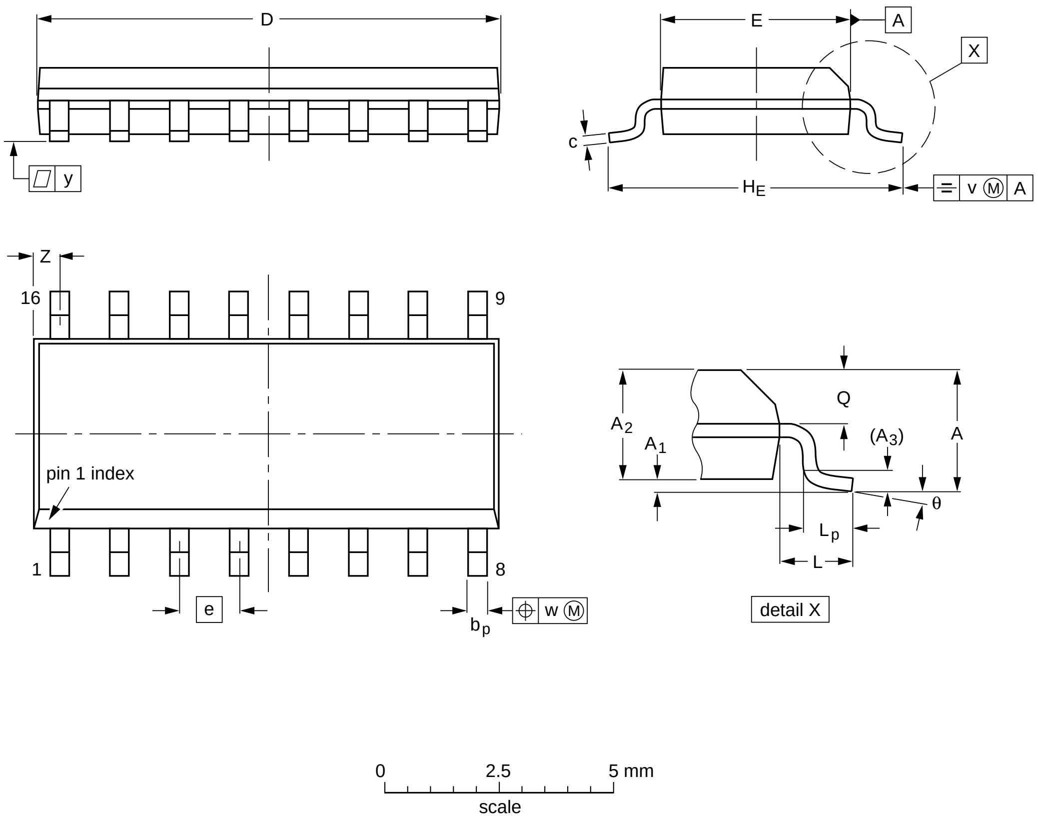
Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT38-4						~~95-01-14~~ 03-02-13

Fig 7. Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 8. Package outline SOT109-1 (SO16)

13. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4557B v.6	20111118	Product data sheet	-	HEF4557B v.5
Modifications:	• Section Applications removed • Table 7: I_{OH} minimum values changed to maximum • Figure 5: "$\overline{A}$/B input" changed to "A/$\overline{B}$ input"			
HEF4557B v.5	20091216	Product data sheet	-	HEF4557B v.4
HEF4557B v.4	20090916	Product data sheet	-	HEF4557B_CNV v.3
HEF4557B_CNV v.3	19950101	Product specification	-	HEF4557B_CNV v.2
HEF4557B_CNV v.2	19950101	Product specification	-	-

14. Legal information

14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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