74LV123

Dual retriggerable monostable multivibrator with reset

Rev. 7 — 12 December 2011 **Product data sheet**

1. General description

The 74LV123 is a low-voltage Si-gate CMOS device and is pin and function compatible with the 74HC123; 74HCT123. It is a dual retriggerable monostable multivibrator which uses three methods to control the output pulse width:

1. The basic pulse time is programmed by the selection of an external resistor (R_{EXT}) and capacitor (C_{EXT}). These are normally connected as shown in Figure 9.
2. Once triggered, the basic output pulse width may be extended by retriggering the gated active LOW-going edge input ($n\overline{A}$) or the active HIGH-going edge input (nB). By repeating this process, the output pulse period (nQ = HIGH, $n\overline{Q}$ = LOW) can be made as long as desired (see Figure 12).
3. Alternatively, an output delay can be terminated at any time by a LOW-going edge on input $n\overline{RD}$, which also inhibits the triggering (see Figure 13).

Schmitt-trigger action in the $n\overline{A}$ and nB inputs makes the circuit highly tolerant of slower input rise and fall times.

2. Features and benefits

- Optimized for low-voltage applications: 1.0 V to 5.5 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical output ground bounce: < 0.8 V at V_{CC} = 3.3 V and T_{amb} = 25 °C
- Typical HIGH-level output voltage (V_{OH}) undershoot: > 2 V at V_{CC} = 3.3 V and T_{amb} = 25 °C
- DC triggered from active HIGH or active LOW inputs
- Retriggerable for very long pulses up to 100 % duty factor
- Direct reset terminates output pulses
- Schmitt-trigger action on all inputs except for the reset input

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LV123N	–40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
74LV123D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74LV123DB	–40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74LV123PW	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74LV123BQ	–40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

4. Functional diagram

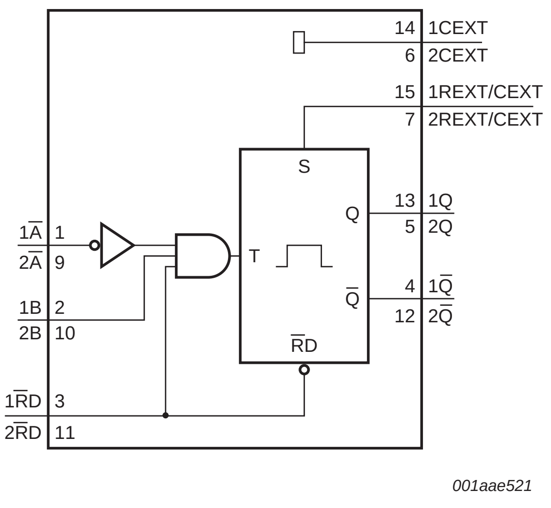


Fig 1. Logic symbol

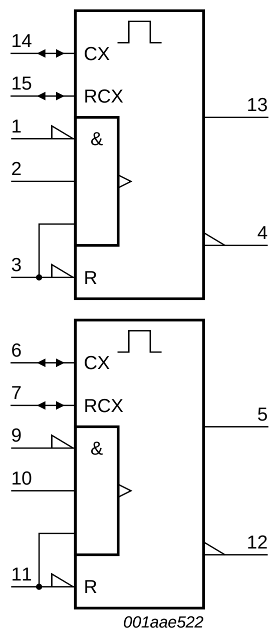


Fig 2. IEC logic symbol

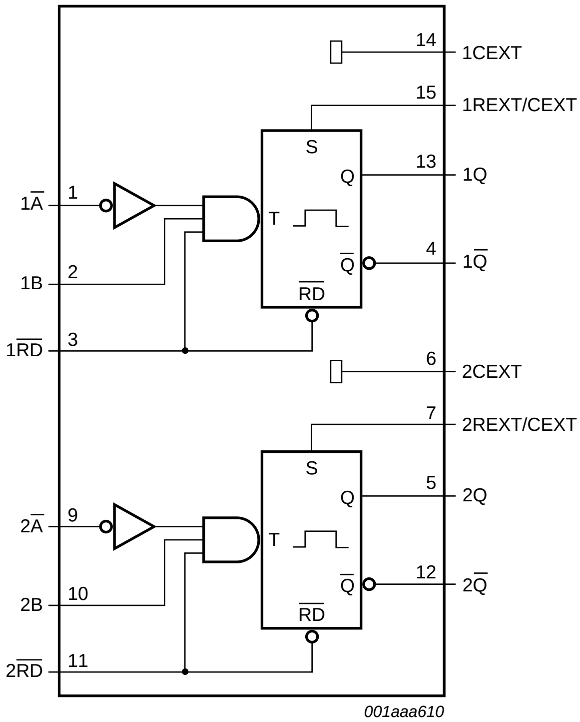


Fig 3. Functional diagram

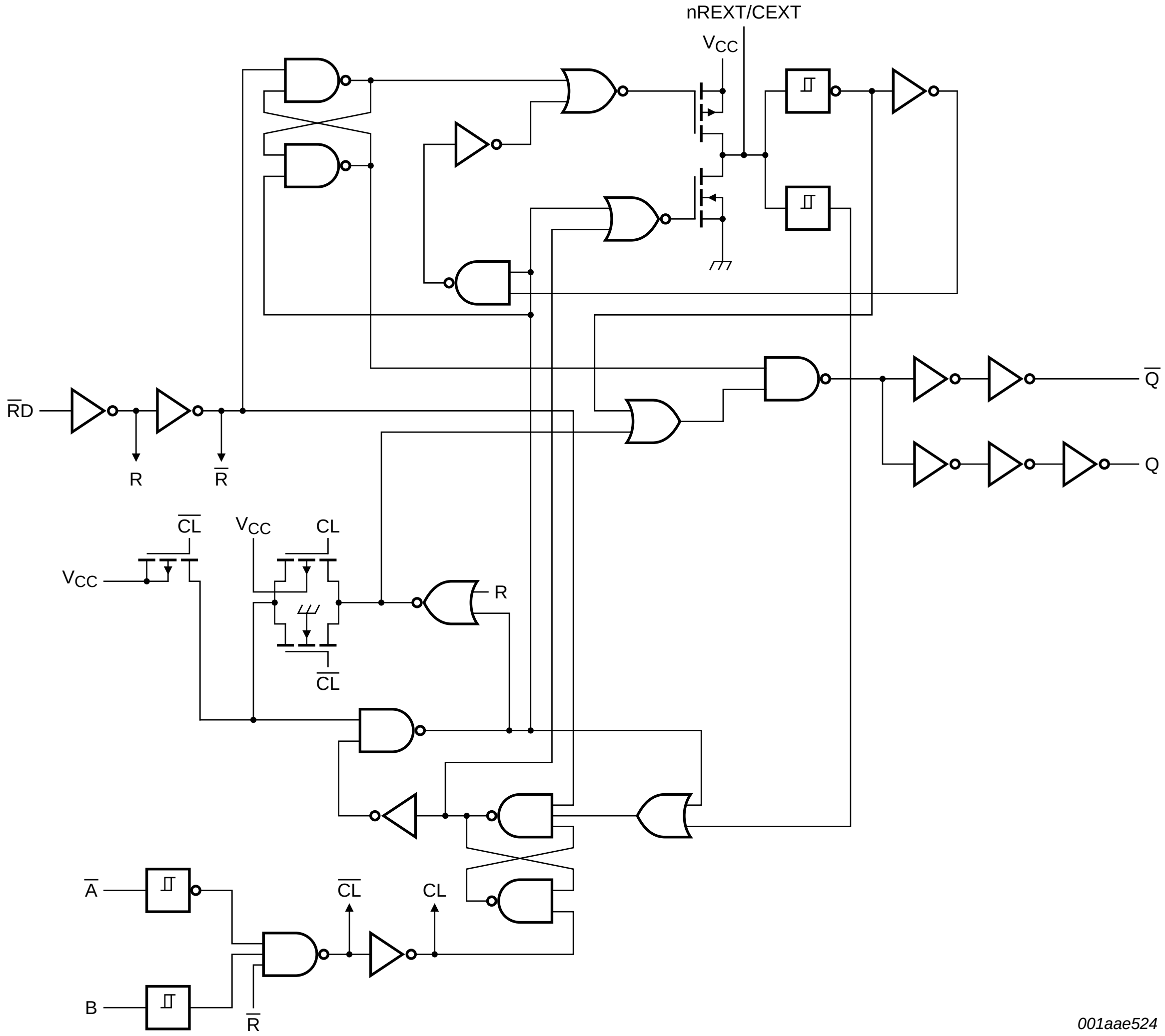


Fig 4. Logic diagram

5. Pinning information

5.1 Pinning

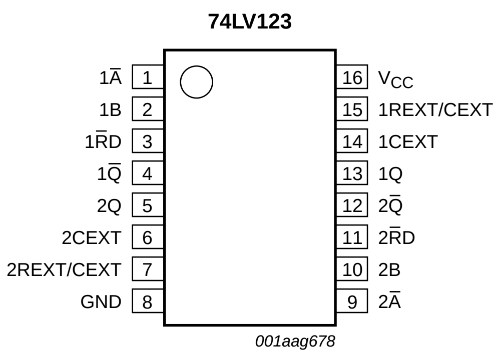
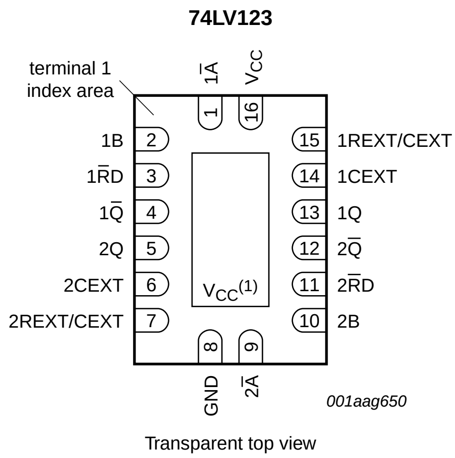


Fig 5. Pin configuration for DIP16, SO16, SSOP16 and TSSOP16



(1) The die substrate is attached to this pad using conductive die attach material. It cannot be used as a supply pin or input.

Fig 6. Pin configuration for DHVQFN16

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$1\overline{A}$	1	negative-edge triggered input 1
1B	2	positive-edge triggered input 1
$1\overline{RD}$	3	direct reset LOW and positive-edge triggered input 1
$1\overline{Q}$	4	active LOW output 1
2Q	5	active HIGH output 2
2CEXT	6	external capacitor connection 2
2REXT/CEXT	7	external resistor and capacitor connection 2
GND	8	ground (0 V)
$2\overline{A}$	9	negative-edge triggered input 2
2B	10	positive-edge triggered input 2
$2\overline{RD}$	11	direct reset LOW and positive-edge triggered input 2
$2\overline{Q}$	12	active LOW output 2
1Q	13	active HIGH output 1
1CEXT	14	external capacitor connection 1
1REXT/CEXT	15	external resistor and capacitor connection 1
V_{CC}	16	supply voltage

6. Functional description

Table 3. Function table[1]

Input			Output	
n$\overline{RD}$	**n$\overline{A}$**	**nB**	**nQ**	**n$\overline{Q}$**
L	X	X	L	H
X	H	X	L[2]	H[2]
X	X	L	L[2]	H[2]
H	L	↑	⊓	⊔
H	↓	H	⊓	⊔
↑	L	H	⊓	⊔

[1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care;
↑ = LOW-to-HIGH transition;
↓ = HIGH-to-LOW transition;
⊓ = one HIGH level output pulse
⊔ = one LOW level output pulse

[2] If the monostable multivibrator was triggered before this condition was established, the pulse will continue as programmed.

7. Limiting values

Table 4. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7	V
I_{IK}	input clamping current	$V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_{OK}	output clamping current	$V_O < –0.5$ V or $V_O > V_{CC} + 0.5$ V	[1]	-	±50	mA
I_O	output current	except for pins nREXT/CEXT; $V_O = –0.5$ V to (V_{CC} + 0.5 V)	[1]	-	±25	mA
I_{CC}	supply current			-	+50	mA
I_{GND}	ground current			-	–50	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +125 °C				
		DIP16 package	[2]	-	750	mW
		SO16 package	[3]	-	500	mW
		SSOP16 package	[4]	-	500	mW
		TSSOP16 package	[4]	-	500	mW
		DHVQFN16 package	[5]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For DIP16 package: P_{tot} derates linearly with 12 mW/K above 70 °C.

[3] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

[4] For SSOP16 and TSSOP16 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

[5] For DHVQFN16 package: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CC}	supply voltage		[1]	1.0	3.3	5.5	V
V_I	input voltage			0	-	V_{CC}	V
V_O	output voltage			0	-	V_{CC}	V
T_{amb}	ambient temperature	in free air		–40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 1.0 V to 2.0 V	[2]	-	-	500	ns/V
		V_{CC} = 2.0 V to 2.7 V		-	-	200	ns/V
		V_{CC} = 2.7 V to 3.6 V		-	-	100	ns/V
		V_{CC} = 3.6 V to 5.5 V		-	-	50	ns/V

[1] The 74LV123 is guaranteed to function down to V_{CC} = 1.0 V (input levels GND or V_{CC}); Section 9 "Static characteristics" are guaranteed from V_{CC} = 1.2 V to V_{CC} = 5.5 V.

[2] Except for Schmitt-trigger inputs $n\overline{A}$ and nB.

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
T_{amb} = –40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V	0.9	-	-	V
		V_{CC} = 2.0 V	1.4	-	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	V
		V_{CC} = 4.5 V to 5.5 V	0.7 × V_{CC}	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V	-	-	0.3	V
		V_{CC} = 2.0 V	-	-	0.6	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	V
		V_{CC} = 4.5 V to 5.5 V	-	-	0.3 × V_{CC}	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = –100 μA; V_{CC} = 1.2 V	-	1.2	-	V
		I_O = –100 μA; V_{CC} = 2.0 V	1.8	2.0	-	V
		I_O = –100 μA; V_{CC} = 2.7 V	2.5	2.7	-	V
		I_O = –100 μA; V_{CC} = 3.0 V	2.8	3.0	-	V
		I_O = –100 μA; V_{CC} = 4.5 V	4.3	4.5	-	V
		I_O = –6 mA; V_{CC} = 3.0 V	2.40	2.82	-	V
		I_O = –12 mA; V_{CC} = 4.5 V	3.60	4.20	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = 100 μA; V_{CC} = 1.2 V	-	0	-	V
		I_O = 100 μA; V_{CC} = 2.0 V	-	0	0.2	V
		I_O = 100 μA; V_{CC} = 2.7 V	-	0	0.2	V
		I_O = 100 μA; V_{CC} = 3.0 V	-	0	0.2	V
		I_O = 100 μA; V_{CC} = 4.5 V	-	0	0.2	V
		I_O = 6 mA; V_{CC} = 3.0 V	-	0.25	0.40	V
		I_O = 12 mA; V_{CC} = 4.5 V	-	0.35	0.55	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 5.5 V	-	-	1.0	μA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	20.0	μA
ΔI_{CC}	additional supply current	V_I = V_{CC} – 0.6 V; V_{CC} = 2.7 V to 3.6 V	-	-	500	μA
C_I	input capacitance		-	3.5	-	pF
T_{amb} = –40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V	0.9	-	-	V
		V_{CC} = 2.0 V	1.4	-	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	V
		V_{CC} = 4.5 V to 5.5 V	0.7 × V_{CC}	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V	-	-	0.3	V
		V_{CC} = 2.0 V	-	-	0.6	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	V
		V_{CC} = 4.5 V to 5.5 V	-	-	0.3 × V_{CC}	V

Table 6. Static characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = -100$ μA; $V_{CC} = 1.2$ V	-	-	-	V
		$I_O = -100$ μA; $V_{CC} = 2.0$ V	1.8	-	-	V
		$I_O = -100$ μA; $V_{CC} = 2.7$ V	2.5	-	-	V
		$I_O = -100$ μA; $V_{CC} = 3.0$ V	2.8	-	-	V
		$I_O = -100$ μA; $V_{CC} = 4.5$ V	4.3	-	-	V
		$I_O = -6$ mA; $V_{CC} = 3.0$ V	2.2	-	-	V
		$I_O = -12$ mA; $V_{CC} = 4.5$ V	3.5	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 100$ μA; $V_{CC} = 1.2$ V	-	-	-	V
		$I_O = 100$ μA; $V_{CC} = 2.0$ V	-	-	0.2	V
		$I_O = 100$ μA; $V_{CC} = 2.7$ V	-	-	0.2	V
		$I_O = 100$ μA; $V_{CC} = 3.0$ V	-	-	0.2	V
		$I_O = 100$ μA; $V_{CC} = 4.5$ V	-	-	0.2	V
		$I_O = 6$ mA; $V_{CC} = 3.0$ V	-	-	0.5	V
		$I_O = 12$ mA; $V_{CC} = 4.5$ V	-	-	0.65	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5$ V	-	-	1.0	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	160	μA
ΔI_{CC}	additional supply current	$V_I = V_{CC} - 0.6$ V; $V_{CC} = 2.7$ V to 3.6 V	-	-	850	μA

[1] All typical values are measured at $T_{amb} = 25$ °C.

10. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V; $t_r = t_f \leq 2.5$ ns; for test circuit see Figure 8.

Symbol	Parameter	Conditions		–40 °C to +85 °C			–40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
Propagation delay; see Figure 7									
t_{pd}	propagation delay	n$\overline{\text{RD}}$, n$\overline{\text{A}}$ and nB to n$\overline{\text{Q}}$	[2]						
		V_{CC} = 1.2 V		-	120	-	-	-	ns
		V_{CC} = 2.0 V		-	40	76	-	92	ns
		V_{CC} = 2.7 V		-	30	56	-	68	ns
		V_{CC} = 3.0 V to 3.6 V		-	25	48	-	57	ns
		V_{CC} = 4.5 V to 5.5 V		-	18	40	-	46	ns
		n$\overline{\text{RD}}$ to nQ (reset)	[2]						
		V_{CC} = 1.2 V		-	100	-	-	-	ns
		V_{CC} = 2.0 V		-	30	57	-	68	ns
		V_{CC} = 2.7 V		-	23	43	-	51	ns
		V_{CC} = 3.0 V to 3.6 V		-	20	38	-	45	ns
		V_{CC} = 4.5 V to 5.5 V		-	14	31	-	36	ns
Inputs n$\overline{\text{A}}$, nB and n$\overline{\text{RD}}$; see Figure 7									
t_W	pulse width	n$\overline{\text{A}}$ = LOW							
		V_{CC} = 2.0 V		30	5	-	40	-	ns
		V_{CC} = 2.7 V		25	3.5	-	30	-	ns
		V_{CC} = 3.0 V to 3.6 V		20	3.0	-	25	-	ns
		V_{CC} = 4.5 V to 5.5 V		15	2.5	-	20	-	ns
		nB = HIGH							
		V_{CC} = 2.0 V		30	13	-	40	-	ns
		V_{CC} = 2.7 V		25	8	-	30	-	ns
		V_{CC} = 3.0 V to 3.6 V		20	7	-	25	-	ns
		V_{CC} = 4.5 V to 5.5 V		15	5	-	20	-	ns
		n$\overline{\text{RD}}$ = LOW; see Figure 13							
		V_{CC} = 2.0 V		35	6	-	45	-	ns
		V_{CC} = 2.7 V		30	5	-	40	-	ns
		V_{CC} = 3.0 V to 3.6 V		25	4	-	30	-	ns
		V_{CC} = 4.5 V to 5.5 V		20	3	-	25	-	ns
t_{rtrig}	retrigger time	nB to n$\overline{\text{A}}$; see Figure 12							
		V_{CC} = 2.0 V		-	70	-	-	-	ns
		V_{CC} = 2.7 V		-	55	-	-	-	ns
		V_{CC} = 3.0 V to 3.6 V		-	45	-	-	-	ns
		V_{CC} = 4.5 V to 5.5 V		-	40	-	-	-	ns

Table 7. Dynamic characteristics *...continued*

GND = 0 V; $t_r = t_f \leq 2.5$ ns; for test circuit see Figure 8.

Symbol	Parameter	Conditions		−40 °C to +85 °C			−40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
Outputs; $n\overline{Q}$ = LOW and nQ = HIGH, see Figure 7									
t_W	pulse width	C_{EXT} = 100 nF; R_{EXT} = 10 kΩ							
		V_{CC} = 2.0 V		-	470	-	-	-	ns
		V_{CC} = 2.7 V		-	460	-	-	-	ns
		V_{CC} = 3.0 V to 3.6 V		-	450	-	-	-	ns
		V_{CC} = 4.5 V to 5.5 V		-	430	-	-	-	ns
		C_{EXT} = 0 pF; R_{EXT} = 5 kΩ							
		V_{CC} = 2.0 V		-	100	-	-	-	ns
		V_{CC} = 2.7 V		-	90	-	-	-	ns
		V_{CC} = 3.0 V to 3.6 V		-	80	-	-	-	ns
		V_{CC} = 4.5 V to 5.5 V		-	70	-	-	-	ns
External components									
R_{EXT}	external resistance	see Figure 11	[3]						
		V_{CC} = 1.2 V		10	-	1000	-	-	kΩ
		V_{CC} = 2.0 V		5	-	1000	-	-	kΩ
		V_{CC} = 2.7 V		3	-	1000	-	-	kΩ
		V_{CC} = 3.0 V to 3.6 V		2	-	1000	-	-	kΩ
		V_{CC} = 4.5 V to 5.5 V		2	-	1000	-	-	kΩ
C_{EXT}	external capacitance	see Figure 11	[3][4]						
		V_{CC} = 1.2 V		-	-	-	-	-	pF
		V_{CC} = 2.0 V		-	-	-	-	-	pF
		V_{CC} = 2.7 V		-	-	-	-	-	pF
		V_{CC} = 3.0 V to 3.6 V		-	-	-	-	-	pF
		V_{CC} = 4.5 V to 5.5 V		-	-	-	-	-	pF
Dynamic power dissipation									
C_{PD}	power dissipation capacitance	V_{CC} = 3.3 V; V_I = GND to V_{CC}	[5]	-	60	-	-	-	pF

[1] All typical values are measured at T_{amb} = 25 °C and nominal supply values (V_{CC} = 3.3 V and 5.0 V).

[2] t_{pd} is the same as t_{PLH} and t_{PHL}; C_{EXT} = 0 pF; R_{EXT} = 5 kΩ.

[3] For other R_{EXT} and C_{EXT} combinations see Figure 11 and Section 12.1.1 “Basic timing”.

[4] C_{EXT} has no limits.

[5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

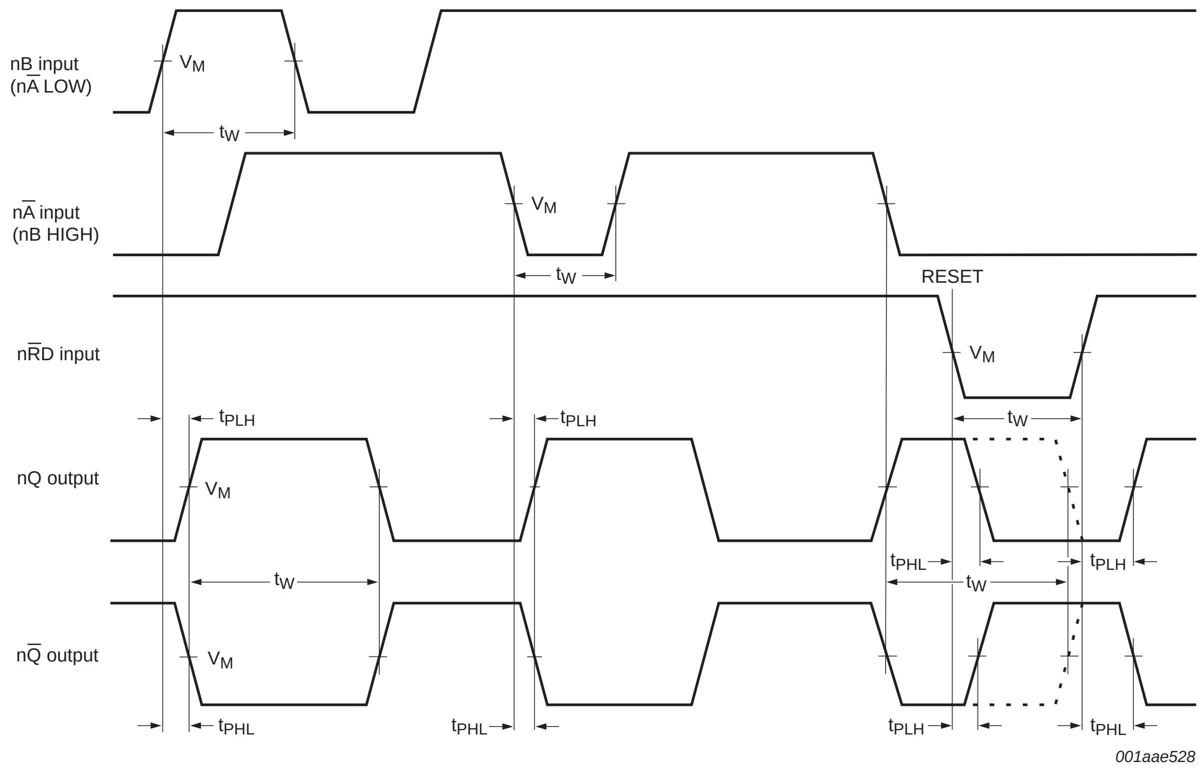
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

11. Waveforms

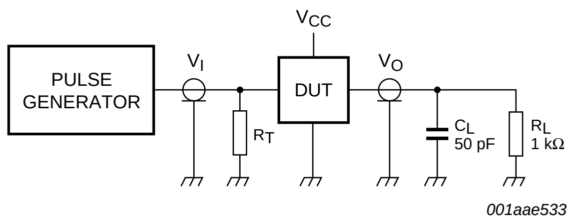


Measurement points are given in Table 8.

Fig 7. Propagation delays from inputs ($n\overline{A}$, nB, $n\overline{RD}$) to outputs (nQ, $n\overline{Q}$)

Table 8. Measurement points

V_{CC}	V_M
≥ 2.7 V	1.5 V
< 2.7 V	0.5 × V_{CC}



Test data is given in Table 9.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to Z_o of the pulse generator.

Fig 8. Load circuitry for switching times

Table 9. Test data

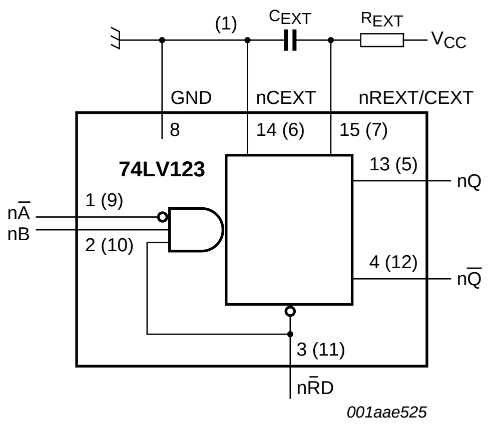
Supply voltage	Input		Load		Test
V_{CC}	V_I	t_r, t_f	C_L	R_L	
< 2.7 V	V_{CC}	≤ 2.5 ns	50 pF	1 kΩ	t_{PHL}, t_{PLH}
2.7 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	1 kΩ	t_{PHL}, t_{PLH}
≥ 4.5 V	V_{CC}	≤ 2.5 ns	50 pF	1 kΩ	t_{PHL}, t_{PLH}

12. Application information

12.1 Timing components

12.1.1 Basic timing

The basic output pulse width is essentially determined by the values of the external timing components R_{EXT} and C_{EXT}.



(1) For minimum noise generation it is recommended to ground pins 6 (2CEXT) and 14 (1CEXT) externally to pin 8 (GND).

Fig 9. Timing components connections

If C_{EXT} > 10 nF, the following formula is valid: $t_W = K \times R_{EXT} \times C_{EXT}$ (typ.) where:

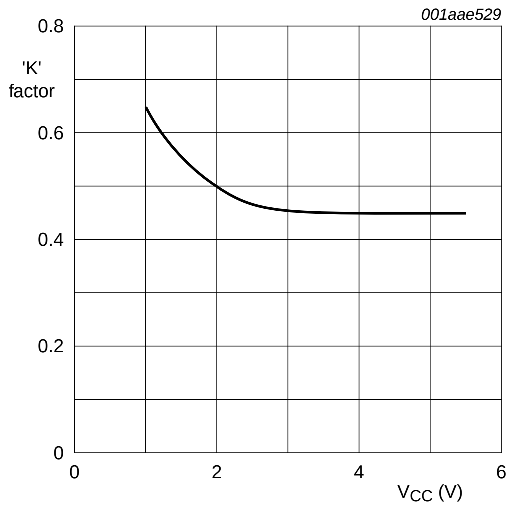
t_W = output pulse width in ns

R_{EXT} = external resistor in kΩ

C_{EXT} = external capacitor in pF

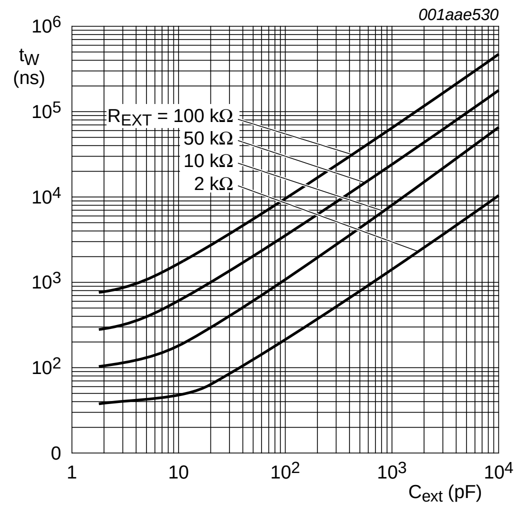
K = constant: this is 0.45 for V_{CC} = 5.0 V and 0.48 for V_{CC} = 2.0 V (see Figure 10)

The inherent test jig and pin capacitance at pin 15 and pin 7 (nREXT/CEXT) is approximately 7 pF.



C_{EXT} = 10 nF; R_{EXT} = 10 kΩ to 100 kΩ

Fig 10. Typical 'K' factor as a function of V_{CC}



V_{CC} = 3.3 V and T_{amb} = 25 °C

Fig 11. Typical output pulse width as a function of the external capacitance values

12.1.2 Retrigger timing

The time to retrigger the monostable multivibrator depends on the values of R_{EXT} and C_{EXT}. The output pulse width will only be extended when the time between the active going edges of the trigger pulses meets the minimum retrigger time. If C_{EXT} > 10 pF, the next formula for the set-up time of a retrigger pulse is valid:

at V_{CC} = 5.0 V: $t_{rtrig} = 30 + 0.19R_{EXT} \times C_{EXT}^{0.9} + 13 \times R_{EXT}^{1.05}$ (typ.)

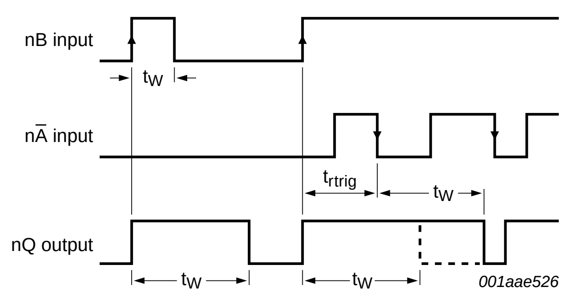
at V_{CC} = 3.0 V: $t_{rtrig} = 41 + 0.15R_{EXT} \times C_{EXT}^{0.9} \times 1 \times R_{EXT}$ (typ.)

where:

t_{rtrig} = retrigger time in ns

C_{EXT} = external capacitor in pF

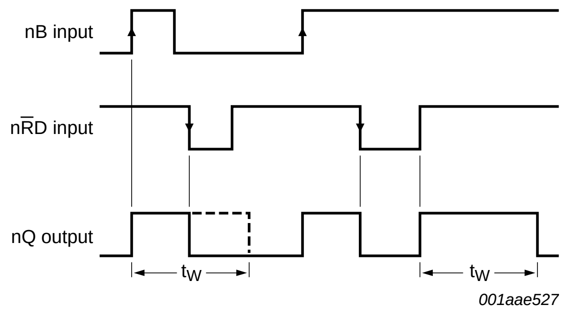
R_{EXT} = external resistor in kΩ



$n\overline{RD}$ = HIGH

Fig 12. Output pulse control using retrigger pulse $n\overline{A}$

12.1.3 Reset timing



n$\overline{A}$ = LOW

Fig 13. Output pulse control using reset input n$\overline{RD}$

12.2 Power considerations

12.2.1 Power-up

When the monostable multivibrator is powered-up, it may produce an output pulse with a pulse width defined by the values of R_{EXT} and C_{EXT}. This output pulse can be eliminated using the RC circuit on pin n$\overline{RD}$ shown in Figure 14.

12.2.2 Power-down

A large capacitor (C_{EXT}) may cause problems when powering-down the monostable due to the energy stored in this capacitor. When a system containing this device is powered-down or a rapid decrease of V_{CC} to zero occurs, the monostable may sustain damage, due to the capacitor discharging through the input protection diodes. To avoid this possibility, connect a damping diode D_{EXT} (preferably a germanium or Schottky type diode) able to withstand large current surges - see Figure 14.

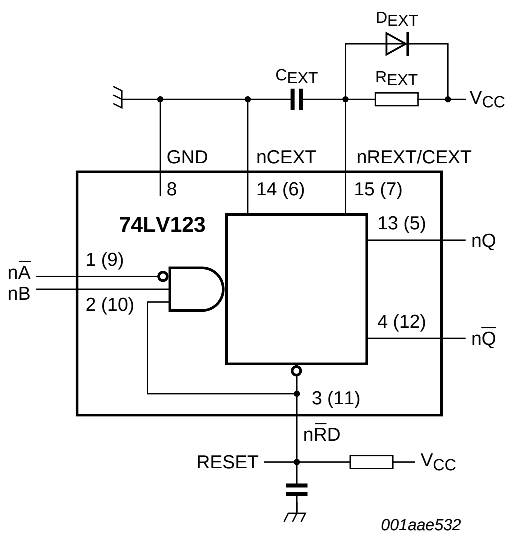
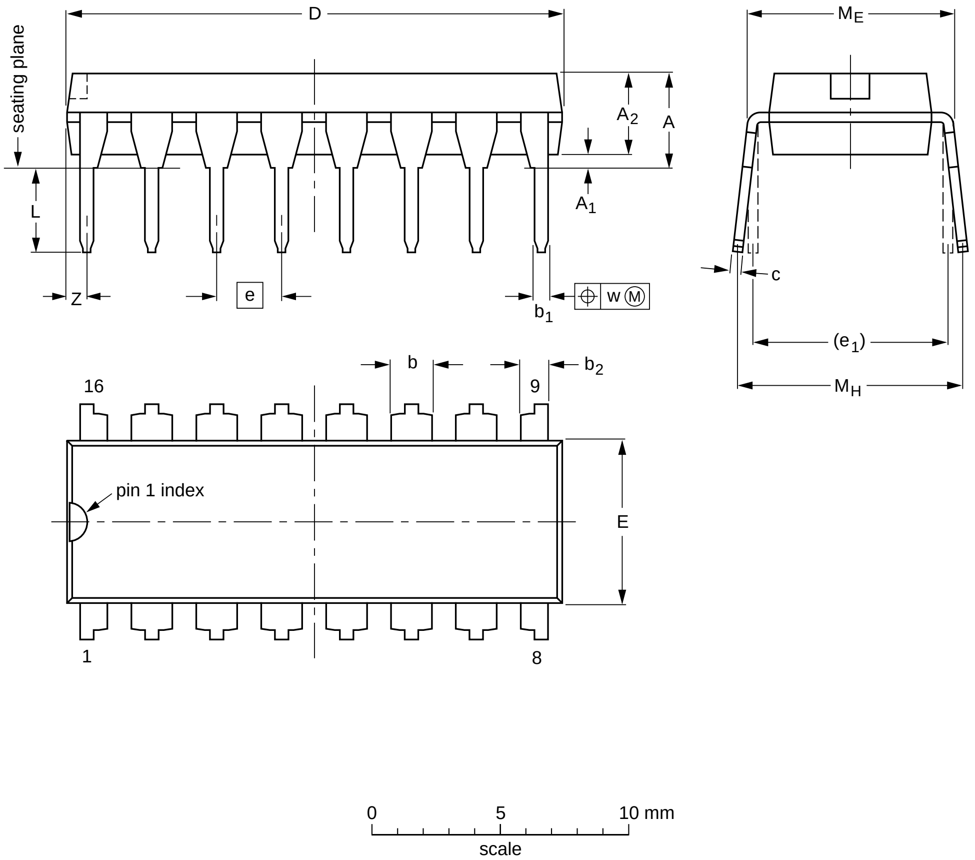


Fig 14. Power-up and power-down circuit

13. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil) **SOT38-4**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.03

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

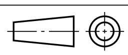
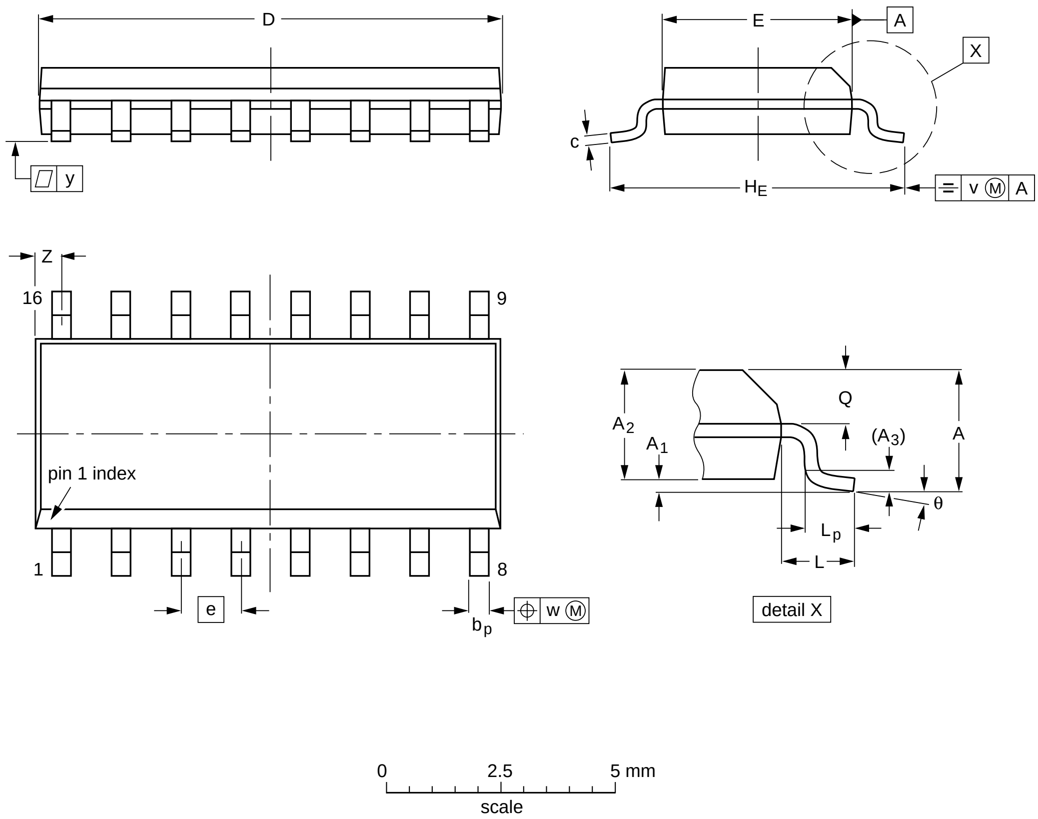
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT38-4						~~95-01-14~~ 03-02-13

Fig 15. Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

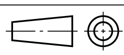
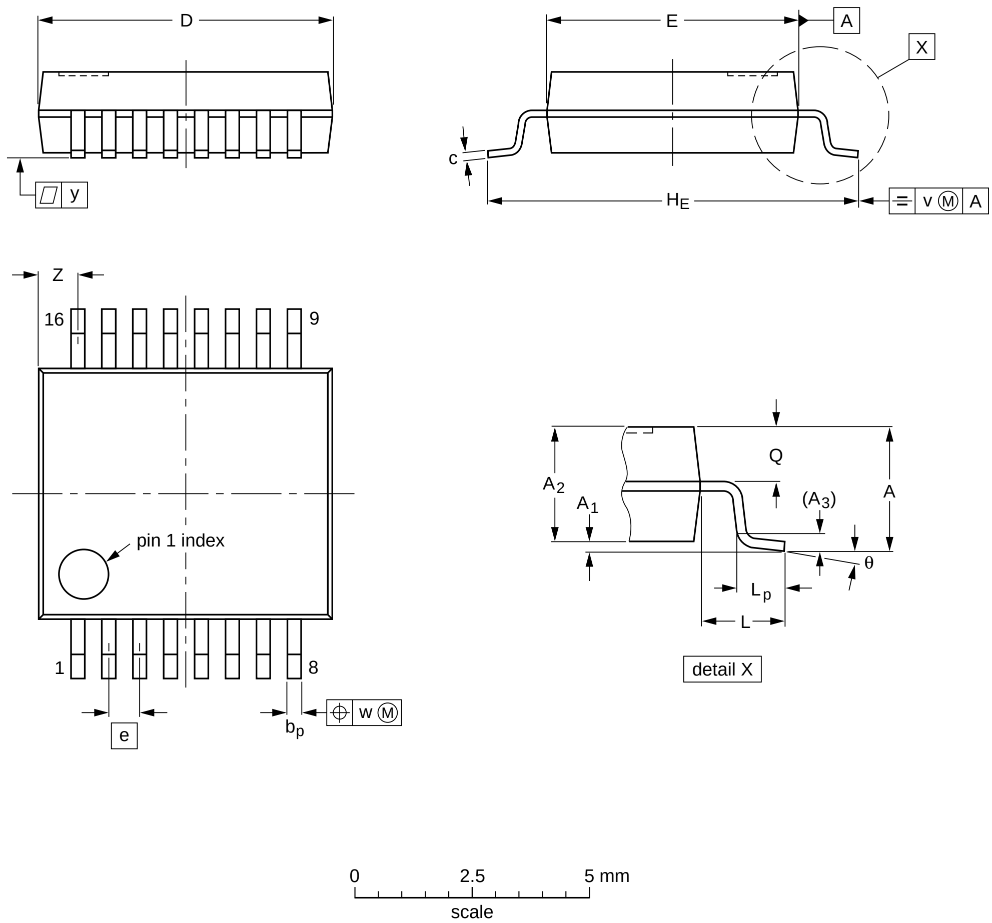
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 16. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8^o 0^o

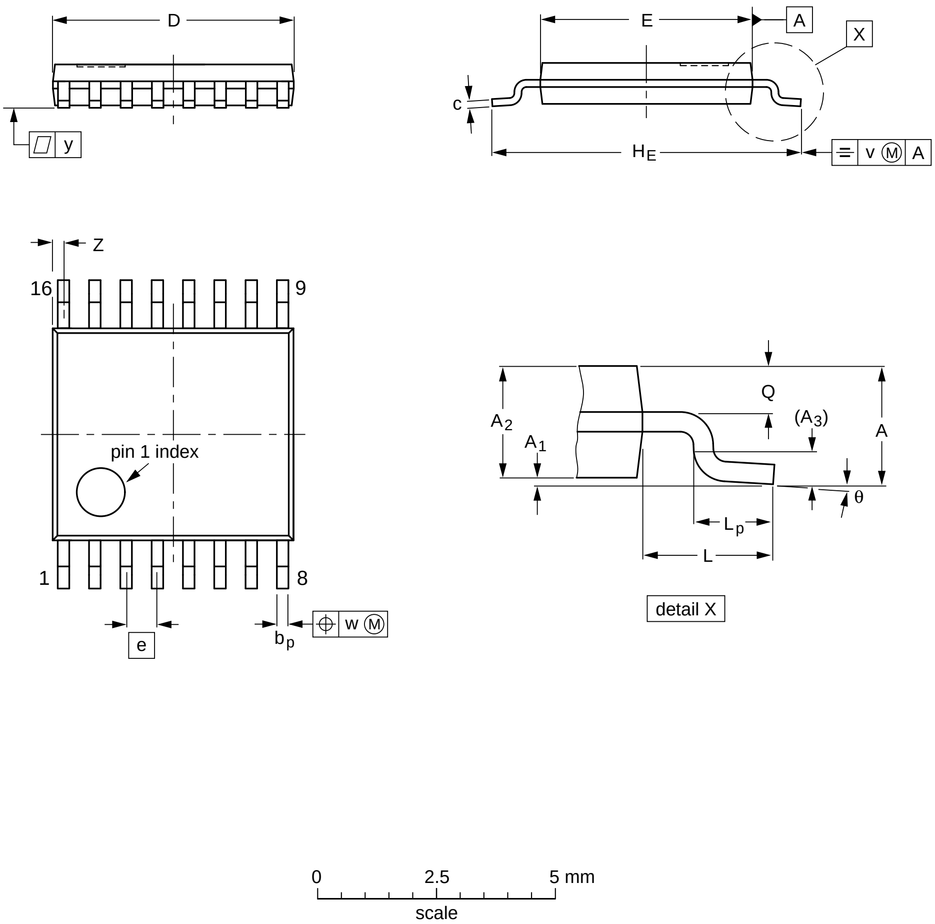
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT338-1		MO-150				~~99-12-27~~ 03-02-19

Fig 17. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^o 0^o

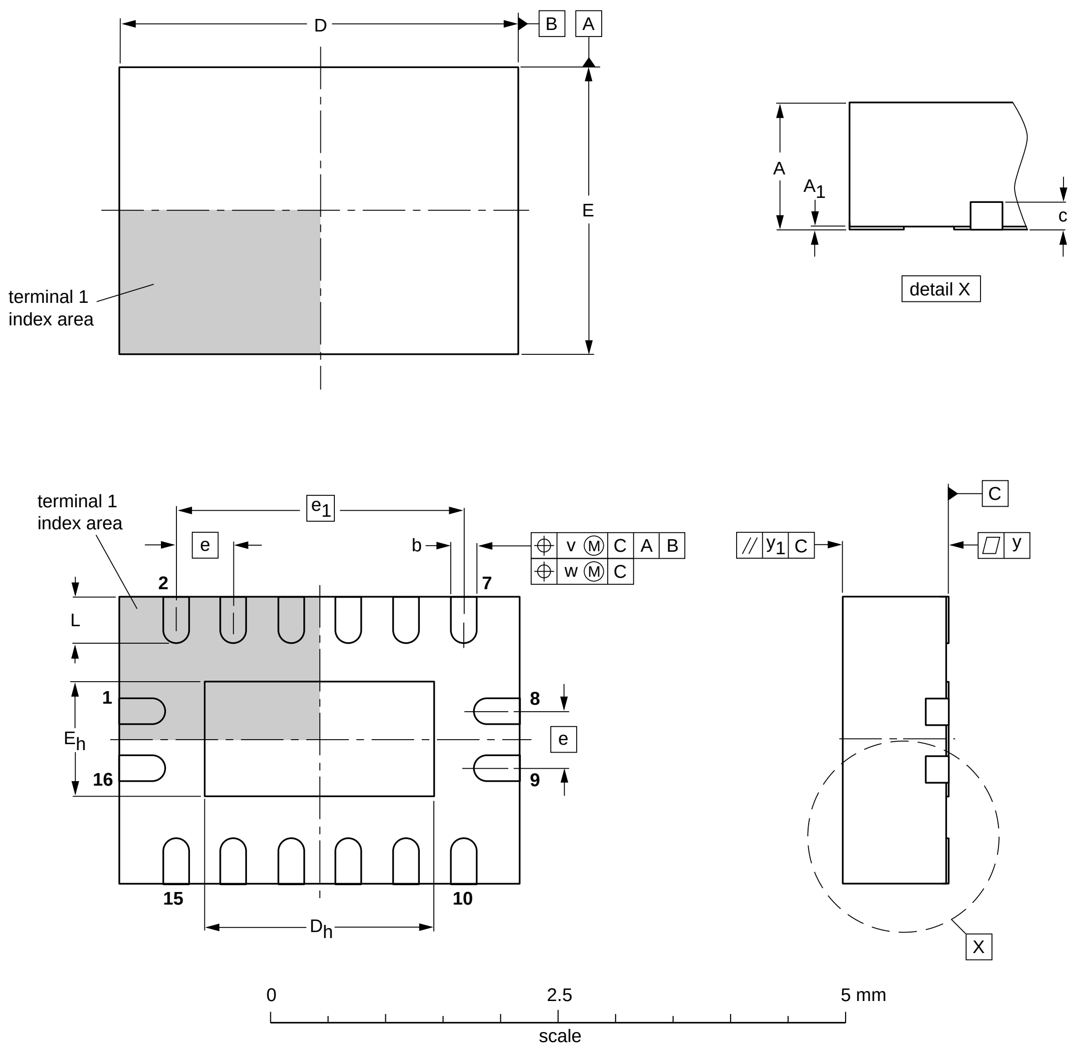
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 18. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm **SOT763-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.6 3.4	2.15 1.85	2.6 2.4	1.15 0.85	0.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT763-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig 19. Package outline SOT736-1 (DHVQFN16)

14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV123 v.7	20111212	Product data sheet	-	74LV123 v.6
Modifications:	• Legal pages updated.			
74LV123 v.6	20110826	Product data sheet	-	74LV123 v.5
74LV123 v.5	20071108	Product data sheet	-	74LV123 v.4
74LV123 v.4	20070919	Product specification	-	74LV123 v.3
74LV123 v.3	20030313	Product specification	-	74LV123 v.2
74LV123 v.2	19980420	Product specification	-	74LV123 v.1
74LV123 v.1	19970204	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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17. Contents

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