

74LVC2GU04

Dual inverter

Rev. 8 — 3 July 2012

Product data sheet

1. General description

The 74LVC2GU04 provides two inverters. Each inverter is a single stage with unbuffered output.

The inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of this device in a mixed 3.3 V and 5 V environment.

2. Features and benefits

- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant input/output for interfacing with 5 V logic
- High noise immunity
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
- ± 24 mA output drive ($V_{CC} = 3.0$ V)
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Input accepts voltages up to 5 V
- Multiple package options
- Specified from -40 °C to $+85$ °C and -40 °C to $+125$ °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC2GU04GW	-40 °C to $+125$ °C	SC-88	plastic surface-mounted package; 6 leads	SOT363
74LVC2GU04GV	-40 °C to $+125$ °C	TSOP6	plastic surface-mounted package (TSOP6); 6 leads	SOT457
74LVC2GU04GM	-40 °C to $+125$ °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body $1 \times 1.45 \times 0.5$ mm	SOT886
74LVC2GU04GF	-40 °C to $+125$ °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body $1 \times 1 \times 0.5$ mm	SOT891
74LVC2GU04GN	-40 °C to $+125$ °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body $0.9 \times 1.0 \times 0.35$ mm	SOT1115
74LVC2GU04GS	-40 °C to $+125$ °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body $1.0 \times 1.0 \times 0.35$ mm	SOT1202



4. Marking

Table 2. Marking codes

Type number	Marking ^[1]
74LVC2GU04GW	YD
74LVC2GU04GV	VU4
74LVC2GU04GM	YD
74LVC2GU04GF	YD
74LVC2GU04GN	YD
74LVC2GU04GS	YD

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

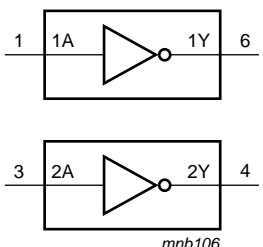


Fig 1. Logic symbol

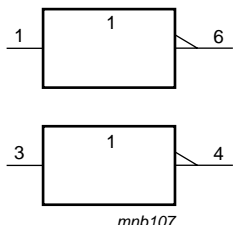


Fig 2. IEC logic symbol

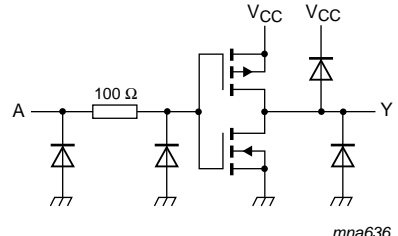


Fig 3. Logic diagram (one gate)

6. Pinning information

6.1 Pinning

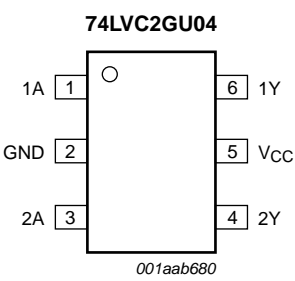


Fig 4. Pin configuration SOT363 and SOT457

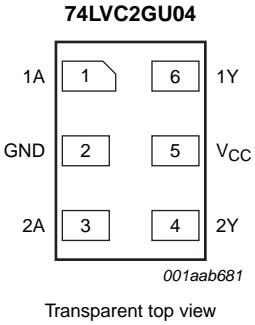


Fig 5. Pin configuration SOT886

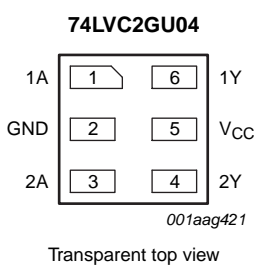


Fig 6. Pin configuration SOT891, SOT1115 and SOT1202

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
1A	1	data input
GND	2	ground (0 V)
2A	3	data input
2Y	4	data output
V _{CC}	5	supply voltage
1Y	6	data output

7. Functional description

Table 4. Function table^[1]

Input	Output
nA	nY
L	H
H	L

[1] H = HIGH voltage level; L = LOW voltage level.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+6.5	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
V _I	input voltage		^[1] -0.5	+6.5	V
I _{OK}	output clamping current	V _O < 0 V	-50	-	mA
V _O	output voltage	Active mode	^{[1][2]} -0.5	V _{CC} + 0.5	V
I _O	output current	V _O = 0 V to V _{CC}	-	±50	mA
I _{CC}	supply current		-	100	mA
I _{GND}	ground current		-100	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C	^[3] -	250	mW

[1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] When V_{CC} = 0 V (Power-down mode), the output voltage can be 5.5 V in normal operation.

[3] For SC-88 and SC-74 packages: above 87.5 °C the value of P_{tot} derates linearly with 4.0 mW/K.
For XSON6 packages: above 118 °C the value of P_{tot} derates linearly with 7.8 mW/K.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.65	-	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage	Active mode	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65 \text{ V to } 2.7 \text{ V}$	-	-	20	ns/V
		$V_{CC} = 2.7 \text{ V to } 5.5 \text{ V}$	-	-	10	ns/V

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{amb} = -40 \text{ °C to } +85 \text{ °C}$ [1]						
V_{IH}	HIGH-level input voltage	$V_{CC} = 1.65 \text{ V to } 5.5 \text{ V}$	$0.75 \times V_{CC}$	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 1.65 \text{ V to } 5.5 \text{ V}$	-	-	$0.25 \times V_{CC}$	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH} \text{ or } V_{IL}$				
		$I_O = -100 \text{ }\mu\text{A}; V_{CC} = 1.65 \text{ V to } 5.5 \text{ V}$	$V_{CC} - 0.1$	-	-	V
		$I_O = -4 \text{ mA}; V_{CC} = 1.65 \text{ V}$	1.2	-	-	V
		$I_O = -8 \text{ mA}; V_{CC} = 2.3 \text{ V}$	1.9	-	-	V
		$I_O = -12 \text{ mA}; V_{CC} = 2.7 \text{ V}$	2.2	-	-	V
		$I_O = -24 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.3	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH} \text{ or } V_{IL}$				
		$I_O = 100 \text{ }\mu\text{A}; V_{CC} = 1.65 \text{ V to } 5.5 \text{ V}$	-	-	0.1	V
		$I_O = 4 \text{ mA}; V_{CC} = 1.65 \text{ V}$	-	-	0.45	V
		$I_O = 8 \text{ mA}; V_{CC} = 2.3 \text{ V}$	-	-	0.3	V
		$I_O = 12 \text{ mA}; V_{CC} = 2.7 \text{ V}$	-	-	0.4	V
		$I_O = 24 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.55	V
		$I_O = 32 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	-	0.55	V
I_I	input leakage current	$V_I = 5.5 \text{ V or GND}; V_{CC} = 0 \text{ V to } 5.5 \text{ V}$	[2] -	± 0.1	± 5	μA
I_{CC}	supply current	$V_I = 5.5 \text{ V or GND}; I_O = 0 \text{ A}; V_{CC} = 1.65 \text{ V to } 5.5 \text{ V}$	-	0.1	10	μA
C_I	input capacitance	$V_{CC} = 3.3 \text{ V}; V_I = \text{GND to } V_{CC}$	-	5	-	pF

Table 7. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = -40 °C to +125 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 1.65 V to 5.5 V	0.8 × V _{CC}	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.65 V to 5.5 V	-	-	0.2 × V _{CC}	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = -100 μA; V _{CC} = 1.65 V to 5.5 V	V _{CC} - 0.1	-	-	V
		I _O = -4 mA; V _{CC} = 1.65 V	0.95	-	-	V
		I _O = -8 mA; V _{CC} = 2.3 V	1.7	-	-	V
		I _O = -12 mA; V _{CC} = 2.7 V	1.9	-	-	V
		I _O = -24 mA; V _{CC} = 3.0 V	2.0	-	-	V
		I _O = -32 mA; V _{CC} = 4.5 V	3.4	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 100 μA; V _{CC} = 1.65 V to 5.5 V	-	-	0.1	V
		I _O = 4 mA; V _{CC} = 1.65 V	-	-	0.7	V
		I _O = 8 mA; V _{CC} = 2.3 V	-	-	0.45	V
		I _O = 12 mA; V _{CC} = 2.7 V	-	-	0.6	V
		I _O = 24 mA; V _{CC} = 3.0 V	-	-	0.8	V
		I _O = 32 mA; V _{CC} = 4.5 V	-	-	0.8	V
I _I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	-	±20	μA
I _{CC}	supply current	V _I = 5.5 V or GND; I _O = 0 A; V _{CC} = 1.65 V to 5.5 V	-	-	40	μA

[1] All typical values are measured at T_{amb} = 25 °C.

[2] These typical values are measured at V_{CC} = 3.3 V.

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 8](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t _{pd}	propagation delay	nA to nY; see Figure 7 ^[2]						
		V _{CC} = 1.65 V to 1.95 V	0.5	2.3	5.0	0.5	6.3	ns
		V _{CC} = 2.3 V to 2.7 V	0.3	1.8	4.0	0.3	5.0	ns
		V _{CC} = 2.7 V	0.3	2.6	4.5	0.3	5.6	ns
		V _{CC} = 3.0 V to 3.6 V	0.3	2.3	3.7	0.3	4.5	ns
		V _{CC} = 4.5 V to 5.5 V	0.3	1.7	3.0	0.3	3.8	ns
C _{PD}	power dissipation capacitance	V _I = GND to V _{CC} ; V _{CC} = 3.3 V ^[3]	-	7.8	-			pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.8 V, 2.5 V, 2.7 V, 3.3 V and 5.0 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

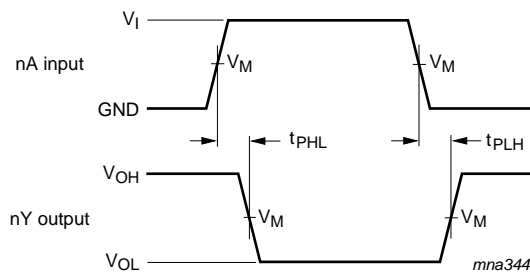
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

∑(C_L × V_{CC}² × f_o) = sum of outputs.

12. Waveforms



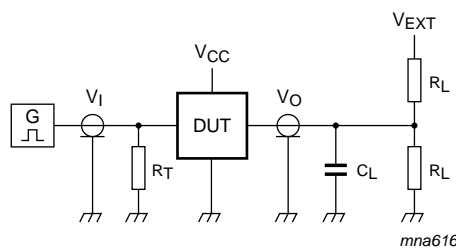
Measurement points are given in [Table 9](#).

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig 7. The input (nA) to output (nY) propagation delay times

Table 9. Measurement points

Supply voltage	Input	Output
V_{CC}	V_M	V_M
1.65 V to 1.95 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.3 V to 2.7 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	1.5 V	1.5 V
4.5 V to 5.5 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$



Test data is given in [Table 10](#).

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

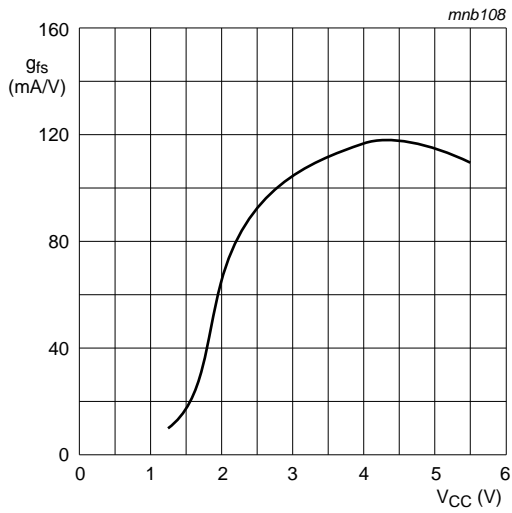
R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig 8. Test circuit for measuring switching times

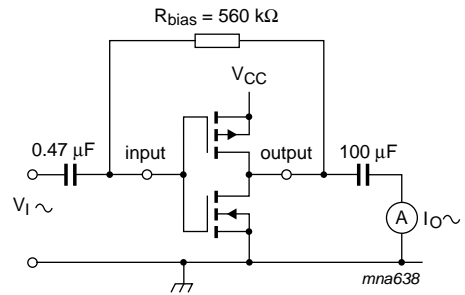
Table 10. Test data

Supply voltage	Input		Load		V_{EXT}
V_{CC}	V_I	$t_r = t_f$	C_L	R_L	t_{PLH}, t_{PHL}
1.65 V to 1.95 V	V_{CC}	≤ 2.0 ns	30 pF	1 k Ω	open
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open
4.5 V to 5.5 V	V_{CC}	≤ 2.5 ns	50 pF	500 Ω	open



T_{amb} = 25 °C.

Fig 9. Typical forward transconductance as a function of supply voltage



$$g_{fs} = \frac{\Delta I_O}{\Delta V_I}$$

f_i = 1 kHz.

V_O is constant.

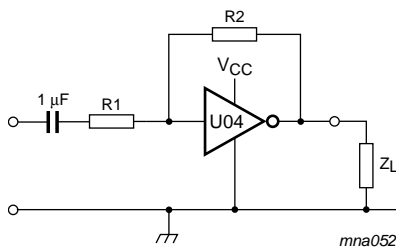
Fig 10. Test set-up for measuring forward transconductance

13. Application information

Some applications are:

- Linear amplifier (see [Figure 11](#))
- In crystal oscillator design (see [Figure 12](#))

Remark: All values given are typical unless otherwise specified.



$$V_{o(p-p)} = V_{CC} - 1.5 \text{ V centered at } 0.5V_{CC}.$$

$$A_u = - \frac{G_{OL}}{1 + \frac{R1}{R2}(1 + G_{OL})}$$

G_{OL} = open loop gain.

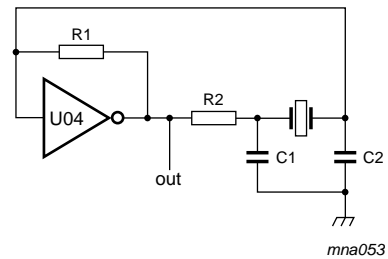
A_u = voltage amplification.

$R1 \geq 3 \text{ k}\Omega$, $R2 \leq 1 \text{ M}\Omega$.

$Z_L > 10 \text{ k}\Omega$; $A_{OL} = 20$ (typical).

Typical unity gain bandwidth product is 5 MHz.

Fig 11. Linear amplifier configuration



$C1 = 47 \text{ pF}$ (typical).

$C2 = 22 \text{ pF}$ (typical).

$R1 = 1 \text{ M}\Omega$ to $10 \text{ M}\Omega$ (typical).

$R2$ optimum value depends on the frequency and required stability against changes in V_{CC} or average minimum I_{CC} (I_{CC} is typically 2 mA at $V_{CC} = 3.3 \text{ V}$ and $f = 10 \text{ MHz}$).

Fig 12. Crystal oscillator configuration

14. Package outline

Plastic surface-mounted package; 6 leads

SOT363

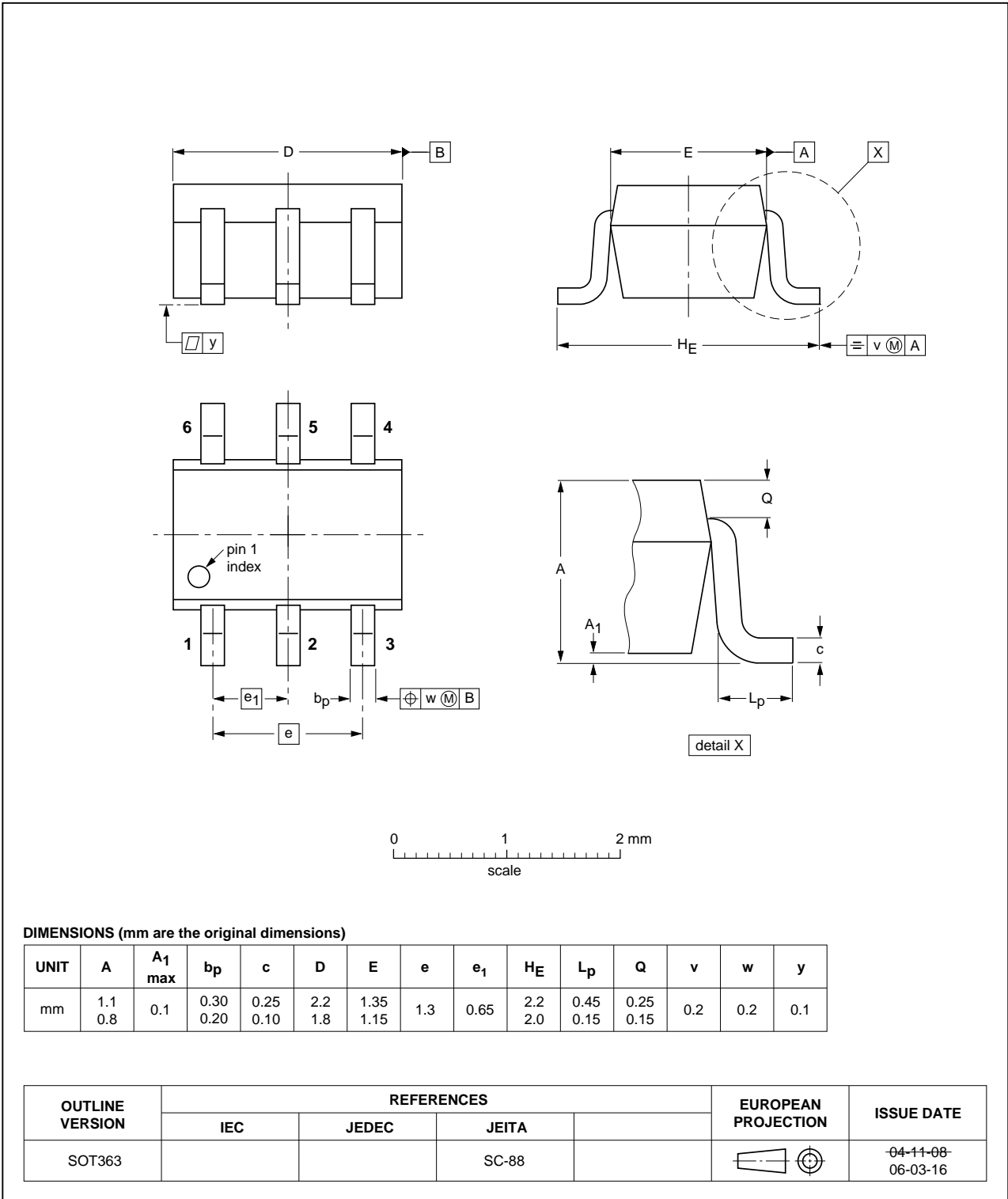


Fig 13. Package outline SOT363 (SC-88)

Plastic surface-mounted package (TSOP6); 6 leads

SOT457

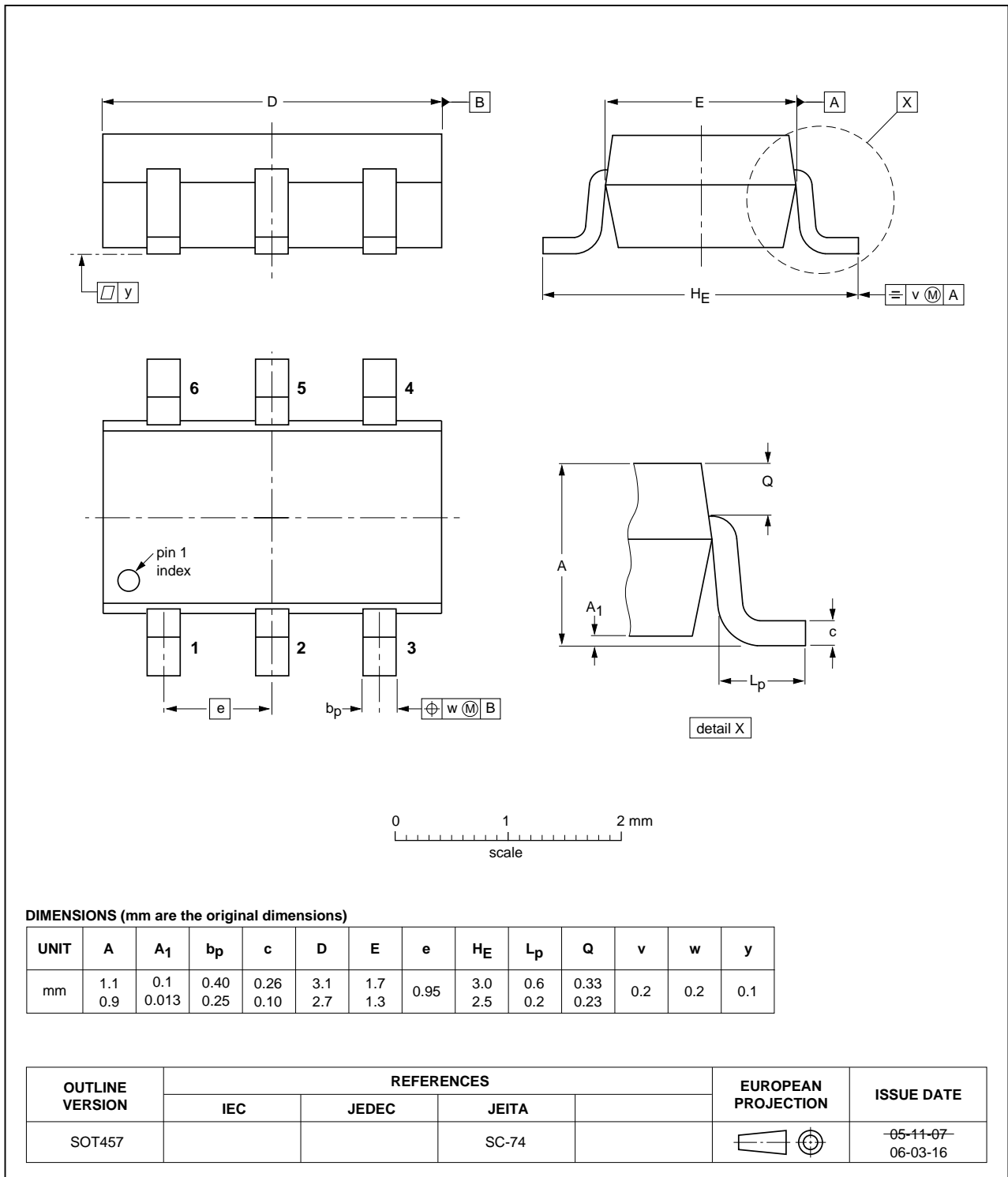


Fig 14. Package outline SOT457 (TSOP6)

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm

SOT886



Fig 15. Package outline SOT886 (XSON6)

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1 x 0.5 mm

SOT891

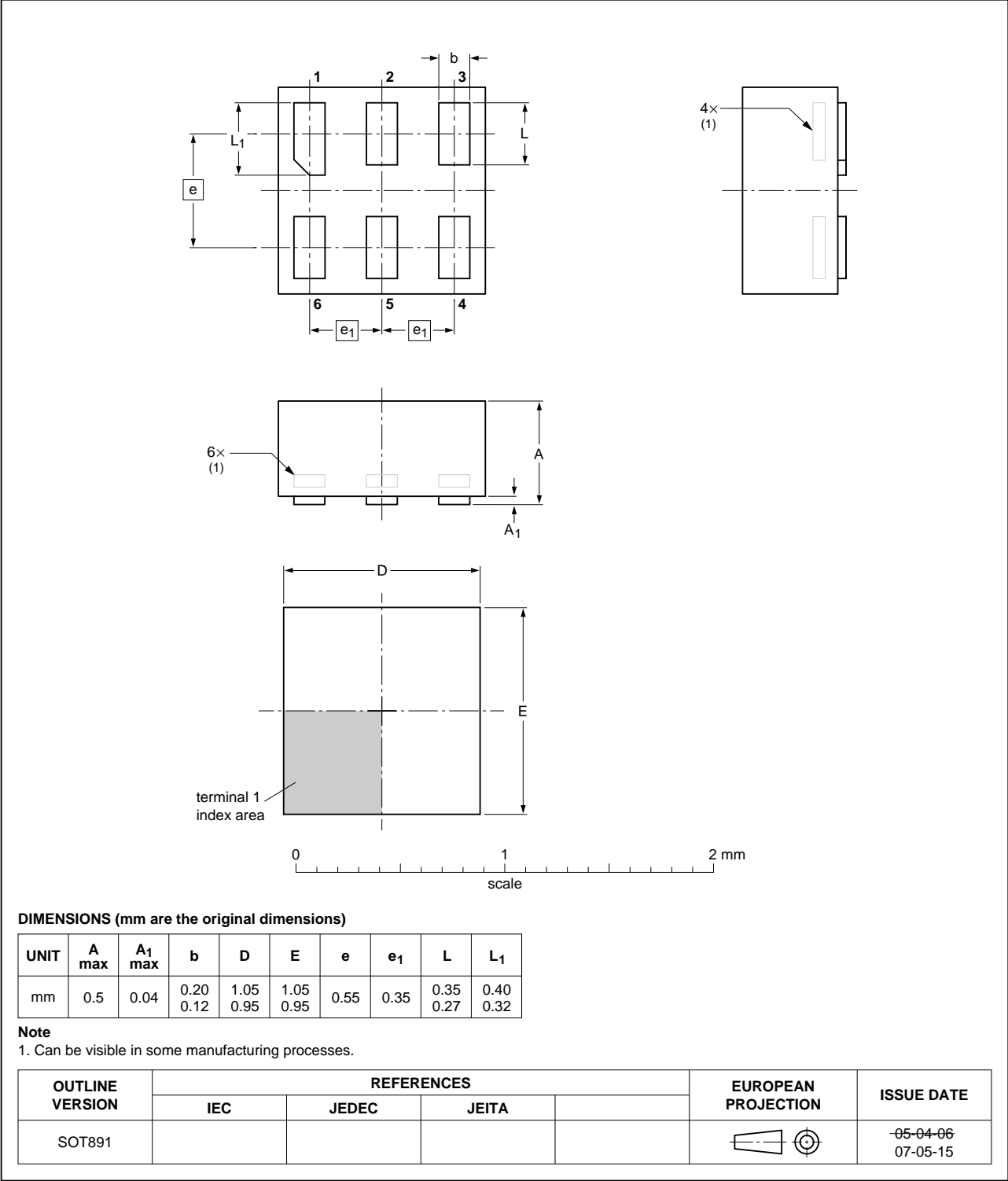


Fig 16. Package outline SOT891 (XSON6)

**XSON6: extremely thin small outline package; no leads;
6 terminals; body 0.9 x 1.0 x 0.35 mm**

SOT1115



Fig 17. Package outline SOT1115 (XSON6)

XSON6: extremely thin small outline package; no leads;
6 terminals; body 1.0 x 1.0 x 0.35 mm

SOT1202



Fig 18. Package outline SOT1202 (XSON6)

15. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

16. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC2GU04 v.8	20120703	Product data sheet	-	74LVC2GU04 v.7
Modifications:	<ul style="list-style-type: none"> Package outline drawing of SOT886 (Figure 15) modified. 			
74LVC2GU04 v.7	20111128	Product data sheet	-	74LVC2GU04 v.6
Modifications:	<ul style="list-style-type: none"> Legal pages updated. 			
74LVC2GU04 v.6	20101027	Product data sheet	-	74LVC2GU04 v.5
74LVC2GU04 v.5	20091027	Product data sheet	-	74LVC2GU04 v.4
74LVC2GU04 v.4	20070521	Product data sheet	-	74LVC2GU04 v.3
74LVC2GU04 v.3	20040921	Product specification	-	74LVC2GU04 v.2
74LVC2GU04 v.2	20040524	Product specification	-	74LVC2GU04 v.1
74LVC2GU04 v.1	20030829	Product specification	-	-

17. Legal information

17.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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19. Contents

1	General description	1
2	Features and benefits	1
3	Ordering information	1
4	Marking	2
5	Functional diagram	2
6	Pinning information	2
6.1	Pinning	2
6.2	Pin description	3
7	Functional description	3
8	Limiting values	3
9	Recommended operating conditions	4
10	Static characteristics	4
11	Dynamic characteristics	6
12	Waveforms	6
13	Application information	9
14	Package outline	10
15	Abbreviations	16
16	Revision history	16
17	Legal information	17
17.1	Data sheet status	17
17.2	Definitions	17
17.3	Disclaimers	17
17.4	Trademarks	18
18	Contact information	18
19	Contents	19

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Date of release: 3 July 2012

Document identifier: 74LVC2GU04