74HC564

Octal D-type flip-flop; positive-edge trigger; 3-state; inverting

Rev. 03 — 11 November 2004 Product data sheet

1. General description

The 74HC564 is a high-speed Si-gate CMOS device and is pin compatible with low-power Schottky TTL (LSTTL). The 74HC564 is specified in compliance with JEDEC standard no. 7A.

The 74HC564 is a octal D-type flip-flop featuring separate D-type inputs for each flip-flop and inverting 3-state outputs for bus oriented applications. A clock (CP) and an output enable ($\overline{OE}$) input are common to all flip-flops.

The 8 flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition. When $\overline{OE}$ is LOW, the contents of the 8 flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high-impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

The 74HC564 is functionally identical to the 74HC574 but has inverting outputs. The 74HC564 is functionally identical to the 74HC534, but has a different pinning.

2. Features

- 3-state inverting outputs for bus oriented applications
- 8-bit positive-edge triggered register
- Common 3-state output enable input
- Independent register and 3-state buffer operation
- Low-power dissipation
- Complies with JEDEC standard no. 7A
- ESD protection:
  - HBM EIA/JESD22-A114-B exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V.
- Multiple package options
- Specified from –40 °C to +80 °C and from –40 °C to +125 °C.

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3. Quick reference data

Table 1: Quick reference data

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{PHL}, t_{PLH}	propagation delay CP to $\overline{Q}$n	C_L = 15 pF; V_{CC} = 5 V		-	15	-	ns
f_{max}	maximum clock frequency	C_L = 15 pF; V_{CC} = 5 V		-	127	-	MHz
C_I	input capacitance			-	3.5	-	pF
C_{PD}	power dissipation capacitance per flip-flop	V_I = GND to V_{CC}	[1]	-	27	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

4. Ordering information

Table 2: Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC564N	–40 °C to +125 °C	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
74HC564D	–40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

5. Functional diagram

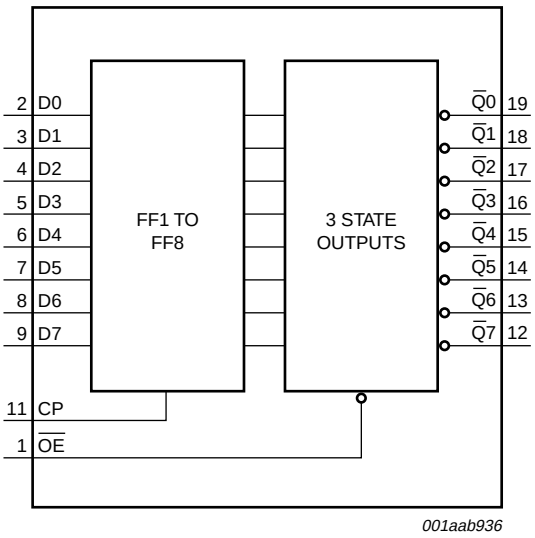


Fig 1. Functional diagram

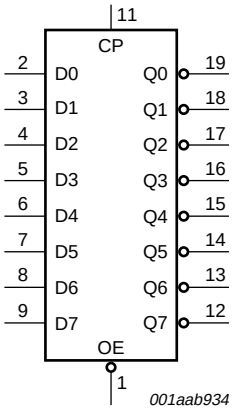


Fig 2. Logic symbol

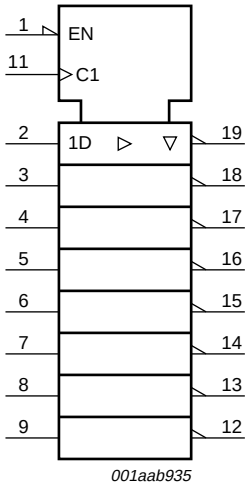


Fig 3. IEC logic symbol

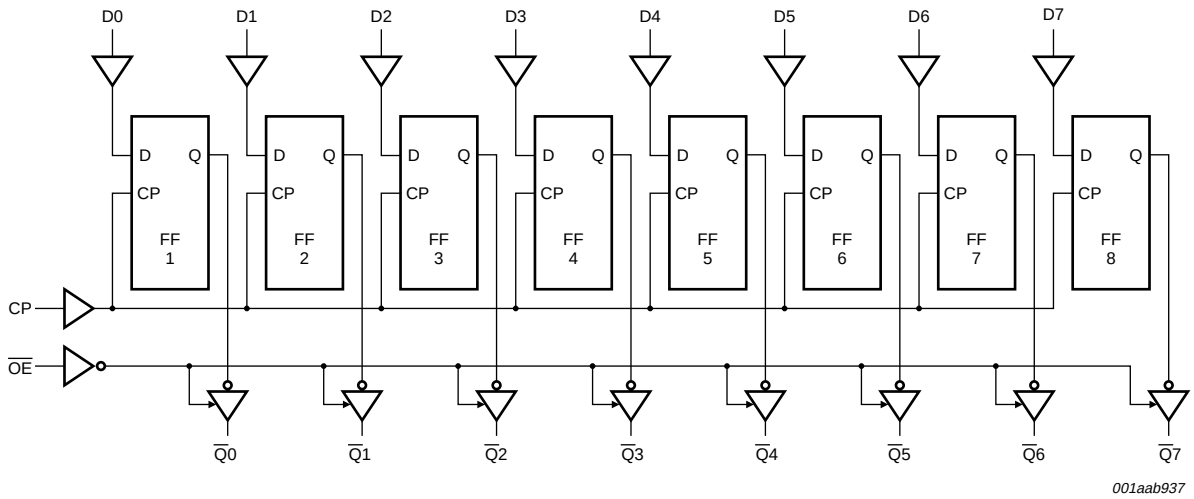


Fig 4. Logic diagram

6. Pinning information

6.1 Pinning

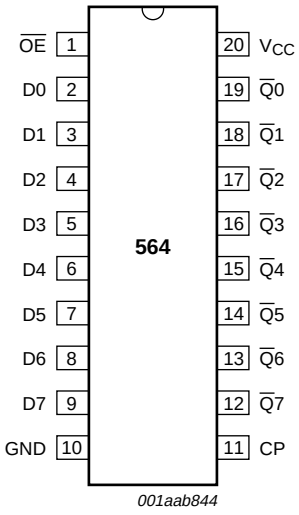


Fig 5. Pin configuration

6.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
$\overline{OE}$	1	3-state output enable input (active LOW)
D0	2	data input 0
D1	3	data input 1
D2	4	data input 2
D3	5	data input 3
D4	6	data input 4
D5	7	data input 5
D6	8	data input 6
D7	9	data input 7
GND	10	ground (0 V)
CP	11	clock input (LOW-to-HIGH, edge-triggered)
$\overline{Q}7$	12	3-state flip-flop output 7
$\overline{Q}6$	13	3-state flip-flop output 6
$\overline{Q}5$	14	3-state flip-flop output 5
$\overline{Q}4$	15	3-state flip-flop output 4
$\overline{Q}3$	16	3-state flip-flop output 3
$\overline{Q}2$	17	3-state flip-flop output 2
$\overline{Q}1$	18	3-state flip-flop output 1
$\overline{Q}0$	19	3-state flip-flop output 0
V_{CC}	20	positive supply voltage

7. Functional description

7.1 Function table

Table 4: Function table [1]

Operating mode	Input			Internal flip-flop	Output
	$\overline{OE}$	CP	Dn		$\overline{Qn}$
Load and read register	L	↑	l	L	H
			h	H	L
Load register and disable output	H	↑	l	L	Z
			h	H	Z

[1] H = HIGH voltage level;
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition;
L = LOW voltage level;
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition;
Z = high-impedance OFF-state;
↑ = LOW-to-HIGH clock transition.

8. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7	V
I_{IK}	input diode current	$V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V		-	±20	mA
I_{OK}	output diode current	$V_O < –0.5$ V or $V_O > V_{CC} + 0.5$ V		-	±20	mA
I_O	output source or sink current	$V_O = –0.5$ V to $V_{CC} + 0.5$ V		-	±35	mA
I_{CC}, I_{GND}	V_{CC} or GND current			-	±70	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	power dissipation					
	DIP20 package		[1]	-	750	mW
	SO20 package		[2]	-	500	mW

[1] Above 70 °C: P_{tot} derates linearly with 12 mW/K.

[2] Above 70 °C: P_{tot} derates linearly with 8 mW/K.

9. Recommended operating conditions

Table 6: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
t_r, t_f	input rise and fall times	$V_{CC} = 2.0$ V	-	-	1000	ns
		$V_{CC} = 4.5$ V	-	6.0	500	ns
		$V_{CC} = 6.0$ V	-	-	400	ns
T_{amb}	ambient temperature		–40	-	+125	°C

10. Static characteristics

Table 7: Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = –20 µA; V_{CC} = 2.0 V	1.9	2.0	-	V
		I_O = –20 µA; V_{CC} = 4.5 V	4.4	4.5	-	V
		I_O = –20 µA; V_{CC} = 6.0 V	5.9	6.0	-	V
		I_O = –6.0 mA; V_{CC} = 4.5 V	3.98	4.32	-	V
		I_O = –7.8 mA; V_{CC} = 6.0 V	5.48	5.81	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 20 µA; V_{CC} = 2.0 V	-	0	0.1	V
		I_O = 20 µA; V_{CC} = 4.5 V	-	0	0.1	V
		I_O = 20 µA; V_{CC} = 6.0 V	-	0	0.1	V
		I_O = 6.0 mA; V_{CC} = 4.5 V	-	0.15	0.26	V
		I_O = 7.8 mA; V_{CC} = 6.0 V	-	0.16	0.26	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 6.0 V	-	-	±0.1	µA
I_{OZ}	3-state OFF-state current	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 6.0 V; $V_O = V_{CC}$ or GND	-	-	±0.5	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	8.0	µA
C_I	input capacitance		-	3.5	-	pF
T_{amb} = –40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = –20 µA; V_{CC} = 2.0 V	1.9	-	-	V
		I_O = –20 µA; V_{CC} = 4.5 V	4.4	-	-	V
		I_O = –20 µA; V_{CC} = 6.0 V	5.9	-	-	V
		I_O = –6.0 mA; V_{CC} = 4.5 V	3.84	-	-	V
		I_O = –7.8 mA; V_{CC} = 6.0 V	5.34	-	-	V

Table 7: Static characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 20 µA; V_{CC} = 2.0 V	-	-	0.1	V
		I_O = 20 µA; V_{CC} = 4.5 V	-	-	0.1	V
		I_O = 20 µA; V_{CC} = 6.0 V	-	-	0.1	V
		I_O = 6.0 mA; V_{CC} = 4.5 V	-	-	0.33	V
		I_O = 7.8 mA; V_{CC} = 6.0 V	-	-	0.33	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 6.0 V	-	-	±1.0	µA
I_{OZ}	3-state OFF-state current	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 6.0 V; $V_O = V_{CC}$ or GND	-	-	±5.0	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	80	µA
T_{amb} = −40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}		-		
		I_O = −20 µA; V_{CC} = 2.0 V	1.9	-	-	V
		I_O = −20 µA; V_{CC} = 4.5 V	4.4	-	-	V
		I_O = −20 µA; V_{CC} = 6.0 V	5.9	-	-	V
		I_O = −6.0 mA; V_{CC} = 4.5 V	3.7	-	-	V
		I_O = −7.8 mA; V_{CC} = 6.0 V	5.2	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}		-		
		I_O = 20 µA; V_{CC} = 2.0 V	-	-	0.1	V
		I_O = 20 µA; V_{CC} = 4.5 V	-	-	0.1	V
		I_O = 20 µA; V_{CC} = 6.0 V	-	-	0.1	V
		I_O = 6.0 mA; V_{CC} = 4.5 V	-	-	0.4	V
		I_O = 7.8 mA; V_{CC} = 6.0 V	-	-	0.4	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 6.0 V	-	-	±1.0	µA
I_{OZ}	3-state OFF-state current	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 6.0 V; $V_O = V_{CC}$ or GND	-	-	±10.0	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	160	µA

11. Dynamic characteristics

Table 8: Dynamic characteristics

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF; see Figure 9.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb} = 25 °C							
t_{PHL}, t_{PLH}	propagation delay CP to $\overline{Q}$n	see Figure 6					
		V_{CC} = 2.0 V		-	50	165	ns
		V_{CC} = 4.5 V		-	18	33	ns
		V_{CC} = 6.0 V		-	14	28	ns
		V_{CC} = 5.0 V; C_L = 15 pF		-	15	-	ns
t_{PZH}, t_{PZL}	3-state output enable time $\overline{OE}$ to $\overline{Q}$n	see Figure 7					
		V_{CC} = 2.0 V		-	44	140	ns
		V_{CC} = 4.5 V		-	16	28	ns
		V_{CC} = 6.0 V		-	13	24	ns
t_{PHZ}, t_{PLZ}	3-state output disable time $\overline{OE}$ to $\overline{Q}$n	see Figure 7					
		V_{CC} = 2.0 V		-	50	135	ns
		V_{CC} = 4.5 V		-	18	27	ns
		V_{CC} = 6.0 V		-	14	23	ns
t_{THL}, t_{TLH}	output transition time	see Figure 6					
		V_{CC} = 2.0 V		-	14	60	ns
		V_{CC} = 4.5 V		-	5	12	ns
		V_{CC} = 6.0 V		-	4	10	ns
t_W	CP clock pulse width HIGH or LOW	see Figure 6					
		V_{CC} = 2.0 V		80	14	-	ns
		V_{CC} = 4.5 V		16	5	-	ns
		V_{CC} = 6.0 V		14	4	-	ns
t_{su}	set-up time Dn to CP	see Figure 8					
		V_{CC} = 2.0 V		60	6	-	ns
		V_{CC} = 4.5 V		12	2	-	ns
		V_{CC} = 6.0 V		10	2	-	ns
t_h	hold time Dn to CP	see Figure 8					
		V_{CC} = 2.0 V		5	0	-	ns
		V_{CC} = 4.5 V		5	0	-	ns
		V_{CC} = 6.0 V		5	0	-	ns
f_{max}	maximum clock frequency	see Figure 6					
		V_{CC} = 2.0 V		6.0	38	-	MHz
		V_{CC} = 4.5 V		30	115	-	MHz
		V_{CC} = 6.0 V		35	137	-	MHz
		V_{CC} = 5.0 V; C_L = 15 pF		-	127	-	MHz
C_{PD}	power dissipation capacitance per flip-flop	V_I = GND to V_{CC}	[1]	-	27	-	pF

Table 8: Dynamic characteristics *...continued*

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF; see Figure 9.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = −40 °C to +85 °C						
t_{PHL}, t_{PLH}	propagation delay CP to $\overline{Q}n$	see Figure 6				
		V_{CC} = 2.0 V	-	-	205	ns
		V_{CC} = 4.5 V	-	-	41	ns
		V_{CC} = 6.0 V	-	-	35	ns
t_{PZH}, t_{PZL}	3-state output enable time $\overline{OE}$ to $\overline{Q}n$	see Figure 7				
		V_{CC} = 2.0 V	-	-	175	ns
		V_{CC} = 4.5 V	-	-	35	ns
		V_{CC} = 6.0 V	-	-	30	ns
t_{PHZ}, t_{PLZ}	3-state output disable time $\overline{OE}$ to $\overline{Q}n$	see Figure 7				
		V_{CC} = 2.0 V	-	-	170	ns
		V_{CC} = 4.5 V	-	-	34	ns
		V_{CC} = 6.0 V	-	-	29	ns
t_{THL}, t_{TLH}	output transition time	see Figure 6				
		V_{CC} = 2.0 V	-	-	75	ns
		V_{CC} = 4.5 V	-	-	15	ns
		V_{CC} = 6.0 V	-	-	13	ns
t_W	CP clock pulse width HIGH or LOW	see Figure 6				
		V_{CC} = 2.0 V	100	-	-	ns
		V_{CC} = 4.5 V	20	-	-	ns
		V_{CC} = 6.0 V	17	-	-	ns
t_{su}	set-up time Dn to CP	see Figure 8				
		V_{CC} = 2.0 V	75	-	-	ns
		V_{CC} = 4.5 V	15	-	-	ns
		V_{CC} = 6.0 V	13	-	-	ns
t_h	hold time Dn to CP	see Figure 8				
		V_{CC} = 2.0 V	5	-	-	ns
		V_{CC} = 4.5 V	5	-	-	ns
		V_{CC} = 6.0 V	5	-	-	ns
f_{max}	maximum clock frequency	see Figure 6				
		V_{CC} = 2.0 V	4.8	-	-	MHz
		V_{CC} = 4.5 V	24	-	-	MHz
		V_{CC} = 6.0 V	28	-	-	MHz

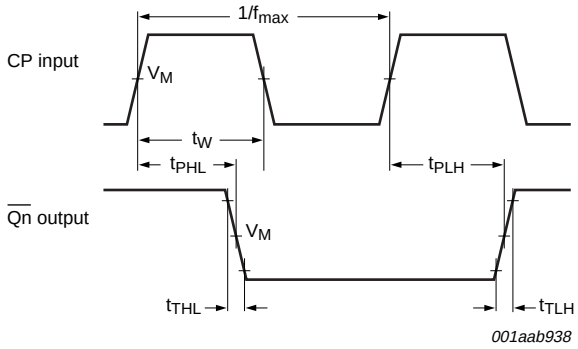
Table 8: Dynamic characteristics *...continued*

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF; see Figure 9.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = −40 °C to +125 °C						
t_{PHL}, t_{PLH}	propagation delay CP to $\overline{Q}n$	see Figure 6				
		V_{CC} = 2.0 V	-	-	250	ns
		V_{CC} = 4.5 V	-	-	50	ns
		V_{CC} = 6.0 V	-	-	43	ns
t_{PZH}, t_{PZL}	3-state output enable time $\overline{OE}$ to $\overline{Q}n$	see Figure 7				
		V_{CC} = 2.0 V	-	-	210	ns
		V_{CC} = 4.5 V	-	-	42	ns
		V_{CC} = 6.0 V	-	-	36	ns
t_{PHZ}, t_{PLZ}	3-state output disable time $\overline{OE}$ to $\overline{Q}n$	see Figure 7				
		V_{CC} = 2.0 V	-	-	205	ns
		V_{CC} = 4.5 V	-	-	41	ns
		V_{CC} = 6.0 V	-	-	35	ns
t_{THL}, t_{TLH}	output transition time	see Figure 6				
		V_{CC} = 2.0 V	-	-	90	ns
		V_{CC} = 4.5 V	-	-	18	ns
		V_{CC} = 6.0 V	-	-	15	ns
t_W	CP clock pulse width HIGH or LOW	see Figure 6				
		V_{CC} = 2.0 V	120	-	-	ns
		V_{CC} = 4.5 V	24	-	-	ns
		V_{CC} = 6.0 V	20	-	-	ns
t_{su}	set-up time Dn to CP	see Figure 8				
		V_{CC} = 2.0 V	90	-	-	ns
		V_{CC} = 4.5 V	18	-	-	ns
		V_{CC} = 6.0 V	15	-	-	ns
t_h	hold time Dn to CP	see Figure 8				
		V_{CC} = 2.0 V	5	-	-	ns
		V_{CC} = 4.5 V	5	-	-	ns
		V_{CC} = 6.0 V	5	-	-	ns
f_{max}	maximum clock frequency	see Figure 6				
		V_{CC} = 2.0 V	4.0	-	-	MHz
		V_{CC} = 4.5 V	20	-	-	MHz
		V_{CC} = 6.0 V	24	-	-	MHz

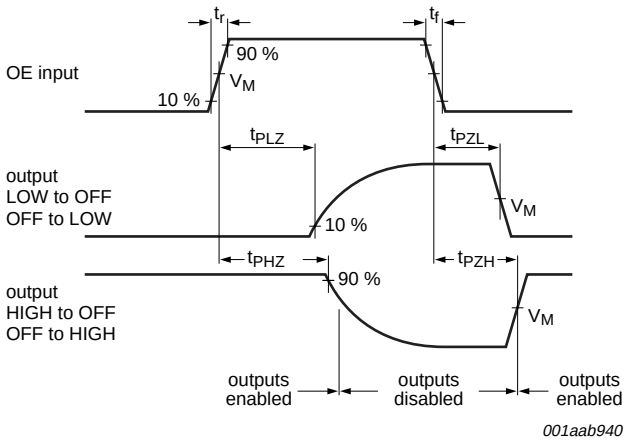
[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

12. Waveforms



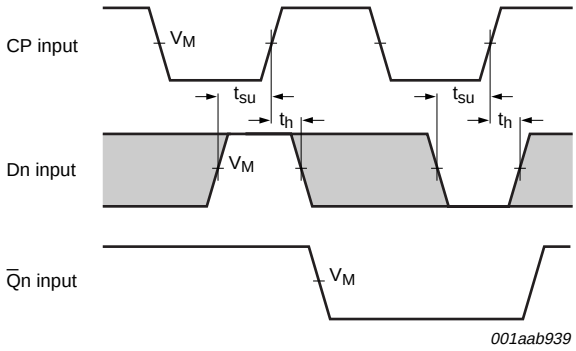
$V_M = 0.5 \times V_I$.

Fig 6. Waveforms showing the clock (CP) to output ($\overline{Qn}$) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency



$V_M = 0.5 \times V_I$.

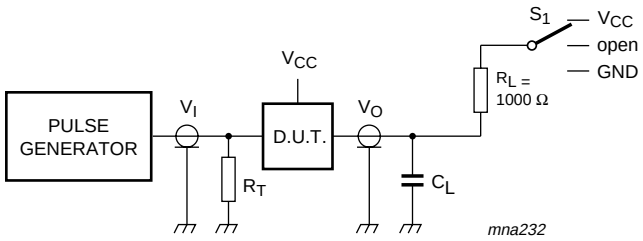
Fig 7. Waveforms showing the 3-state enable and disable times



The shaded areas indicate when the input is permitted to change for predictable output performance.

$V_M = 0.5 \times V_I$.

Fig 8. Waveforms showing the data set-up and hold times for the data input (Dn)



Test data is given in Table 9.

Definitions for test circuit:

R_L = Load resistor.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

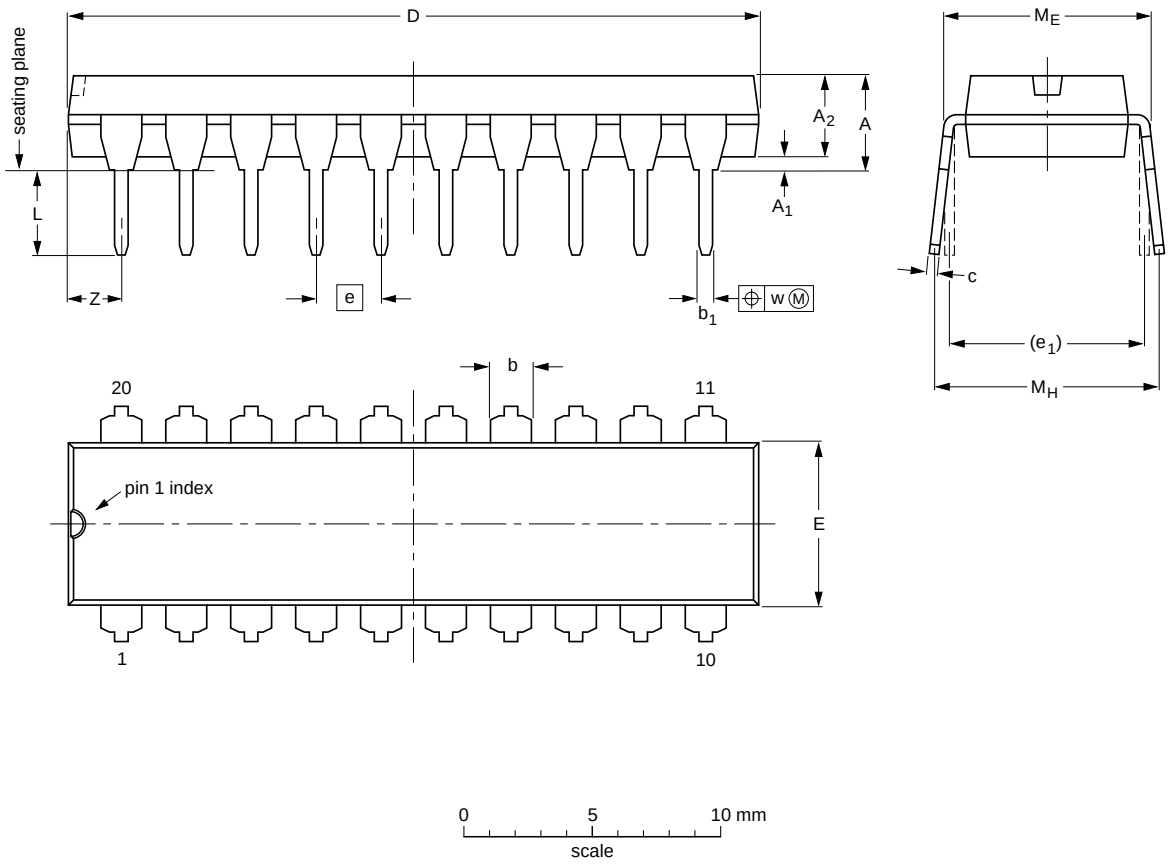
Fig 9. Load circuitry for switching times

Table 9: Test data

Supply	Input		Load		S_1		
V_{CC}	V_I	$t_r = t_f$	C_L	R_L	t_{PZL}, t_{PLZ}	t_{PZH}, t_{PHZ}	t_{PHL}, t_{PLH}
2.0 V	V_{CC}	6 ns	50 pF	1 kΩ	V_{CC}	GND	open
4.5 V	V_{CC}	6 ns	50 pF	1 kΩ	V_{CC}	GND	open
6.0 V	V_{CC}	6 ns	50 pF	1 kΩ	V_{CC}	GND	open
5.0 V	V_{CC}	6 ns	15 pF	1 kΩ	V_{CC}	GND	open

13. Package outline

DIP20: plastic dual in-line package; 20 leads (300 mil) **SOT146-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

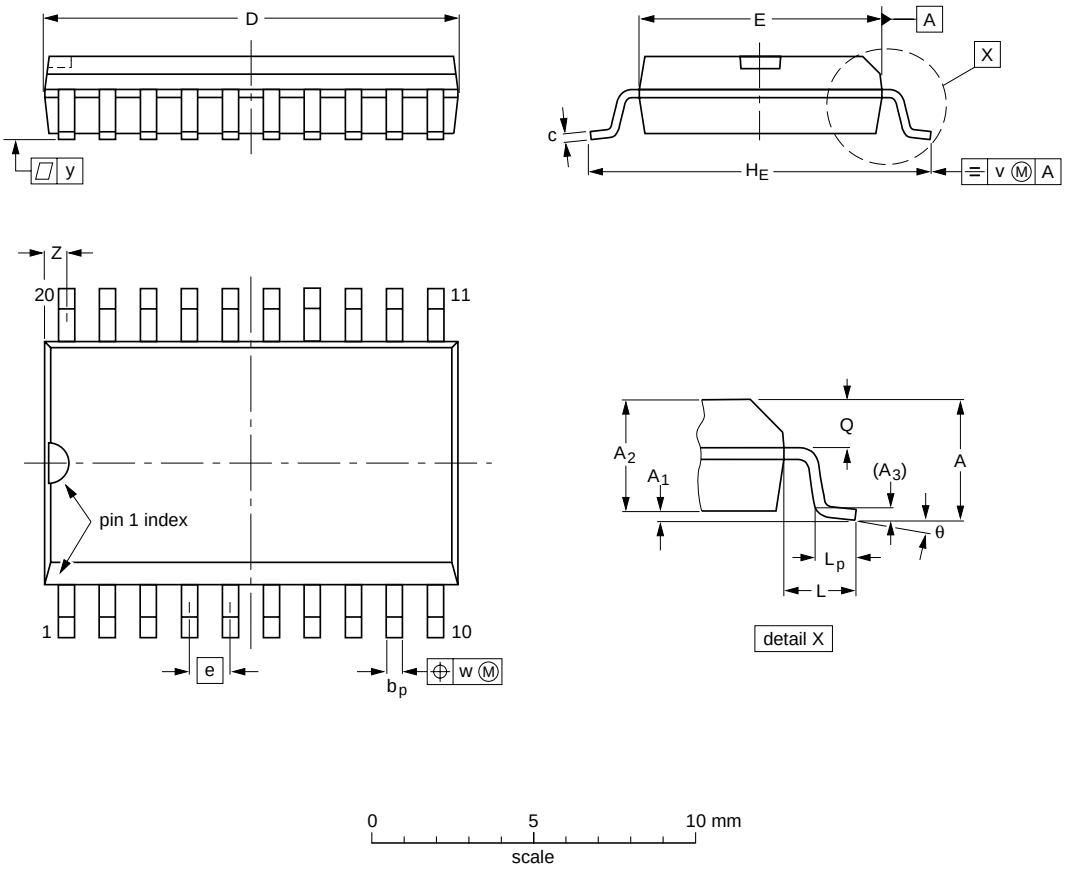
Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT146-1		MS-001	SC-603			~~99-12-27~~ 03-02-13

Fig 10. Package outline SOT146-1 (DIP20)

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				~~99-12-27~~ 03-02-19

Fig 11. Package outline SOT163-1 (SO20)

14. Revision history

Table 10: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
74HC564_3	20041111	Product data sheet	-	9397 750 13814	74HC_HCT564_CNV_2
Modifications:	• The format of this data sheet has been redesigned to comply with the current presentation and information standard of Philips Semiconductors. • Removed type number 74HCT564. • Inserted family specification.				
74HC_HCT564_CNV_2	19970905	Product specification	-	-	74HC_HCT564_1
74HC_HCT564_1	19901201	Product specification	-	-	-

15. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

16. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

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19. Contents

Date of release: 11 November 2004
Document number: 9397 750 13814

Published in The Netherlands