74LVC169

Presettable synchronous 4-bit up/down binary counter

Rev. 6 — 29 November 2012 | Product data sheet

1. General description

The 74LVC169 is a synchronous presettable 4-bit binary counter which features an internal look-ahead carry circuitry for cascading in high-speed counting applications. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs (pins Q0 to Q3) change simultaneously with each other when so instructed by the count-enable (pins $\overline{CEP}$ and $\overline{CET}$) inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock (pin CP) input triggers the four flip-flops on the LOW-to-HIGH transition of the clock.

The counter is fully programmable; that is, the outputs may be preset to any number between 0 and its maximum count. Presetting is synchronous with the clock and takes place regardless of the levels of the count enable inputs. A LOW level on the parallel enable (pin $\overline{PE}$) input disables the counter and causes the data at the Dn input to be loaded into the counter on the next LOW-to-HIGH transition of the clock. The direction of the counting is controlled by the up/down (pin U/$\overline{D}$) input. When pin U/$\overline{D}$ is HIGH, the counter counts up, when LOW, it counts down.

The look-ahead carry circuitry is provided for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable (pins $\overline{CEP}$ and $\overline{CET}$) inputs and a terminal count (pin $\overline{TC}$) output. Both count-enable (pins $\overline{CEP}$ and $\overline{CET}$) inputs must be LOW to count. Input pin $\overline{CET}$ is fed forward to enable the terminal count (pin $\overline{TC}$) output. Pin $\overline{TC}$ thus enabled will produce a LOW-level output pulse with a duration approximately equal to a HIGH level portion of pin Q0 output. The LOW level pin $\overline{TC}$ pulse is used to enable successive cascaded stages.

The 74LVC169 uses edge triggered J-K type flip-flops and has no constraints on changing the control of data input signals in either state of the clock. The only requirement is that the various inputs attain the desired state at least a set-up time before the next LOW-to-HIGH transition of the clock and remain valid for the recommended hold time thereafter.

The parallel load operation takes precedence over the other operations, as indicated in the mode select table. When pin $\overline{PE}$ is LOW, the data on the input pins D0 to D3 enters the flip-flops on the next LOW-to-HIGH transition of the clock.

In order for counting to occur, both pins $\overline{CEP}$ and $\overline{CET}$ must be LOW and pin $\overline{PE}$ must be HIGH. The pin U/$\overline{D}$ input determines the direction of the counting. The terminal count output pin $\overline{TC}$ output is normally HIGH and goes LOW, provided that pin $\overline{CET}$ is LOW, when a counter reaches 15 in the count up mode. The pin $\overline{TC}$ output state is not a function of the count-enable parallel (pin $\overline{CEP}$) input level. Since pin $\overline{TC}$ signal is derived by decoding the flip-flop states, there exists the possibility of decoding spikes on pin $\overline{TC}$. For this reason the use of pin $\overline{TC}$ as a clock signal is not recommended; see the following logic equations:

$$\text{count enable} = \overline{CEP} \bullet \overline{CET} \bullet \overline{PE}$$

$$\text{count up: TC} = Q3 \bullet Q2 \bullet Q1 \bullet Q0 \bullet CET \bullet U/\overline{D}$$

$$\text{count down: TC} = \overline{Q3} \bullet \overline{Q2} \bullet \overline{Q1} \bullet \overline{Q0} \bullet CET \bullet \overline{U}/D$$

2. Features and benefits

- 5 V tolerant inputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- Direct interface with TTL levels
- Up/down counting
- Two count enable inputs for n-bit cascading
- Built-in look-ahead carry capability
- Presettable for programmable operation
- Complies with JEDEC standard:
  - JESD8-7A (1.65 V to 1.95 V)
  - JESD8-5A (2.3 V to 2.7 V)
  - JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-B exceeds 200 V
  - CDM JESD22-C101E exceeds 1000 V
- Multiple package options
- Specified from –40 °C to +85 °C and from –40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Temperature range	Package		
		Name	Description	Version
74LVC169D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74LVC169DB	–40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74LVC169PW	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74LVC169BQ	–40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

4. Functional diagram

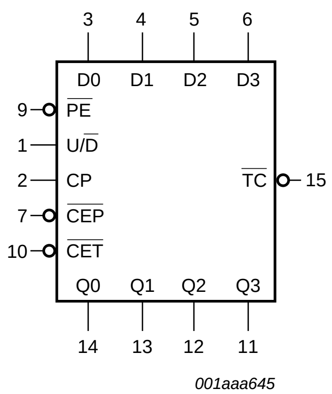


Fig 1. Logic symbol

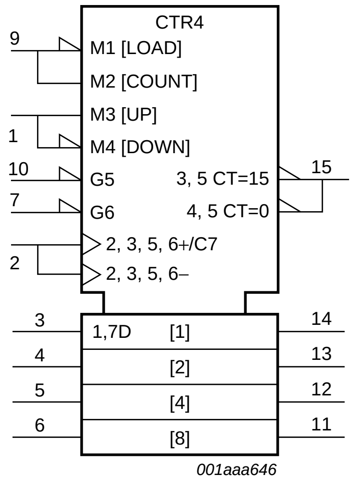


Fig 2. IEC logic symbol

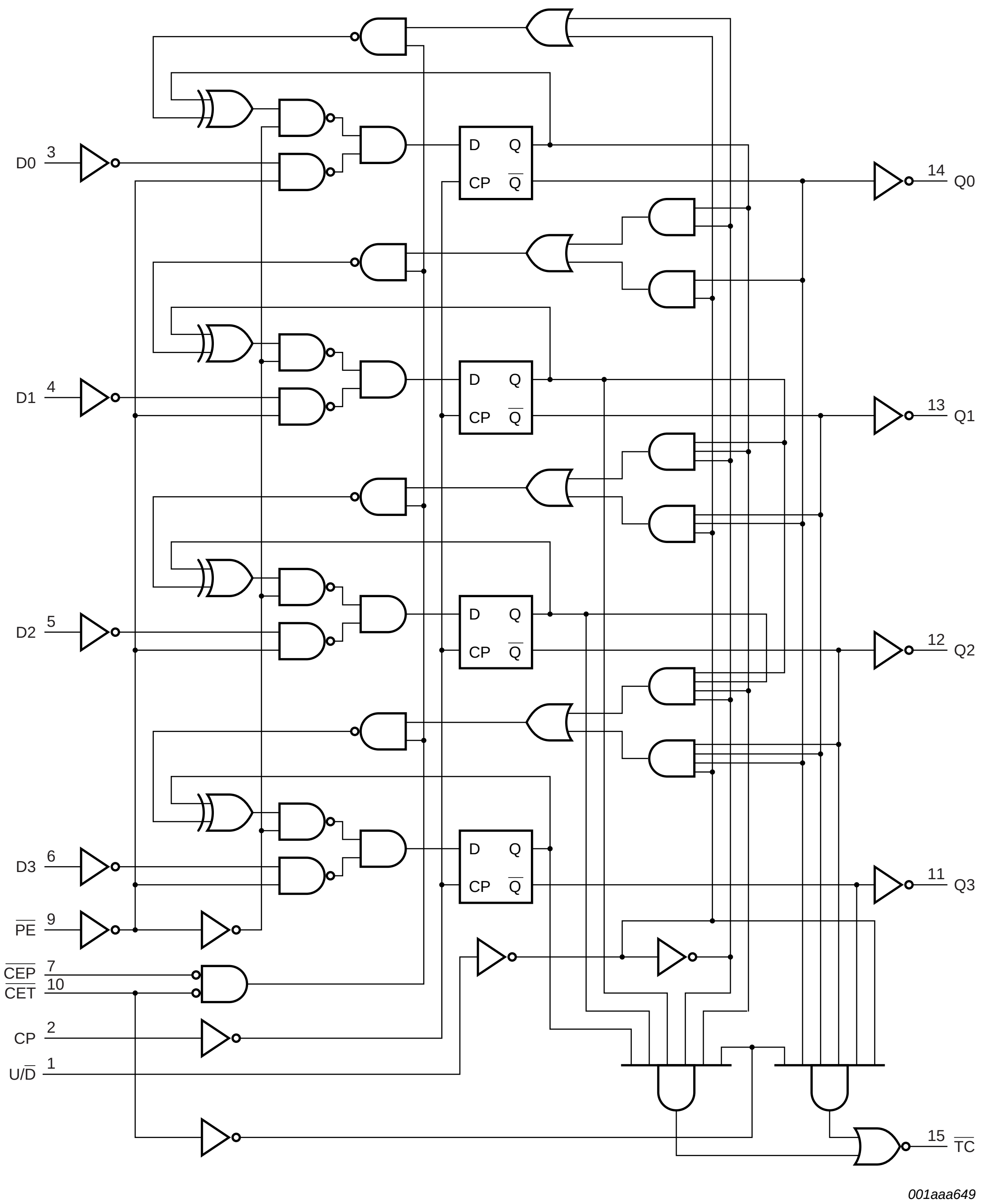


Fig 3. Logic diagram

5. Pinning information

5.1 Pinning

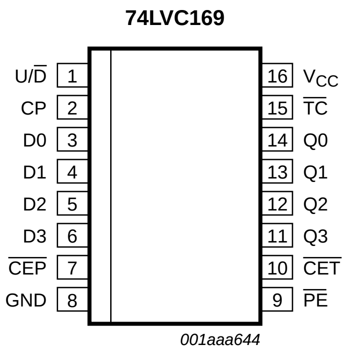
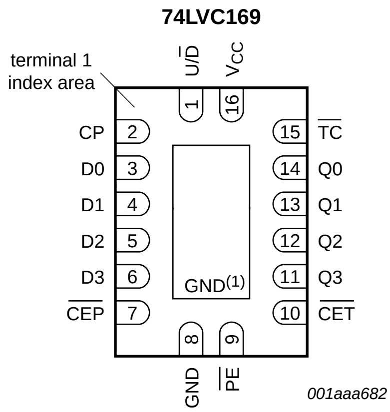


Fig 4. Pin configuration for SO16 and (T)SSOP16



Transparent top view

(1) This is not a supply pin. The substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However, if it is soldered, the solder land should remain floating or be connected to GND.

Fig 5. Pin configuration for DHVQFN16

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
U/$\overline{D}$	1	up/down control input
CP	2	clock input (LOW-to-HIGH, edge-triggered)
D0 to D3	3, 4, 5, 6	data input
$\overline{CEP}$	7	count enable input (active LOW)
GND	8	ground (0 V)
$\overline{PE}$	9	parallel enable input (active LOW)
$\overline{CET}$	10	count enable carry input (active LOW)
Q0 to Q3	14, 13, 12, 11	flip-flop output
$\overline{TC}$	15	terminal count output (active LOW)
V_{CC}	16	supply voltage

6. Functional description

Table 3. Function table[1]

Operating mode	Input						Output	
	CP	U/$\overline{D}$	$\overline{CEP}$	$\overline{CET}$	$\overline{PE}$	Dn	Qn	$\overline{TC}$
Parallel load (Dn to Qn)	↑	X	X	X	l	l	L	*
	↑	X	X	X	l	h	H	*
Count up (increment)	↑	h	l	l	h	X	count up	*
Count down (decrement)	↑	l	l	l	h	X	count down	*
Hold (do nothing)	↑	X	h	X	h	X	qn	*
	↑	X	X	X	h	X	qn	H

[1] H = HIGH voltage level steady state
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition
L = LOW voltage level steady state
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition
qn = Lower case letters indicate state of referenced output prior to the LOW-to-HIGH clock transition
X = don't care
↑ = LOW-to-HIGH clock transition
* = The $\overline{TC}$ is LOW when $\overline{CET}$ is LOW and the counter is at terminal count
Terminal count up is (HHHH) and terminal count down is (LLLL)

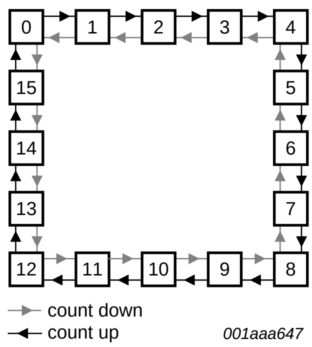
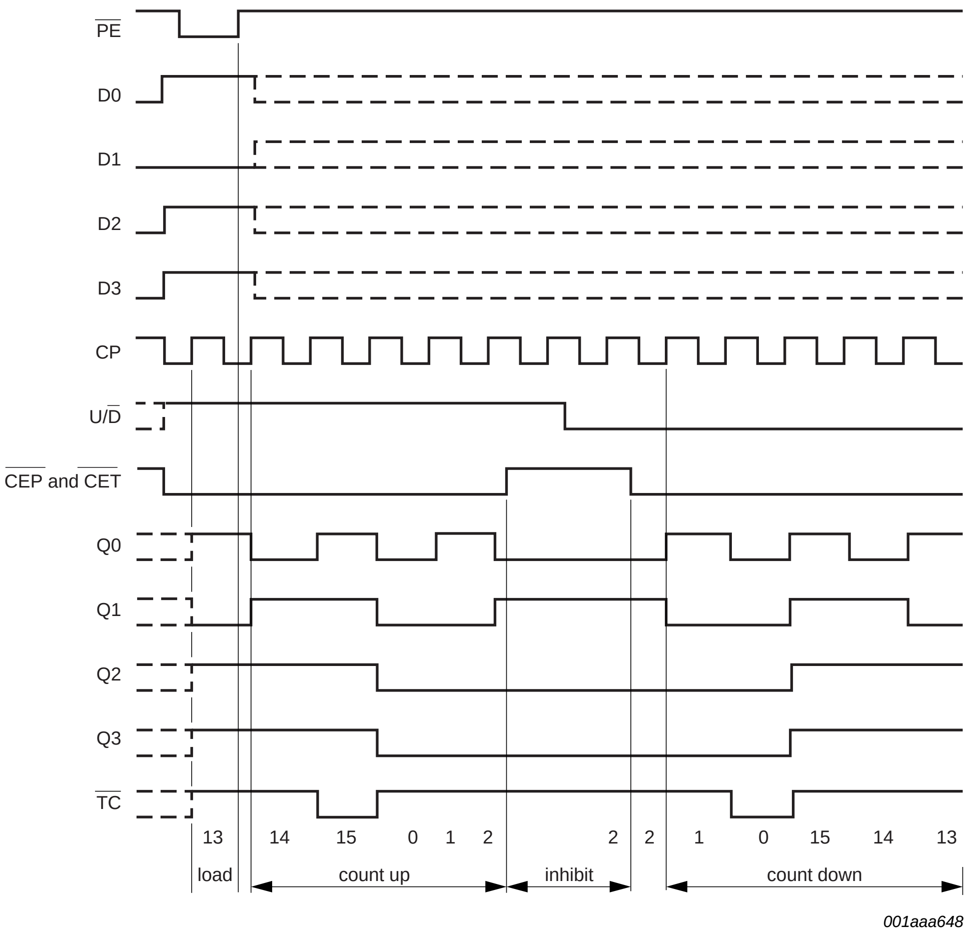


Fig 6. State diagram



The following sequence is illustrated:

- Load (preset) to thirteen.
- Count up to fourteen, fifteen (maximum), zero, one and two.
- Inhibit.
- Count down to one, zero (minimum), fifteen, fourteen and thirteen.

Fig 7. Typical timing sequence

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V		–50	-	mA
V_I	input voltage		[1]	–0.5	+5.5	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V		-	±50	mA
V_O	output voltage		[2]	–0.5	V_{CC} + 0.5	V
I_O	output current			-	±50	mA
I_{CC}	supply current			-	100	mA
I_{GND}	ground current			–100	-	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +125 °C	[3]	-	500	mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] For SO16 packages: above 70 °C the value of P_{tot} derates linearly with 8 mW/K.
For (T)SSOP16 packages: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.
For DHVQFN16 packages: above 60 °C the value of P_{tot} derates linearly with 4.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.65	-	3.6	V
		functional	1.2	-	-	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature	in free air	–40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 1.65 V to 2.7 V	0	-	20	ns/V
		V_{CC} = 2.7 V to 3.6 V	0	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V	1.08	-	-	1.08	-	V
		V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}	-	-	0.65 × V_{CC}	-	V
		V_{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V	-	-	0.12	-	0.12	V
		V_{CC} = 1.65 V to 1.95 V	-	-	0.35 × V_{CC}	-	0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = –100 µA; V_{CC} = 1.65 V to 3.6 V	V_{CC} – 0.2	-	-	V_{CC} – 0.3	-	V
		I_O = –4 mA; V_{CC} = 1.65 V	1.2	-	-	1.05	-	V
		I_O = –8 mA; V_{CC} = 2.3 V	1.8	-	-	1.65	-	V
		I_O = –12 mA; V_{CC} = 2.7 V	2.2	-	-	2.05	-	V
		I_O = –18 mA; V_{CC} = 3.0 V	2.4	-	-	2.25	-	V
		I_O = –24 mA; V_{CC} = 3.0 V	2.2	-	-	2.0	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = 100 µA; V_{CC} = 1.65 V to 3.6 V	-	-	0.2	-	0.3	V
		I_O = 4 mA; V_{CC} = 1.65 V	-	-	0.45	-	0.65	V
		I_O = 8 mA; V_{CC} = 2.3 V	-	-	0.6	-	0.8	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	-	0.4	-	0.6	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	-	0.55	-	0.8	V
I_I	input leakage current	V_{CC} = 3.6 V; V_I = 5.5 V or GND	-	±0.1	±5	-	±20	µA
I_{CC}	supply current	V_{CC} = 3.6 V; V_I = V_{CC} or GND; I_O = 0 A	-	0.1	10	-	40	µA
ΔI_{CC}	additional supply current	per input pin; V_{CC} = 2.7 V to 3.6 V; V_I = V_{CC} – 0.6 V; I_O = 0 A	-	5	500	-	5000	µA
C_I	input capacitance	V_{CC} = 0 V to 3.6 V; V_I = GND to V_{CC}	-	5.0	-	-	-	pF

[1] All typical values are measured at V_{CC} = 3.3 V (unless stated otherwise) and T_{amb} = 25 °C.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 13.

Symbol	Parameter	Conditions		–40 °C to +85 °C			–40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	CP to Qn; see Figure 8	[2]						
		V_{CC} = 1.2 V		-	17	-	-	-	ns
		V_{CC} = 1.65 V to 1.95 V		1.5	7.1	13.1	1.5	15.1	ns
		V_{CC} = 2.3 V to 2.7 V		2.4	4.1	7.4	2.4	8.6	ns
		V_{CC} = 2.7 V		1.5	3.9	7.2	1.5	9.0	ns
		V_{CC} = 3.0 V to 3.6 V		1.5	3.7	6.6	1.5	10.0	ns
		CP to $\overline{TC}$; see Figure 8	[2]						
		V_{CC} = 1.2 V		-	21	-	-	-	ns
		V_{CC} = 1.65 V to 1.95 V		2.0	8.5	14.9	2.0	17.2	ns
		V_{CC} = 2.3 V to 2.7 V		3.0	4.9	8.4	3.0	9.7	ns
		V_{CC} = 2.7 V		1.5	4.7	8.8	1.5	11.0	ns
		V_{CC} = 3.0 V to 3.6 V		1.5	4.4	7.5	1.5	9.5	ns
		$\overline{CET}$ to $\overline{TC}$; see Figure 9	[2]						
		V_{CC} = 1.2 V		-	19	-	-	-	ns
		V_{CC} = 1.65 V to 1.95 V		1.5	6.6	12.3	1.5	14.2	ns
		V_{CC} = 2.3 V to 2.7 V		2.2	3.8	7.0	2.2	8.1	ns
		V_{CC} = 2.7 V		1.5	4.0	7.2	1.5	9.0	ns
		V_{CC} = 3.0 V to 3.6 V		1.5	3.4	6.2	1.5	8.0	ns
		U/$\overline{D}$ to $\overline{TC}$; see Figure 10	[2]						
		V_{CC} = 1.2 V		-	21	-	-	-	ns
		V_{CC} = 1.65 V to 1.95 V		1.0	7.3	13.7	1.0	15.8	ns
		V_{CC} = 2.3 V to 2.7 V		1.7	4.2	7.7	1.7	8.9	ns
		V_{CC} = 2.7 V		1.5	4.4	8.2	1.5	10.5	ns
		V_{CC} = 3.0 V to 3.6 V		1.5	3.8	6.9	1.5	9.0	ns
t_W	pulse width	CP HIGH or LOW; see Figure 8							
		V_{CC} = 1.65 V to 1.95 V		6.0	-	-	6.0	-	ns
		V_{CC} = 2.3 V to 2.7 V		5.0	-	-	5.0	-	ns
		V_{CC} = 2.7 V		5.0	-	-	5.0	-	ns
		V_{CC} = 3.0 V to 3.6 V		4.0	1.2	-	4.0	-	ns

Table 7. Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 13.

Symbol	Parameter	Conditions		−40 °C to +85 °C			−40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
t_{su}	set-up time	Dn to CP; see Figure 11							
		V_{CC} = 1.65 V to 1.95 V		5.5	-	-	5.5	-	ns
		V_{CC} = 2.3 V to 2.7 V		4.5	-	-	4.5	-	ns
		V_{CC} = 2.7 V		3.0	-	-	3.0	-	ns
		V_{CC} = 3.0 V to 3.6 V		2.5	1.0	-	2.5	-	ns
		$\overline{PE}$ to CP; see Figure 11							
		V_{CC} = 1.65 V to 1.95 V		4.5	-	-	4.5	-	ns
		V_{CC} = 2.3 V to 2.7 V		4.0	-	-	4.0	-	ns
		V_{CC} = 2.7 V		3.5	-	-	3.5	-	ns
		V_{CC} = 3.0 V to 3.6 V		3.0	1.2	-	3.0	-	ns
		U/$\overline{D}$ to CP; see Figure 12							
		V_{CC} = 1.65 V to 1.95 V		9.0	-	-	9.0	-	ns
		V_{CC} = 2.3 V to 2.7 V		7.0	-	-	7.0	-	ns
		V_{CC} = 2.7 V		6.5	-	-	6.5	-	ns
		V_{CC} = 3.0 V to 3.6 V		5.5	2.8	-	5.5	-	ns
		$\overline{CEP}$, $\overline{CET}$ to CP; see Figure 12							
		V_{CC} = 1.65 V to 1.95 V		9.0	-	-	9.0	-	ns
		V_{CC} = 2.3 V to 2.7 V		6.0	-	-	6.0	-	ns
		V_{CC} = 2.7 V		5.5	-	-	5.5	-	ns
		V_{CC} = 3.0 V to 3.6 V		4.5	2.1	-	4.5	-	ns
t_h	hold time	Dn, $\overline{PE}$, $\overline{CEP}$, $\overline{CET}$, U/$\overline{D}$ to CP; see Figure 11 and 12							
		V_{CC} = 1.65 V to 1.95 V		1.0	-	-	1.0	-	ns
		V_{CC} = 2.3 V to 2.7 V		1.0	-	-	1.0	-	ns
		V_{CC} = 2.7 V		0.0	-	-	0.0	-	ns
		V_{CC} = 3.0 V to 3.6 V		0.5	0.0	-	0.5	-	ns
f_{max}	maximum frequency	see Figure 8							
		V_{CC} = 1.65 V to 1.95 V		100	-	-	80	-	MHz
		V_{CC} = 2.3 V to 2.7 V		125	-	-	100	-	MHz
		V_{CC} = 2.7 V		150	-	-	120	-	MHz
		V_{CC} = 3.0 V to 3.6 V		150	200	-	120	-	MHz
$t_{sk(o)}$	output skew time	V_{CC} = 3.0 V to 3.6 V	[3]	-	-	1.0	-	1.5	ns

Table 7. Dynamic characteristics *...continued*
Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 13.

Symbol	Parameter	Conditions		–40 °C to +85 °C			–40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
C_{PD}	power dissipation capacitance	per input pin; V_I = GND to V_{CC}	[4]						
		V_{CC} = 1.65 V to 1.95 V		-	12.7	-	-	-	pF
		V_{CC} = 2.3 V to 2.7 V		-	16.4	-	-	-	pF
		V_{CC} = 3.0 V to 3.6 V		-	19.7	-	-	-	pF

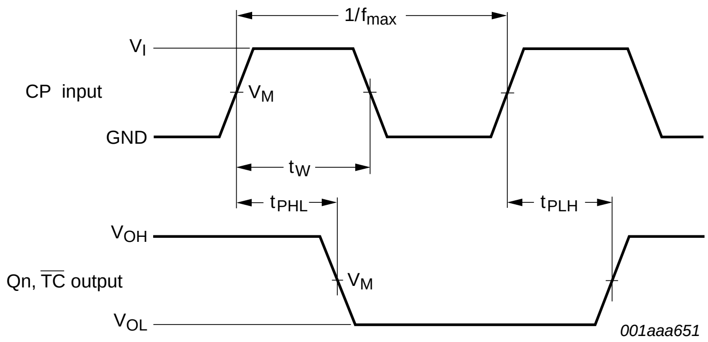
[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.2 V, 1.8 V, 2.5 V, 2.7 V and 3.3 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz; f_o = output frequency in MHz
C_L = output load capacitance in pF
V_{CC} = supply voltage in Volt
N = number of inputs switching
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

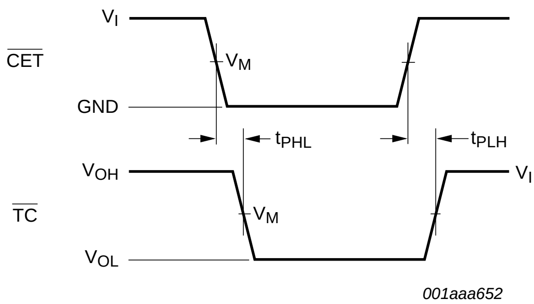
11. Waveforms



Measurement points are given in Table 8.

Logic levels: V_{OL} and V_{OH} are the typical output voltage levels that occur with the output load.

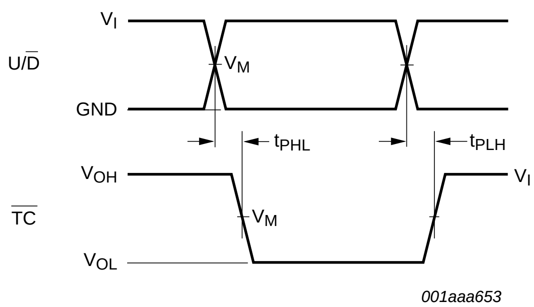
Fig 8. Clock (CP) to outputs (Qn, $\overline{TC}$) propagation delays, the clock pulse width, and the maximum frequency



Measurement points are given in Table 8.

Logic levels: V_{OL} and V_{OH} are the typical output voltage levels that occur with the output load.

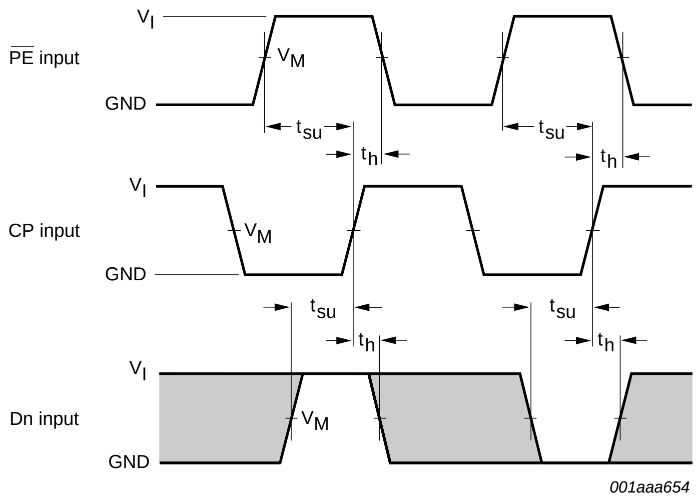
Fig 9. Input ($\overline{CET}$) to output ($\overline{TC}$) propagation delays



Measurement points are given in Table 8.

Logic levels: V_{OL} and V_{OH} are the typical output voltage levels that occur with the output load.

Fig 10. The up/down control input (U/$\overline{D}$) to output ($\overline{TC}$) propagation delays

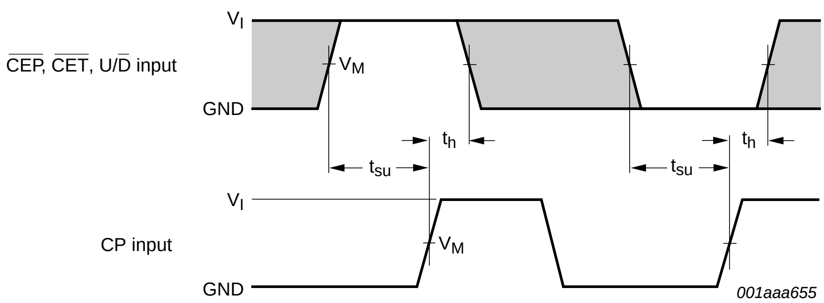


The shaded areas indicate when the input is permitted to change for predictable output performance.

Measurement points are given in Table 8.

Logic levels: V_{OL} and V_{OH} are the typical output voltage levels that occur with the output load.

Fig 11. Set-up and hold times for the input (Dn) and parallel enable input ($\overline{PE}$)



The shaded areas indicate when the input is permitted to change for predictable output performance.

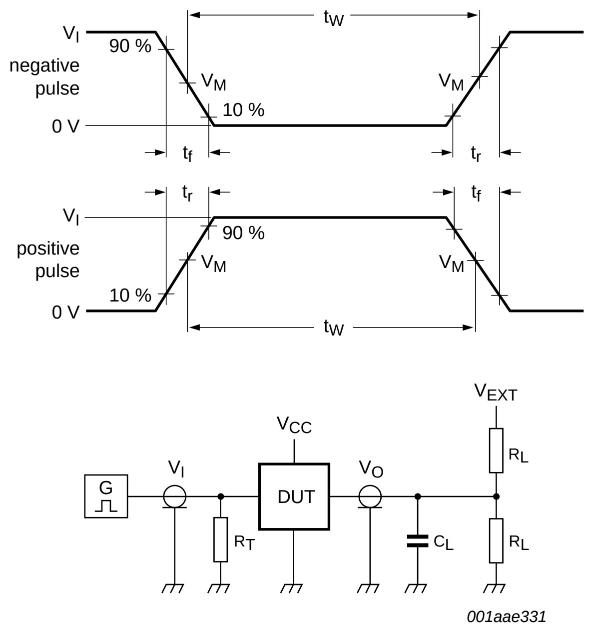
Measurement points are given in Table 8.

Logic levels: V_{OL} and V_{OH} are the typical output voltage levels that occur with the output load.

Fig 12. Set-up and hold times for count enable inputs ($\overline{CEP}$ and $\overline{CET}$) and control input (U/$\overline{D}$)

Table 8. Measurement points

Supply voltage	Input		Output
V_{CC}	V_I	V_M	V_M
1.2 V	V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
1.65 V to 1.95 V	V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.3 V to 2.7 V	V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.7 V	2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V



Test data is given in Table 9.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig 13. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		S1 position
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}
1.2 V	V_{CC}	≤ 2 ns	30 pF	1 kΩ[1]	open
1.65 V to 1.95 V	V_{CC}	≤ 2 ns	30 pF	1 kΩ[1]	open
2.3 V to 2.7 V	V_{CC}	≤ 2 ns	30 pF	500 Ω	open
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open

[1] The circuit performs better when R_L = 1000 kΩ.

12. Application information

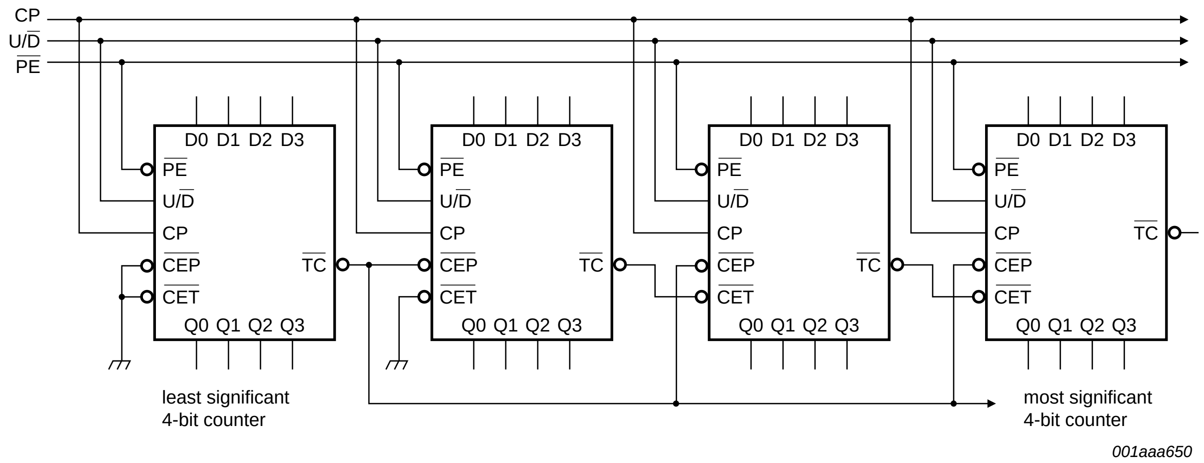
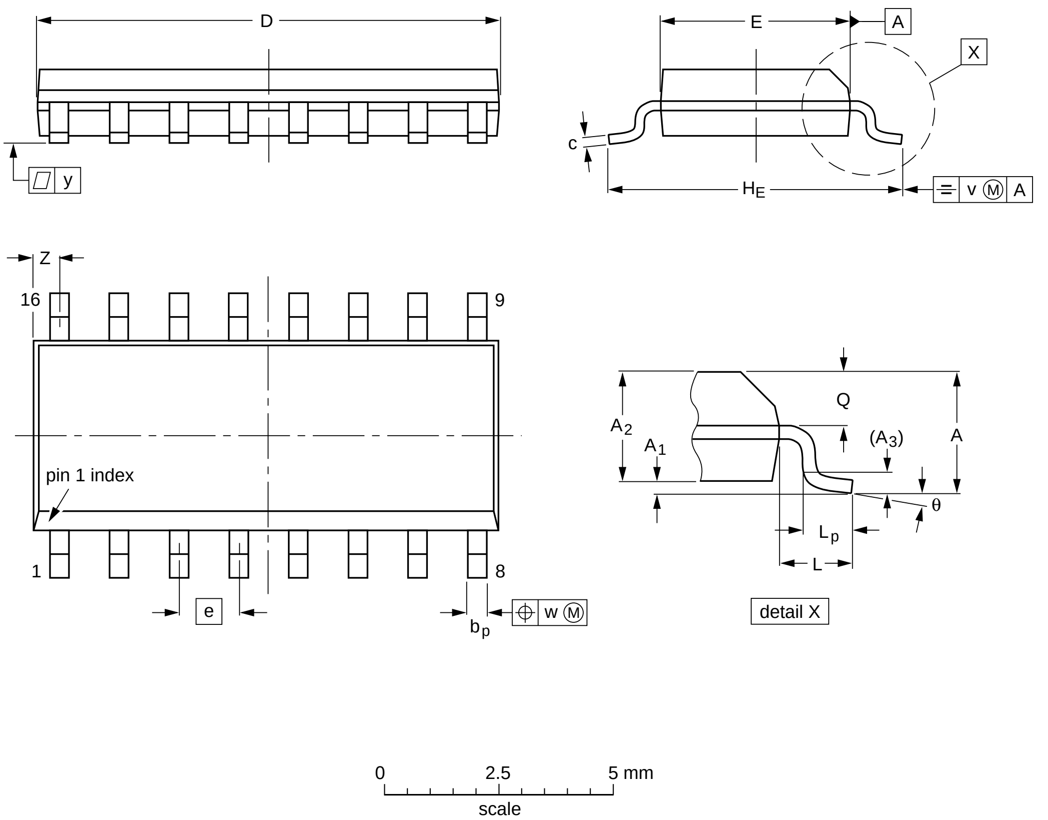


Fig 14. Synchronous multistage counting scheme

13. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

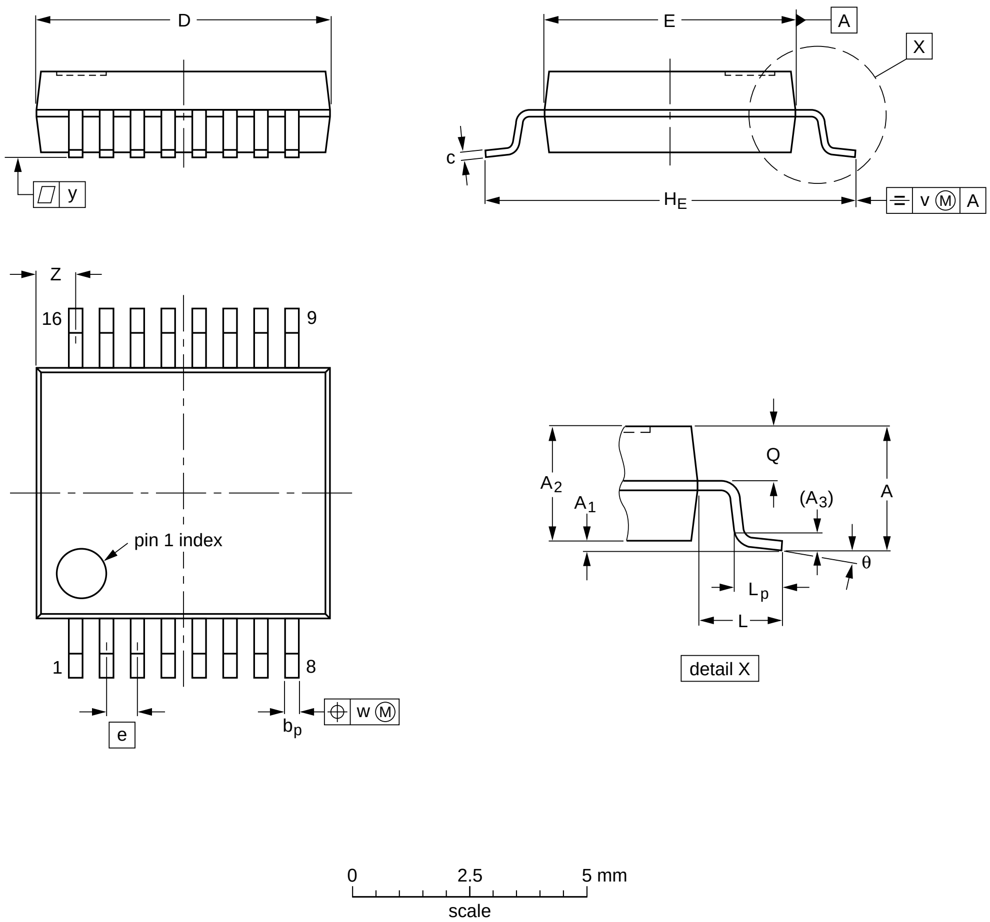
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 15. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

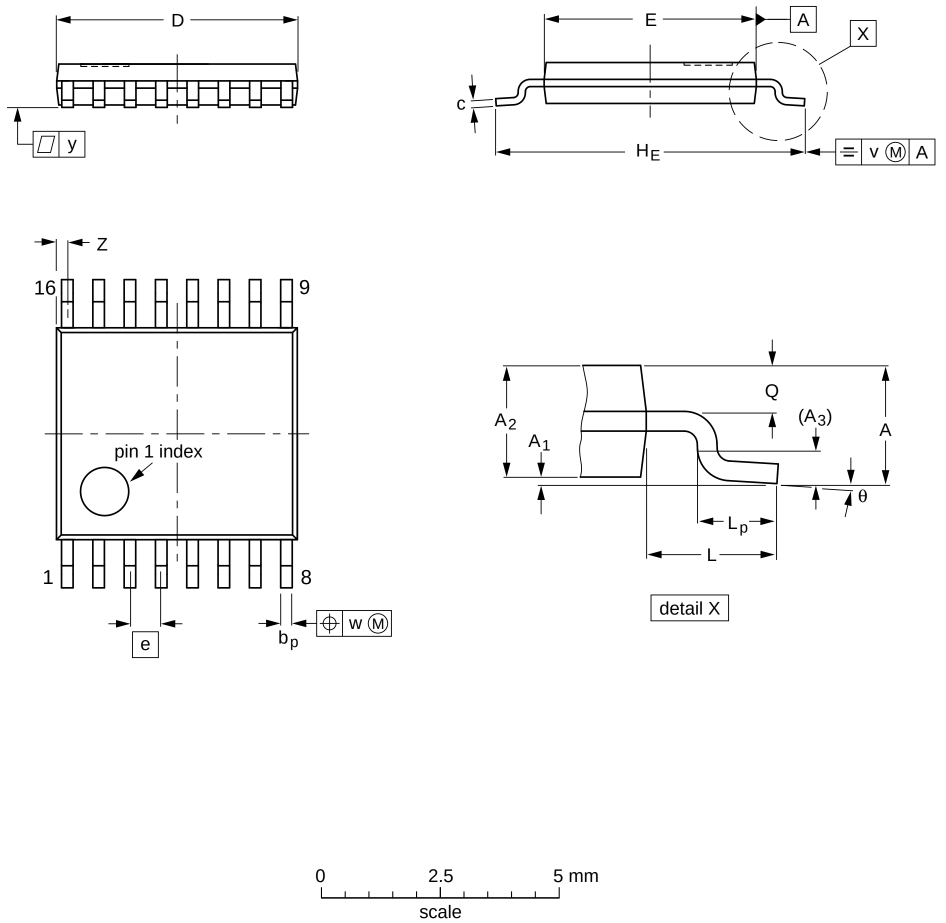
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT338-1		MO-150				~~99-12-27~~ 03-02-19

Fig 16. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

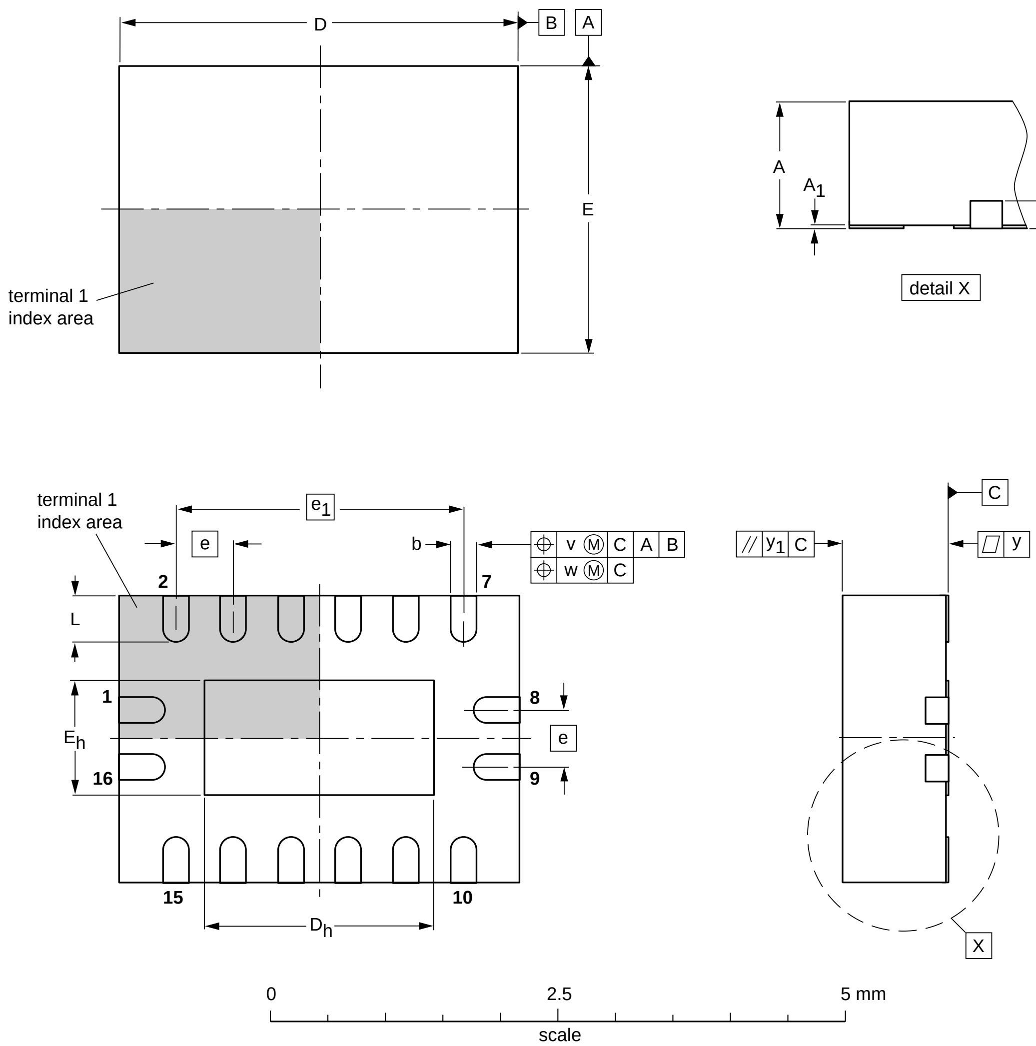
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 17. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm **SOT763-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.6 3.4	2.15 1.85	2.6 2.4	1.15 0.85	0.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT763-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig 18. Package outline SOT763-1 (DHVQFN16)

14. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

15. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC169 v.6	20121129	Product data sheet	-	74LVC169 v.5
Modifications:	• Table 4, Table 5, Table 6, Table 7, Table 8 and Table 9: values added for lower voltage ranges.			
74LVC169 v.5	20090608	Product data sheet	-	74LVC169 v.4
74LVC169 v.4	20041014	Product specification	-	74LVC169 v.3
74LVC169 v.3	20040512	Product specification	-	74LVC169 v.2
74LVC169 v.2	19980520	Product specification	-	74LVC169 v.1
74LVC169 v.1	19960823	Product specification	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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18. Contents

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