

74LVT273

3.3 V octal D-type flip-flop

Rev. 03 — 10 September 2008

Product data sheet

1. General description

The 74LVT273 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3 V.

This device has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset (\overline{MR}) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced LOW independent of the clock or data inputs by a LOW voltage level on the \overline{MR} input. The device is useful for applications where only the true output is required and the CP and \overline{MR} are common elements.

2. Features

- Eight edge-triggered D-type flip-flops
- Buffered common clock and asynchronous master reset
- Input and output interface capability to systems at 5 V supply
- TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- Output capability: +64 mA/−32 mA
- Latch-up protection
 - ◆ JESD78 Class II exceeds 500 mA
- ESD protection:
 - ◆ HBM JESD22-A114E exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
- Bus-hold data inputs eliminate the need for external pull-up resistors for unused inputs
- Live insertion/extraction permitted
- Power-up reset
- No bus current loading when output is tied to 5 V bus

3. Ordering information

Table 1. Ordering information

| Type number | Package | | | Version |
|-------------|-------------------|----------|---|----------|
| | Temperature range | Name | Description | |
| 74LVT273D | -40 °C to +125 °C | SO20 | plastic small outline package; 20 leads; body width 7.5 mm | SOT163-1 |
| 74LVT273DB | -40 °C to +125 °C | SSOP20 | plastic shrink small outline package; 20 leads; body width 5.3 mm | SOT339-1 |
| 74LVT273PW | -40 °C to +125 °C | TSSOP20 | plastic thin shrink small outline package; 20 leads; body width 4.4 mm | SOT360-1 |
| 74LVT273BQ | -40 °C to +125 °C | DHVQFN20 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm | SOT764-1 |

4. Functional diagram

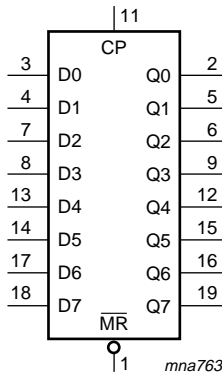


Fig 1. Logic symbol

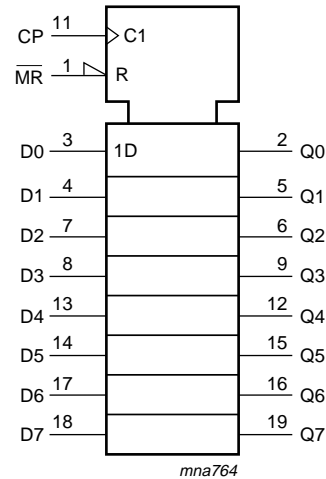


Fig 2. IEC logic symbol

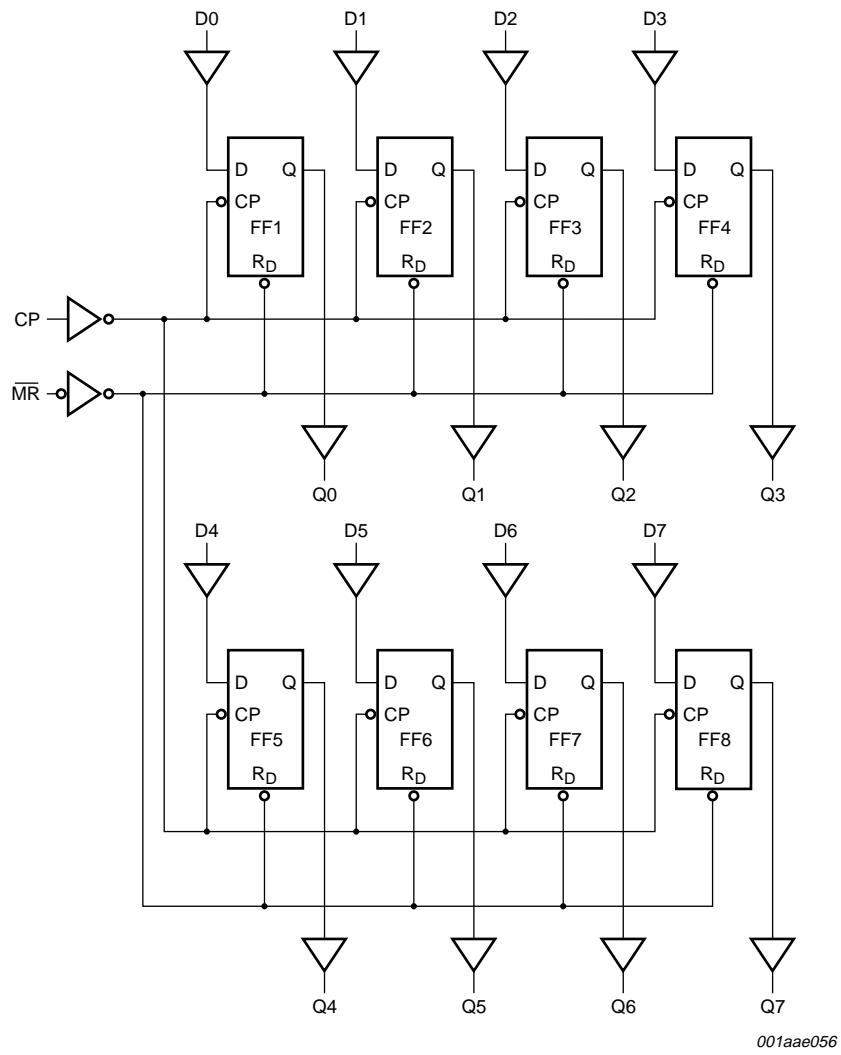
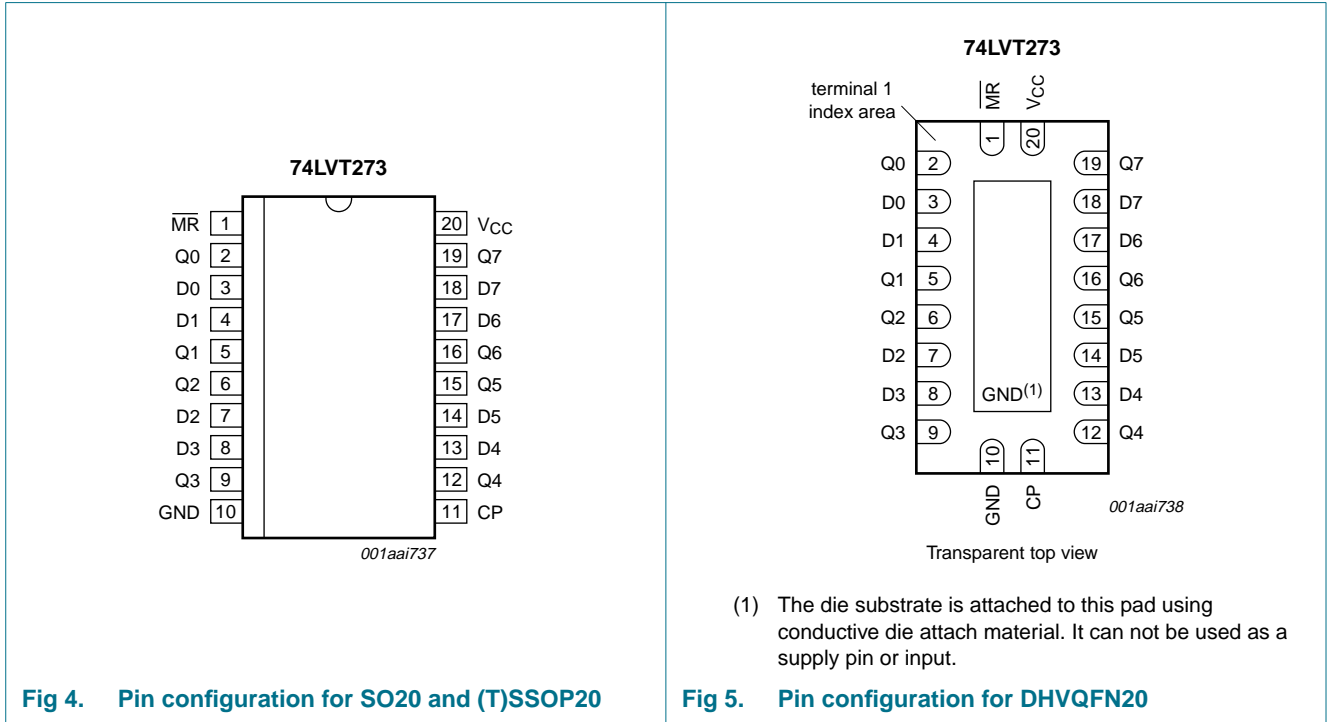


Fig 3. Logic diagram

5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|-----------------|----------------------------|---|
| MR | 1 | master reset input (active LOW) |
| Q0 to Q7 | 2, 5, 6, 9, 12, 15, 16, 19 | data output |
| D0 to D7 | 3, 4, 7, 8, 13, 14, 17, 18 | data input |
| GND | 10 | ground (0 V) |
| CP | 11 | clock pulse input (active on rising edge) |
| V _{CC} | 20 | positive supply voltage |

6. Functional description

Table 3. Function selection

| Inputs | | | Outputs | Operating mode |
|--------|----|----|---------|----------------|
| MR | CP | Dn | Qn | |
| L | X | X | L | Reset (clear) |
| H | ↑ | h | H | Load 1 |
| H | ↑ | l | L | Load 0 |
| H | L | X | Q0 | Retain state |

- [1] H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the prior to the LOW-to-HIGH clock transition;
 L = LOW voltage level; l = LOW voltage level one set-up time prior to the prior to the LOW-to-HIGH clock transition;
 X = Don't care; ↑ = LOW-to-HIGH clock transition; Q0 = output as it was.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------|-------------------------|-------------------------------------|----------|------|------|
| V _{CC} | supply voltage | | -0.5 | +4.6 | V |
| V _I | input voltage | | [1] -0.5 | +7.0 | V |
| V _O | output voltage | Output in OFF or HIGH state | [1] -0.5 | +7.0 | V |
| I _{IK} | input clamping current | V _I < 0 V | -50 | - | mA |
| I _{OK} | output clamping current | V _O < 0 V | -50 | - | mA |
| I _O | output current | output in LOW state | - | 128 | mA |
| | | output in HIGH state | -64 | - | mA |
| T _{stg} | storage temperature | | -65 | +150 | °C |
| T _j | junction temperature | | [2] - | 150 | °C |
| P _{tot} | total power dissipation | T _{amb} = -40 °C to +85 °C | [3] | 500 | mW |

- [1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
 [2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.
 [3] For SO20 packages: above 70 °C derate linearly with 8 mW/K.
 For SSOP20 and TSSOP20 packages: above 60 °C derate linearly with 5.5 mW/K.
 For DHVQFN20 packages: above 60 °C derate linearly with 4.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------|---------------------------|------------|-----|-----|-----|------|
| V _{CC} | supply voltage | | 2.7 | - | 3.6 | V |
| V _I | input voltage | | 0 | - | 5.5 | V |
| I _{OH} | HIGH-level output current | | -32 | - | - | mA |

Table 5. Recommended operating conditions ...continued

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|--|-------------|-----|-----|-----|------|
| I_{OL} | LOW-level output current | | - | - | 64 | mA |
| T_{amb} | ambient temperature | in free air | -40 | - | +85 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate; output enabled | | - | - | 10 | ns/V |

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | Unit |
|--------------|-----------------------------------|--|-------------------|--------------------|-----------|---------------|
| | | | Min | Typ ^[1] | Max | |
| V_{IK} | input clamping voltage | $V_{CC} = 2.7V; I_{IK} = -18\text{ mA}$ | -1.2 | -0.9 | - | V |
| V_{IH} | HIGH-level input voltage | | 2.0 | - | - | V |
| V_{IL} | LOW-level input voltage | | - | - | 0.8 | |
| V_{OH} | HIGH-level output voltage | $V_{CC} = 2.7\text{ V to }3.6V; I_{OH} = -100\ \mu\text{A}$ | $V_{CC} - 0.2$ | $V_{CC} - 0.1$ | - | V |
| | | $V_{CC} = 2.7\text{ V}; I_{OH} = -8\text{ mA}$ | 2.4 | 2.5 | - | V |
| | | $V_{CC} = 3.0\text{ V}; I_{OH} = -32\text{ mA}$ | 2.0 | 2.2 | - | V |
| V_{OL} | LOW-level output voltage | $V_{CC} = 2.7\text{ V}; I_{OL} = 100\ \mu\text{A}$ | | 0.1 | 0.2 | V |
| | | $V_{CC} = 2.7\text{ V}; I_{OL} = 24\text{ mA}$ | - | 0.3 | 0.5 | V |
| | | $V_{CC} = 3.0\text{ V}; I_{OL} = 16\text{ mA}$ | - | 0.25 | 0.4 | V |
| | | $V_{CC} = 3.0\text{ V}; I_{OL} = 32\text{ mA}$ | - | 0.3 | 0.5 | V |
| | | $V_{CC} = 3.0\text{ V}; I_{OL} = 64\text{ mA}$ | - | 0.4 | 0.55 | V |
| $V_{OL(pu)}$ | power-up LOW-level output voltage | $V_{CC} = 3.6\text{ V}; I_O = 1\text{ mA}; V_I = \text{GND or } V_{CC}$ ^[2] | - | 0.13 | 0.55 | V |
| I_I | input leakage current | input pins | | | | |
| | | $V_{CC} = 0\text{ V or }3.6\text{ V}; V_I = 5.5\text{ V}$ | - | 1 | 10 | μA |
| | | control pins | | | | |
| | | $V_{CC} = 3.6\text{ V}; V_I = V_{CC}\text{ or GND}$ | - | ± 0.1 | ± 1 | μA |
| | | data pins ^[3] | | | | |
| | | $V_{CC} = 3.6\text{ V}; V_I = V_{CC}$ | - | 0.1 | 1 | μA |
| I_{OFF} | power-off leakage current | $V_{CC} = 0\text{ V}; V_I\text{ or }V_O = 0\text{ V to }4.5\text{ V}$ | - | 1 | ± 100 | μA |
| I_{LO} | output leakage current | $V_{CC} = 3.0\text{ V}; V_O = 5.5\text{ V}; \text{output HIGH}$ | - | 60 | 125 | μA |
| I_{BHL} | bus hold LOW current | $V_{CC} = 3.0\text{ V}; V_I = 0.8\text{ V}$ | ^[4] 75 | 150 | - | μA |
| I_{BHH} | bus hold HIGH current | $V_{CC} = 3.0\text{ V}; V_I = 2.0\text{ V}$ | - | -150 | -75 | μA |
| I_{BHHO} | bus hold HIGH overdrive current | $V_{CC} = 3.6\text{ V}; V_I = 0\text{ V to }3.6\text{ V}$ | - | - | 500 | μA |
| I_{BHLO} | bus hold LOW overdrive current | $V_{CC} = 3.6\text{ V}; V_I = 0\text{ V to }3.6\text{ V}$ | -500 | - | - | μA |

Table 6. Static characteristics ...continued

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | Unit |
|------------------|---------------------------|---|------------------|--------------------|------|------|
| | | | Min | Typ ^[1] | Max | |
| I _{CC} | supply current | V _{CC} = 3.6 V; V _I = V _{CC} or GND; I _O = 0 A | | | | |
| | | outputs HIGH | - | 0.13 | 0.19 | mA |
| | | outputs LOW | - | 3 | 12 | mA |
| ΔI _{CC} | additional supply current | per input pin; V _{CC} = 3.0 V to 3.6 V; one input = V _{CC} - 0.6 V other inputs at V _{CC} or GND | [5] | 0.1 | 0.2 | mA |
| C _I | input capacitance | V _I = 0 V or 3.0 V | - | 4 | - | pF |

[1] All typical values are measured at V_{CC} = 3.3 V (unless stated otherwise) and T_{amb} = 25 °C.

[2] For valid test results data must not be loaded into the flip-flops (or latches) after applying the power.

[3] Unused pins at V_{CC} or GND.

[4] This is the bus hold overdrive current required to force the input to the opposite logic state.

[5] Increase in supply current for each input at the specified voltage level other than V_{CC} or GND

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 9](#).

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | Unit |
|------------------|-------------------------------|---|------------------|--------------------|-----|------|
| | | | Min | Typ ^[1] | Max | |
| t _{PLH} | LOW to HIGH propagation delay | CP to Qn; Figure 6 | | | | |
| | | V _{CC} = 2.7 V | - | - | 6.3 | ns |
| | | V _{CC} = 3.3 V ± 0.3 V | 1.7 | 3.5 | 5.5 | ns |
| t _{PHL} | HIGH to LOW propagation delay | CP to Qn; Figure 6 | | | | |
| | | V _{CC} = 2.7 V | - | - | 5.9 | ns |
| | | V _{CC} = 3.3 V ± 0.3 V | 1.9 | 3.5 | 5.5 | ns |
| | | MR to Qn; see Figure 7 | | | | |
| | | V _{CC} = 2.7 V | - | - | 6.2 | ns |
| | | V _{CC} = 3.3 V ± 0.3 V | 1.3 | 3.2 | 6.2 | ns |
| t _{su} | set-up time | Dn to CP HIGH; see Figure 7 [2] | | | | |
| | | V _{CC} = 2.7 V | 2.7 | - | - | ns |
| | | V _{CC} = 3.3 V ± 0.3 V | 2.3 | 1.0 | - | ns |
| | | Dn to CP LOW; see Figure 7 | | | | |
| | | V _{CC} = 2.7 V | 2.7 | - | - | ns |
| | | V _{CC} = 3.3 V ± 0.3 V | 2.3 | 1.0 | - | ns |
| t _h | hold time | Dn to CP HIGH; see Figure 8 [3] | | | | |
| | | V _{CC} = 2.7 V | 0 | - | - | ns |
| | | V _{CC} = 3.3 V ± 0.3 V | 0 | -0.6 | - | ns |
| | | Dn to CP LOW; see Figure 8 | | | | |
| | | V _{CC} = 2.7 V | 0 | - | - | ns |
| | | V _{CC} = 3.3 V ± 0.3 V | 0 | -0.6 | - | ns |

Table 7. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 9](#).

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | Unit |
|-----------|-------------------|---|------------------|--------------------|-----|------|
| | | | Min | Typ ^[1] | Max | |
| t_W | pulse width | CP input HIGH or LOW; see Figure 6 ^[4] | | | | |
| | | $V_{CC} = 2.7\text{ V}$ | 3.3 | - | - | ns |
| | | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | 3.3 | 1.5 | - | ns |
| | | \overline{MR} input LOW; see Figure 7 | | | | |
| | | $V_{CC} = 2.7\text{ V}$ | 3.3 | - | - | ns |
| | | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | 3.3 | 1.5 | - | ns |
| t_{rec} | recovery time | see Figure 7 | | | | |
| | | $V_{CC} = 2.7\text{ V}$ | 3.2 | - | - | ns |
| | | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | 2.7 | 1.0 | - | ns |
| f_{max} | maximum frequency | CP input; see Figure 7 | 150 | - | - | MHz |

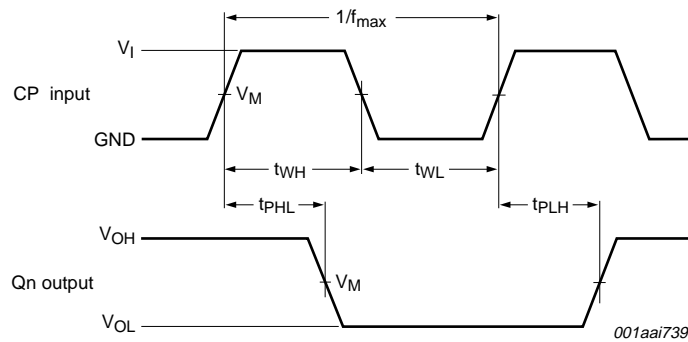
[1] Typical values are measured at $T_{amb} = 25\text{ °C}$ and $V_{CC} = 3.3\text{ V}$

[2] t_{su} is the same as $t_{su(L)}$ and $t_{su(H)}$

[3] t_h is the same as $t_{h(L)}$ and $t_{h(H)}$

[4] t_W is the same as t_{WL} and t_{WH}

11. Waveforms



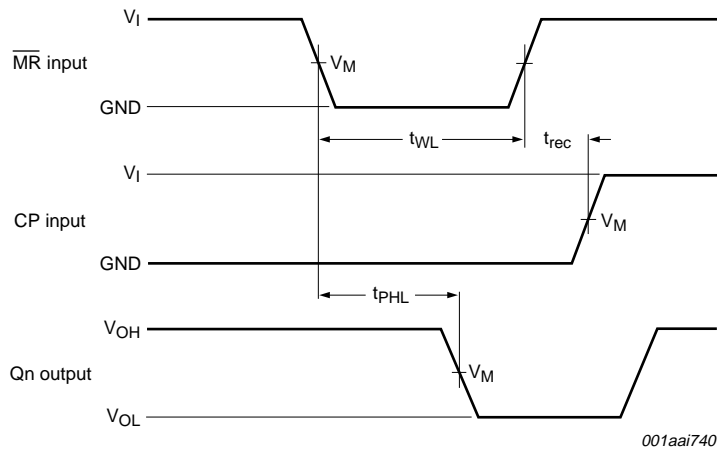
see [Table 8](#) for measurement points.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 6. CP Input to Qn output propagation delays and clock pulse width and maximum frequency

Table 8. Measurement points

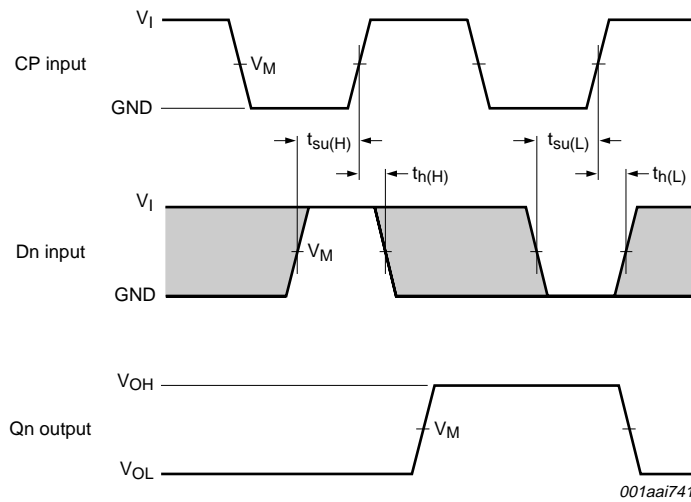
| Input | | Output |
|-------|-------|--------|
| V_I | V_M | V_M |
| 2.7 V | 1.5 V | 1.5 V |



see [Table 8](#) for measurement points.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 7. \overline{MR} pulse width, \overline{MR} to CP recovery time and \overline{MR} to Qn delay

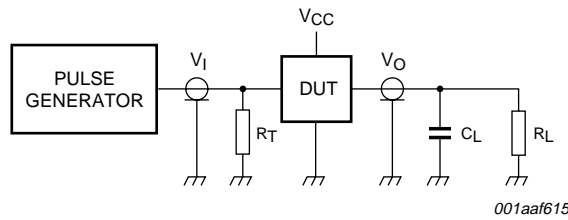
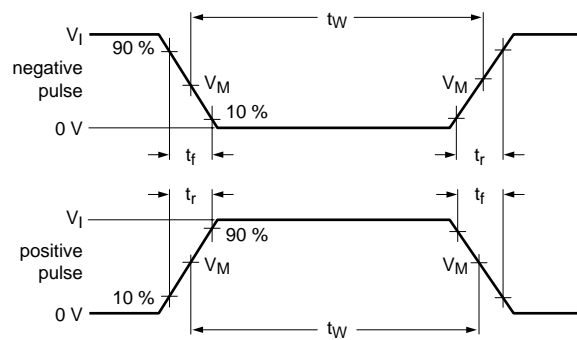


see [Table 8](#) for measurement points.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

The shaded areas indicate when the input is permitted to change for predicable output performance.

Fig 8. Data set-up and hold times



Test data is given in given in [Table 9](#).

Definitions for test circuit:

R_L = Load resistance;

C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

Fig 9. Load circuitry for switching times

Table 9. Test data

| Input | | | | Load | |
|-------|-----------------|--------|------------|-------|-------|
| V_I | Repetition rate | t_W | t_r, t_f | R_L | C_L |
| 2.7 V | ≤ 10 MHz | 500 ns | ≤ 2.5 ns | 500 Ω | 50 pF |

12. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

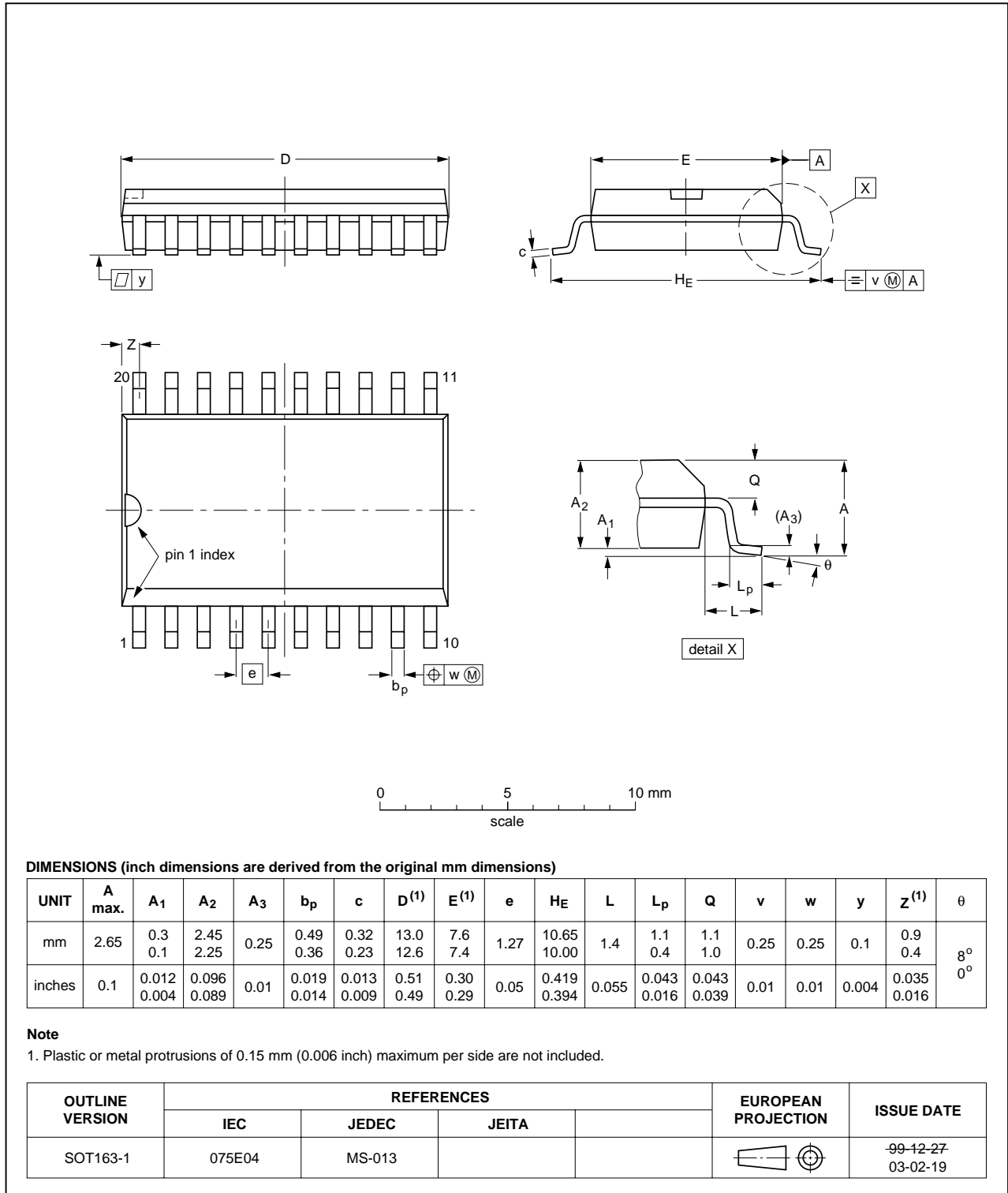


Fig 10. Package outline SOT163-1 (SO20)

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1

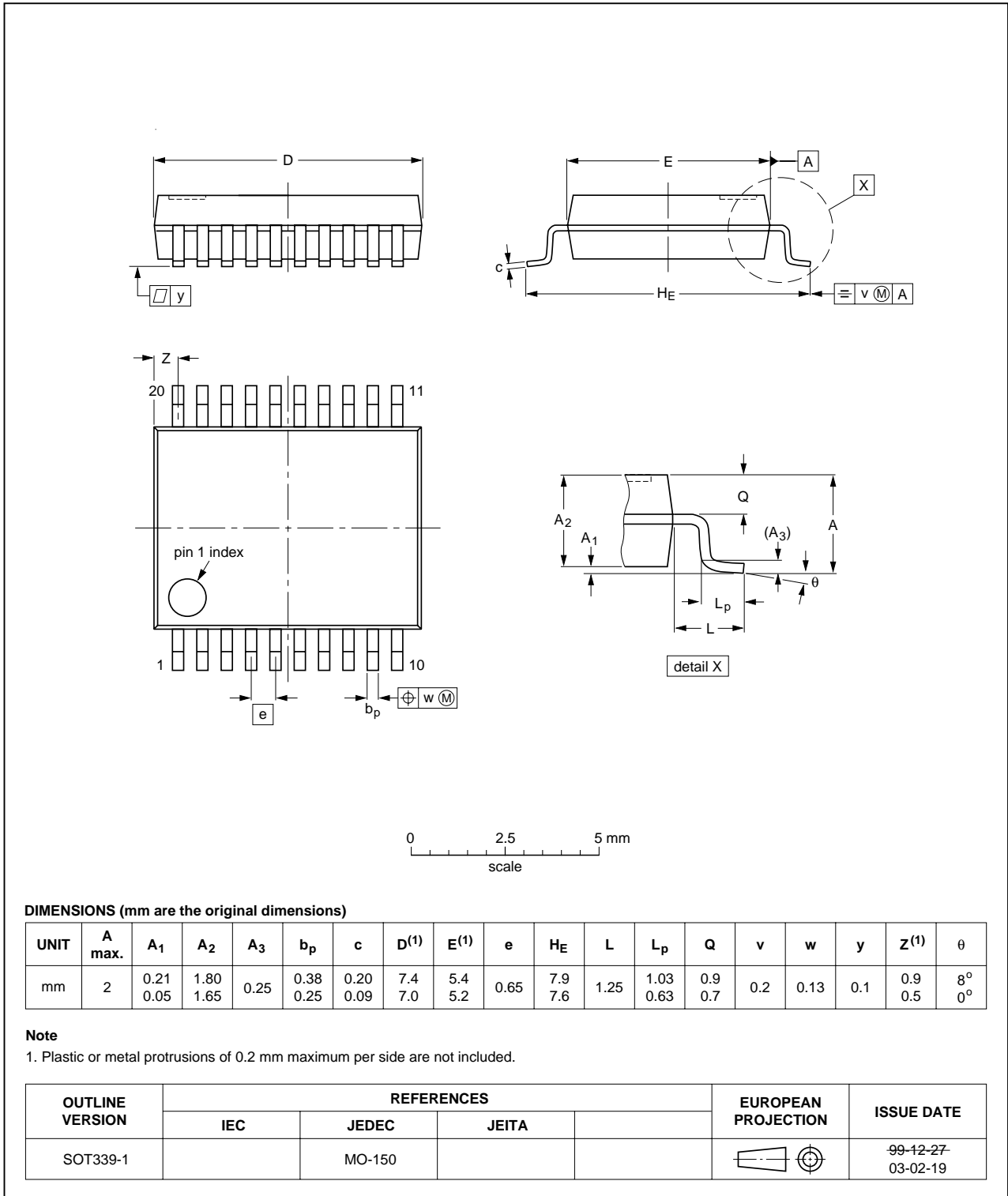


Fig 11. Package outline SOT339-1 (SSOP20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

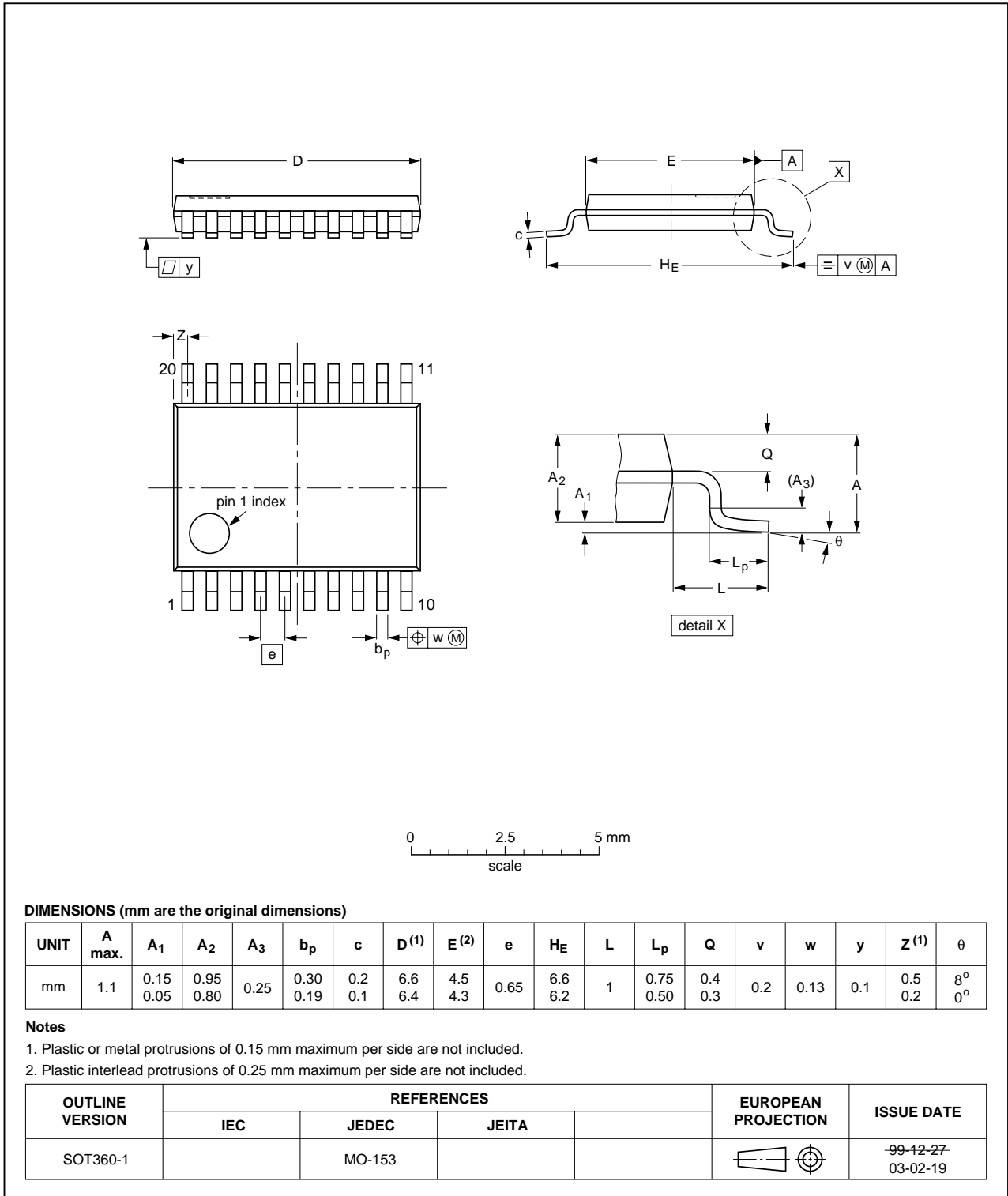


Fig 12. Package outline SOT360-1 (TSSOP20)

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm

SOT764-1

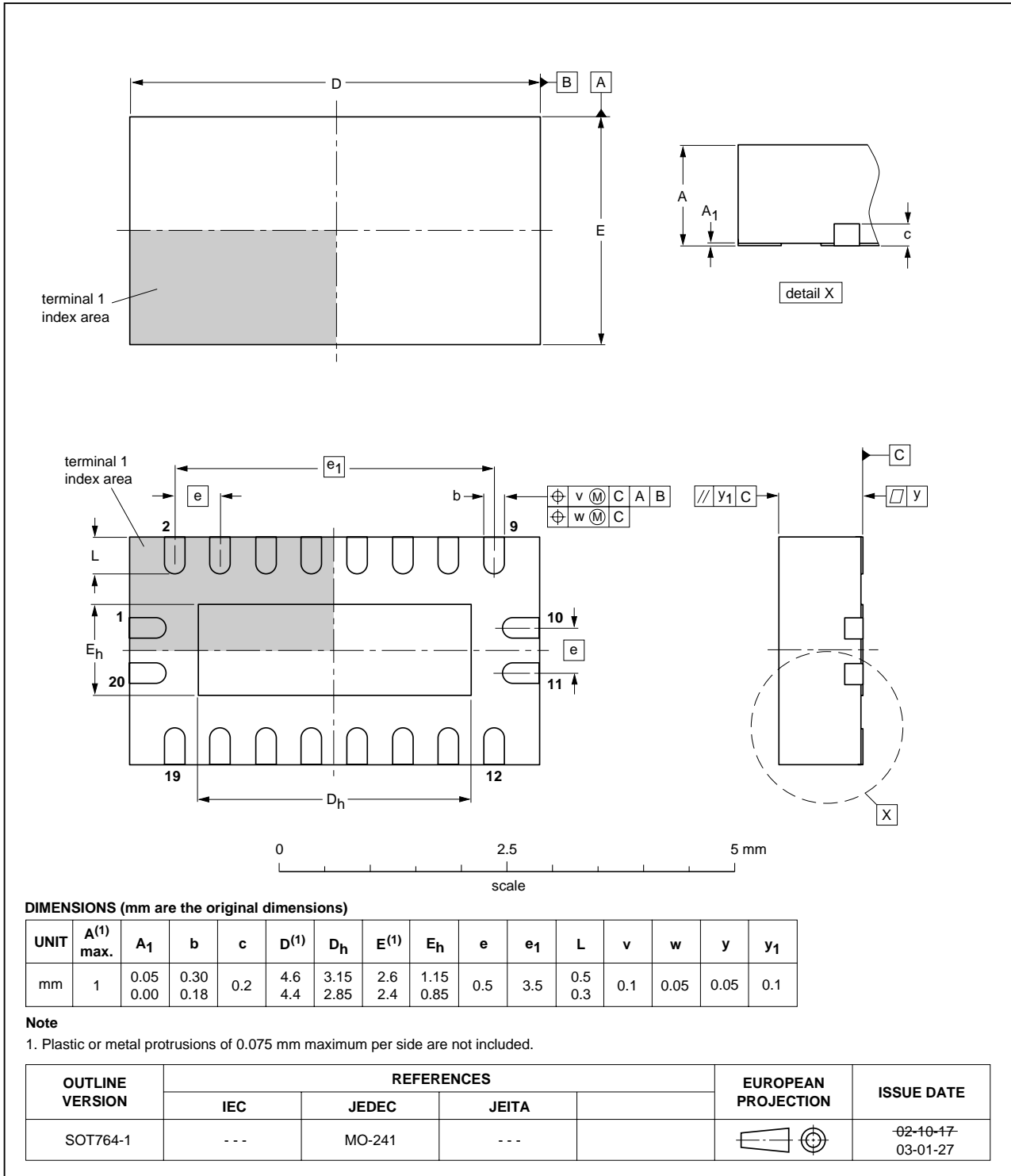


Fig 13. Package outline SOT764-1 (DHVQFN20)

13. Abbreviations

Table 10. Abbreviations

| Acronym | Description |
|---------|--|
| BiCMOS | Integrated Bipolar junction transistors and CMOS |
| CDM | Charged Device Model |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| TTL | Transistor-Transistor Logic |

14. Revision history

Table 11. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|----------------|--|-----------------------|---------------|------------|
| 74LVT273_3 | 20080910 | Product data sheet | - | 74LVT273_2 |
| Modifications: | <ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. Title changed to 3.3 V octal D-type flip-flop Section 3 "Ordering information" and Section 12 "Package outline" DHVQFN20 package added. Table 4 "Limiting values" T_j and P_{tot} values added. | | | |
| 74LVT273_2 | 19980219 | Product specification | - | - |

15. Legal information

16. Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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18. Contents

| | | |
|-----------|---|-----------|
| 1 | General description | 1 |
| 2 | Features | 1 |
| 3 | Ordering information | 2 |
| 4 | Functional diagram | 2 |
| 5 | Pinning information | 4 |
| 5.1 | Pinning | 4 |
| 5.2 | Pin description | 4 |
| 6 | Functional description | 5 |
| 7 | Limiting values | 5 |
| 8 | Recommended operating conditions | 5 |
| 9 | Static characteristics | 6 |
| 10 | Dynamic characteristics | 7 |
| 11 | Waveforms | 8 |
| 12 | Package outline | 11 |
| 13 | Abbreviations | 15 |
| 14 | Revision history | 15 |
| 15 | Legal information | 16 |
| 16 | Data sheet status | 16 |
| 16.1 | Definitions | 16 |
| 16.2 | Disclaimers | 16 |
| 16.3 | Trademarks | 16 |
| 17 | Contact information | 16 |
| 18 | Contents | 17 |

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