CBTL03SB212

DisplayPort Gen2 sideband signal multiplexer

Rev. 1 — 21 February 2011 Product data sheet

1. General description

The CBTL03SB212 is a sideband signal multiplexer for DisplayPort Gen2 applications. It provides one differential channel capable of switching or multiplexing (bidirectional and AC-coupled) DisplayPort 1.2 Fast AUX or AUX signal, using high-bandwidth pass-gate technology. Additionally, it provides for switching/multiplexing of the Hot Plug Detect signal as well as the Display Data Channel (DDC) signals, for a total of three channels.

A typical application of CBTL03SB212 is on motherboards where one of two GPU display sources needs to be selected to connect to a display sink device or connector. A controller chip selects which path to use by setting a select signal HIGH or LOW. Due to the non-directional nature of the signal paths (which use high-bandwidth pass-gate technology), the CBTL03SB212 can also be used in the reverse topology, e.g., to connect one display source device to one of two display sink devices or connectors.

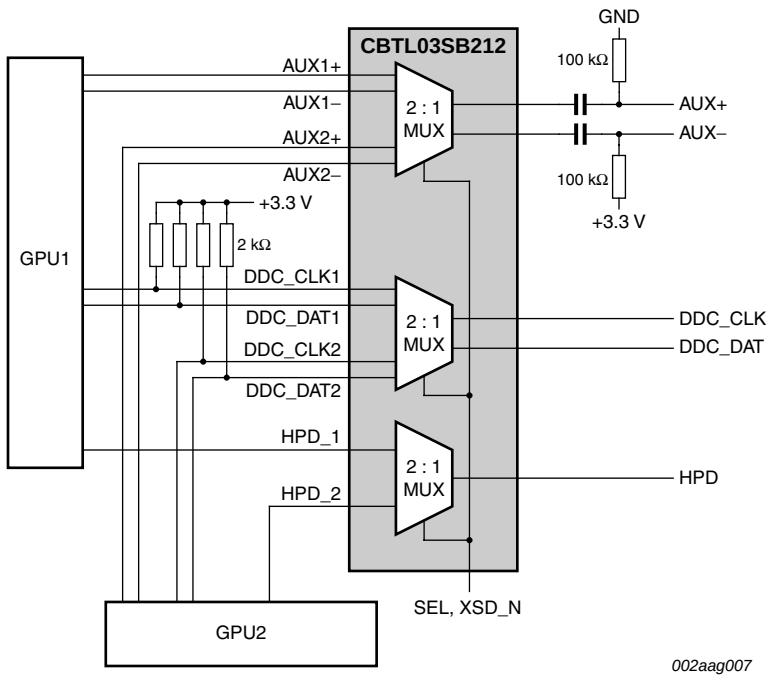


Fig 1. CBTL03SB212 application example

2. Features and benefits

- 1 : 2 multiplexing of DisplayPort signals
  - 1 high-speed differential channel for Fast AUX or AUX
  - 1 channel for DDC clock and data
  - 1 channel for HPD
- High-bandwidth analog pass-gate technology
- Very low intra-pair differential skew (5 ps typical)
- Switch/MUX position select
- Shutdown mode CMOS input
- Shutdown mode minimizes power consumption while switching all channels off
- Very low operation current of 0.2 mA typical
- Very low shutdown current of < 10 μA
- Single 3.3 V power supply
- ESD 4 kV HBM, 1 kV CDM
- Available in 4 mm × 4 mm HVQFN20 package

3. Applications

- Motherboard applications requiring DisplayPort sideband switching/multiplexing
- Docking stations
- Notebook computers

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
CBTL03SB212BS	HVQFN20	plastic thermal enhanced very thin quad flat package; no leads; 20 terminals; body 4 × 4 × 0.85 mm[1]	SOT917-1

[1] Total height after printed-circuit board mounting = 1 mm (maximum).

5. Functional diagram

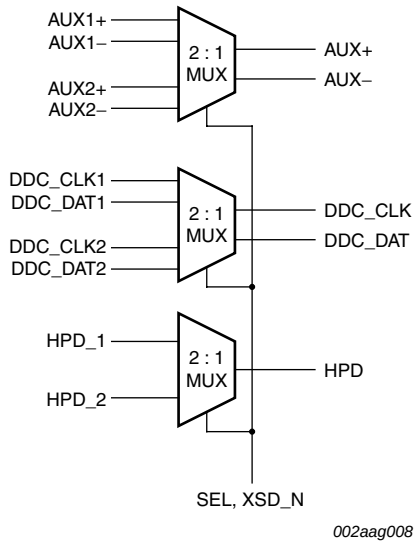


Fig 2. Functional diagram

6. Pinning information

6.1 Pinning

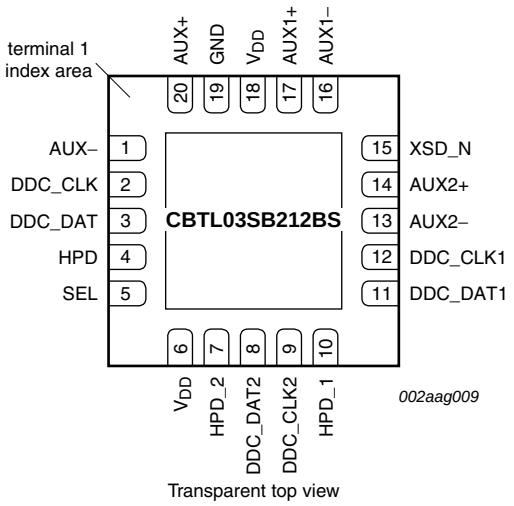


Fig 3. Pin configuration for HVQFN20

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Type	Description
SEL	5	3.3 V CMOS single-ended input	Selects between two multiplexer/switch paths.
XSD_N	15	3.3 V CMOS single-ended input	Shutdown pin. Should be driven HIGH or connected to V_{DD} for normal operation. When LOW, all paths are switched off (non-conducting high-impedance state), and supply current consumption is minimized.
AUX+	20	differential I/O	High-speed differential pair for AUX signals, right-side.
AUX−	1	differential I/O	
DDC_CLK	2	differential I/O	Pair of single-ended terminals for DDC clock and data signals, right-side.
DDC_DAT	3	differential I/O	
HPD	4	single-ended I/O	Single-ended channel for the HPD signal, right-side.
AUX1+	17	differential I/O	High-speed differential pair for AUX signals, path 1, left-side.
AUX1−	16	differential I/O	
AUX2+	14	differential I/O	High-speed differential pair for AUX signals, path 2, left-side.
AUX2−	13	differential I/O	
DDC_CLK1	12	differential I/O	Pair of single-ended terminals for DDC clock and data signals, path 1, left-side.
DDC_DAT1	11	differential I/O	
DDC_CLK2	9	differential I/O	Pair of single-ended terminals for DDC clock and data signals, path 2, left-side.
DDC_DAT2	8	differential I/O	
HPD_1	10	single-ended I/O	Single-ended channel for the HPD signal, path 1, left-side.
HPD_2	7	single-ended I/O	Single-ended channel for the HPD signal, path 2, left-side.
V_{DD}	6, 18	power supply	3.3 V power supply.
GND[1]	19	ground	Ground.

[1] HVQFN20 package die supply ground is connected to both GND pin and exposed center pad. GND pin and the exposed center pad must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias need to be incorporated in the printed-circuit board in the thermal pad region.

7. Functional description

Refer to Figure 2 “Functional diagram”.

The CBTL03SB212 uses 3.3 V power supply. All signal paths are implemented using high-bandwidth pass-gate technology, are bidirectional and no clock or reset signal is needed for the multiplexer to function.

The switch position is selected using the select signal (SEL). The detailed operation is described in Section 7.1.

7.1 MUX select (SEL) function

The internal multiplexer switch position is controlled by the logic inputs SEL as described below.

Table 3. MUX select control

SEL	Path 2	Path 1
0	high-impedance	active
1	active	high-impedance

7.2 Shutdown function

The CBTL03SB212 provides a shutdown function to minimize power consumption when the application is not active but power to the CBTL03SB212 is provided. Pin XSD_N (active LOW) puts all channels in Off mode (non-conducting high-impedance state) while reducing current consumption to near-zero.

Table 4. Shutdown function

XSD_N	State
0	shutdown
1	active

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			−0.3	+5	V
T_{case}	case temperature	for operation within specification		−40	+85	°C
V_{ESD}	electrostatic discharge voltage	HBM	[1]	-	4000	V
		CDM	[2]	-	1000	V

[1] Human Body Model: ANSI/EOS/ESD-S5.1-1994, standard for ESD sensitivity testing, Human Body Model - Component level; Electrostatic Discharge Association, Rome, NY, USA.

[2] Charged-Device Model: ANSI/EOS/ESD-S5.3-1-1999, standard for ESD sensitivity testing, Charged-Device Model - Component level; Electrostatic Discharge Association, Rome, NY, USA.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		3.0	3.3	3.6	V
V_I	input voltage		-	-	3.6	V
T_{amb}	ambient temperature	operating in free air	−40	-	+85	°C

10. Characteristics

10.1 General characteristics

Table 7. General characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	supply current	operating mode (XSD_N = HIGH); V_{DD} = 3.3 V	-	0.2	1	mA
		shutdown mode (XSD_N = LOW); V_{DD} = 3.3 V	-	-	10	μA
P_{tot}	total power dissipation	operating mode (XSD_N = HIGH); V_{DD} = 3.3 V	-	-	5	mW
$t_{startup}$	start-up time	supply voltage valid or XSD_N going HIGH to channel specified operating characteristics	-	-	10	μs
t_{rcfg}	reconfiguration time	SEL state change to channel specified operating characteristics	-	-	1	μs

10.2 AUX channel characteristics

Table 8. AUX channel characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_I	input voltage		–0.3	-	+2.6	V
V_{IC}	common-mode input voltage		0	-	2.0	V
V_{ID}	differential input voltage	peak-to-peak	-	-	+1.4	V
DDIL	differential insertion loss	channel is on; f = 100 MHz	-	–0.8	-	dB
		channel is on; f = 2.5 GHz	-	–3	-	dB
		channel is off; 0 Hz ≤ f ≤ 1.0 GHz	-	-	–30	dB
DDRL	differential return loss	channel is on; 0 Hz ≤ f ≤ 1.0 GHz	-	-	–10	dB
DDNEXT	differential near-end crosstalk	adjacent channels are on; 0 Hz ≤ f ≤ 1.0 GHz	-	-	–40	dB
B	bandwidth	–3.0 dB intercept	-	2.5	-	GHz
t_{PD}	propagation delay	from left-side port to right-side port or vice versa	-	100	-	ps
$t_{sk(dif)}$	differential skew time	intra-pair	-	5	-	ps

10.3 DDC ports

Table 9. DDC port characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_I	input voltage		–0.3	-	V_{DD}	V
t_{PD}	propagation delay	from left-side port to right-side port or vice versa	-	100	-	ps

10.4 HPD input, HPD output

Table 10. HPD input and output characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_I	input voltage		[1]	–0.3	-	3.6	V
t_{PD}	propagation delay	from left-side port to right-side port or vice versa		-	100	-	ps

[1] Low-speed input changes state on cable plug/unplug.

10.5 MUX select input

Table 11. SEL, XSD_N input characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage	SEL, XSD_N	2.0	-	3.6	V
V_{IL}	LOW-level input voltage	SEL, XSD_N	0	-	0.8	V
I_{LI}	input leakage current	measured with input at $V_{IH(max)}$ and $V_{IL(min)}$	-	-	10	μA

11. Test information

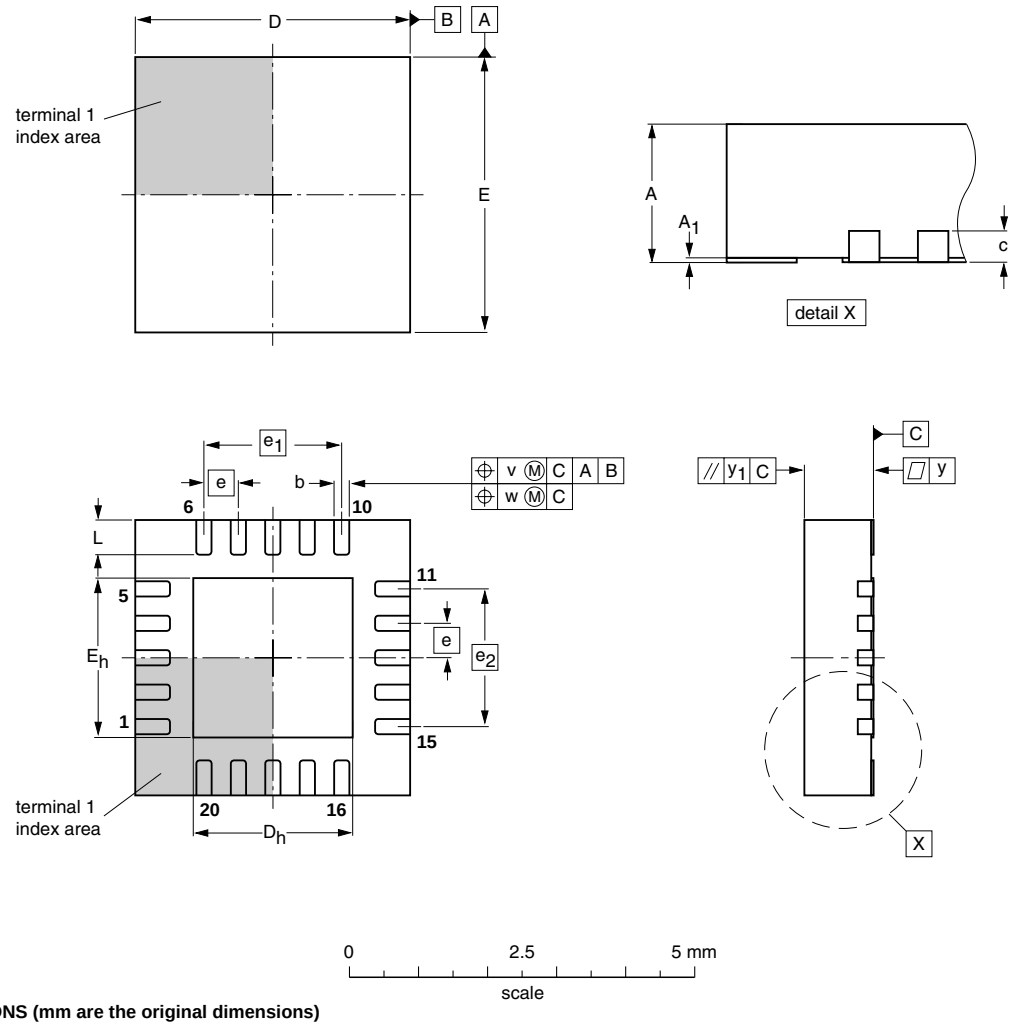
11.1 Switch test fixture requirements

The test fixture for switch S-parameter measurement shall be designed and built to specific requirements, as described below, to ensure good measurement quality and consistency.

- The test fixture shall be a FR4-based PCB of the microstrip structure; the dielectric thickness or stack-up shall be about 4 mils.
- The total thickness of the test fixture PCB shall be 1.57 mm (0.062 in).
- The measurement signals shall be launched into the switch from the top of the test fixture, capturing the through-hole stub effect.
- Traces between the DUT and measurement ports (SMA or microprobe) should be uncoupled from each other, as much as possible. Therefore, the traces should be routed in such a way that traces will diverge from each other exiting from the switch pin field.
- The trace lengths between the DUT and measurement port shall be minimized. The maximum trace length shall not exceed 1000 mils. The trace lengths between the DUT and measurement port shall be equal.
- All of the traces on the test board and add-in card must be held to a characteristic impedance of 50 Ω with a tolerance of ±7 %.
- SMA connector is recommended for ease of use. The SMA launch structure shall be designed to minimize the connection discontinuity from SMA to the trace. The impedance range of the SMA connector seen from a TDR with a 60 ps rise time should be within 50 Ω ± 7 Ω.

12. Package outline

HVQFN20: plastic thermal enhanced very thin quad flat package; no leads; 20 terminals; body 4 x 4 x 0.85 mm **SOT917-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	4.1 3.9	2.45 2.15	4.1 3.9	2.45 2.15	0.5	2	2	0.6 0.4	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT917 -1	- - -	MO-220	- - -			~~05-10-08~~ 05-10-31

Fig 4. Package outline HVQFN20 (SOT917-1)

13. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 5) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 12 and 13

Table 12. SnPb eutectic process (from J-STD-020C)

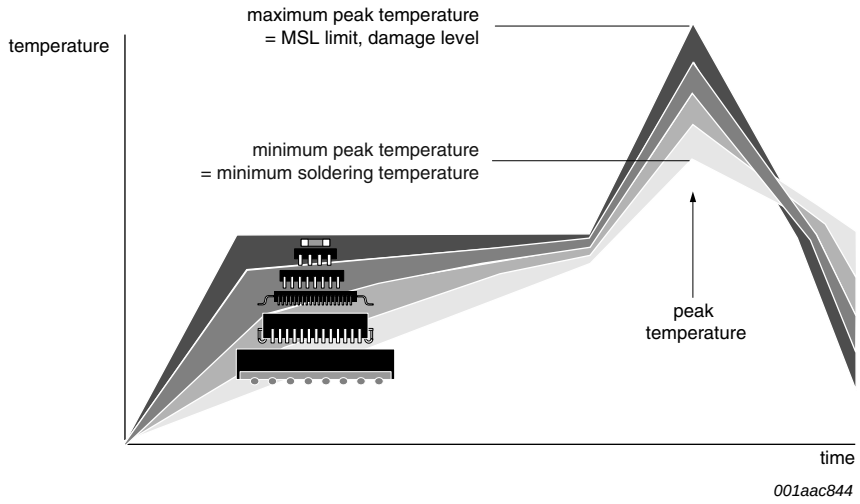
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 13. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 5.



MSL: Moisture Sensitivity Level

Fig 5. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

14. Abbreviations

Table 14. Abbreviations

Acronym	Description
AUX	Auxiliary channel in DisplayPort definition
CDM	Charged-Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DDC	Display Data Channel
DUT	Device Under Test
ESD	ElectroStatic Discharge
FAUX	Fast AUX
GPU	Graphics Processor Unit
HBM	Human Body Model
HPD	Hot Plug Detect
I/O	Input/Output
MUX	Multiplexer
PCB	Printed-Circuit Board
SMA	SubMiniature, version A (connector)
TDR	Time-Domain Reflectometry

15. Revision history

Table 15. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
CBTL03SB212 v.1	20110221	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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[2] The term 'short data sheet' is explained in section "Definitions".

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