



BUK98150-55A

N-channel TrenchMOS logic level FET

19 March 2014

Product data sheet

1. General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

2. Features and benefits

- Low conduction losses due to low on-state resistance
- Q101 compliant
- Suitable for logic level gate drive sources

3. Applications

- 12 V and 24 V loads
- Automotive and general purpose power switching
- Motors, lamps and solenoids

4. Quick reference data

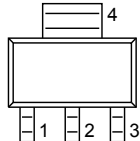
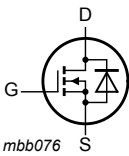
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 150\text{ °C}$	-	-	55	V
I_D	drain current	$V_{GS} = 5\text{ V}; T_{sp} = 25\text{ °C};$ Fig. 2 ; Fig. 3	-	-	5.5	A
P_{tot}	total power dissipation	$T_{sp} = 25\text{ °C};$ Fig. 1	-	-	8	W
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}; I_D = 5\text{ A}; T_j = 25\text{ °C}$	-	-	161	m Ω
		$V_{GS} = 10\text{ V}; I_D = 5\text{ A}; T_j = 25\text{ °C}$	-	116	137	m Ω
		$V_{GS} = 5\text{ V}; I_D = 5\text{ A}; T_j = 25\text{ °C};$ Fig. 12 ; Fig. 13	-	128	150	m Ω
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 5\text{ V}; I_D = 5\text{ A}; V_{DS} = 44\text{ V};$ $T_j = 25\text{ °C};$ Fig. 14	-	2.8	-	nC
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 5.5\text{ A}; V_{sup} \leq 55\text{ V}; R_{GS} = 50\ \Omega;$ $V_{GS} = 5\text{ V}; T_{j(init)} = 25\text{ °C};$ unclamped	-	-	22	mJ



5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>SC-73 (SOT223)</p>	 <p>mbb076</p>
2	D	drain		
3	S	source		
4	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK98150-55A	SC-73	plastic surface-mounted package with increased heatsink; 4 leads	SOT223
BUK98150-55A/CU	SC-73	plastic surface-mounted package with increased heatsink; 4 leads	SOT223

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK98150-55A	915055A
BUK98150-55A/CU	915055

8. Limiting values

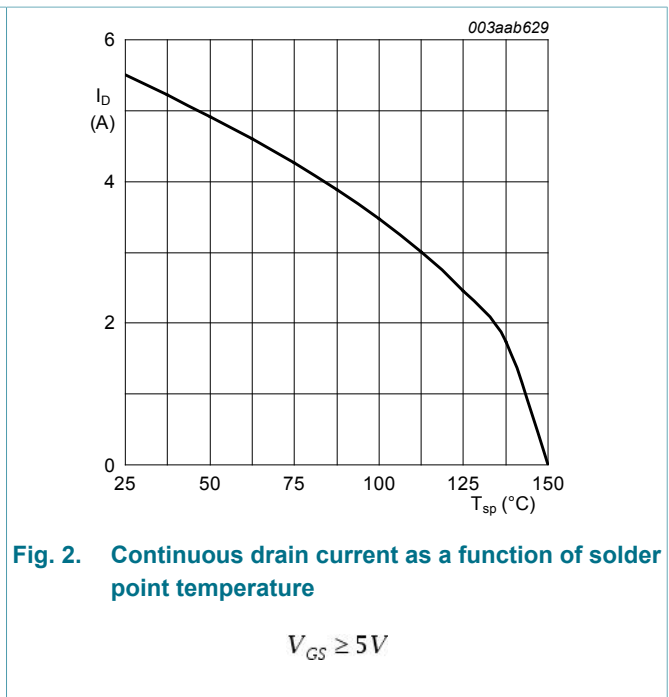
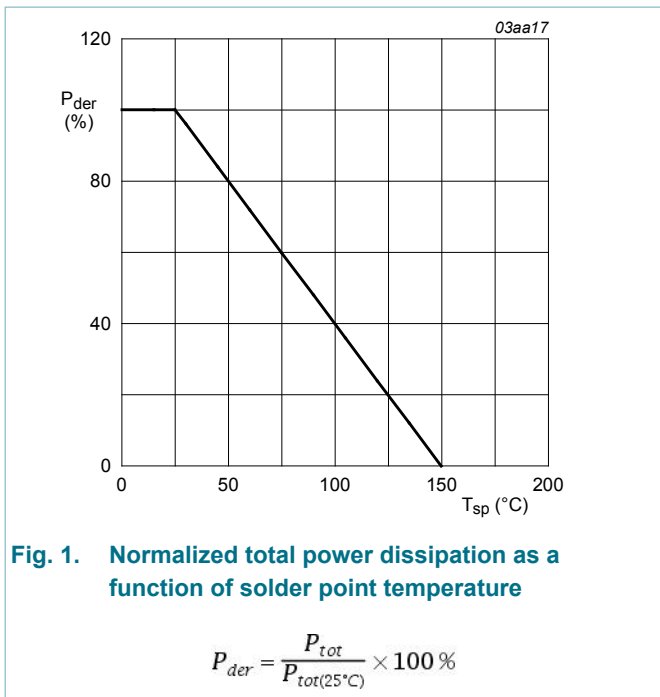
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ }^\circ\text{C}$; $T_j \leq 150\text{ }^\circ\text{C}$	-	55	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	55	V
V_{GS}	gate-source voltage		-15	15	V
P_{tot}	total power dissipation	$T_{sp} = 25\text{ }^\circ\text{C}$; Fig. 1	-	8	W
I_D	drain current	$T_{sp} = 25\text{ }^\circ\text{C}$; $V_{GS} = 5\text{ V}$; Fig. 2 ; Fig. 3	-	5.5	A
		$T_{sp} = 100\text{ }^\circ\text{C}$; $V_{GS} = 5\text{ V}$; Fig. 2	-	3	A
I_{DM}	peak drain current	$T_{sp} = 25\text{ }^\circ\text{C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; Fig. 3	-	22	A

Symbol	Parameter	Conditions	Min	Max	Unit
T _{stg}	storage temperature		-55	150	°C
T _j	junction temperature		-55	150	°C
Source-drain diode					
I _S	source current	T _{sp} = 25 °C	-	5.5	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{sp} = 25 °C	-	22	A
Avalanche ruggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 5.5 A; V _{sup} ≤ 55 V; R _{GS} = 50 Ω; V _{GS} = 5 V; T _{j(init)} = 25 °C; unclamped	-	22	mJ
E _{DS(AL)R}	repetitive drain-source avalanche energy	Fig. 4	[1][2][3][4]	-	J

- [1] Value not quoted. Repetitive rating defined in avalanche rating figure.
- [2] Single-pulse avalanche rating limited by maximum junction temperature of 150 °C.
- [3] Repetitive avalanche rating limited by an average junction temperature of 145 °C.
- [4] Refer to application note AN10273 for further information.



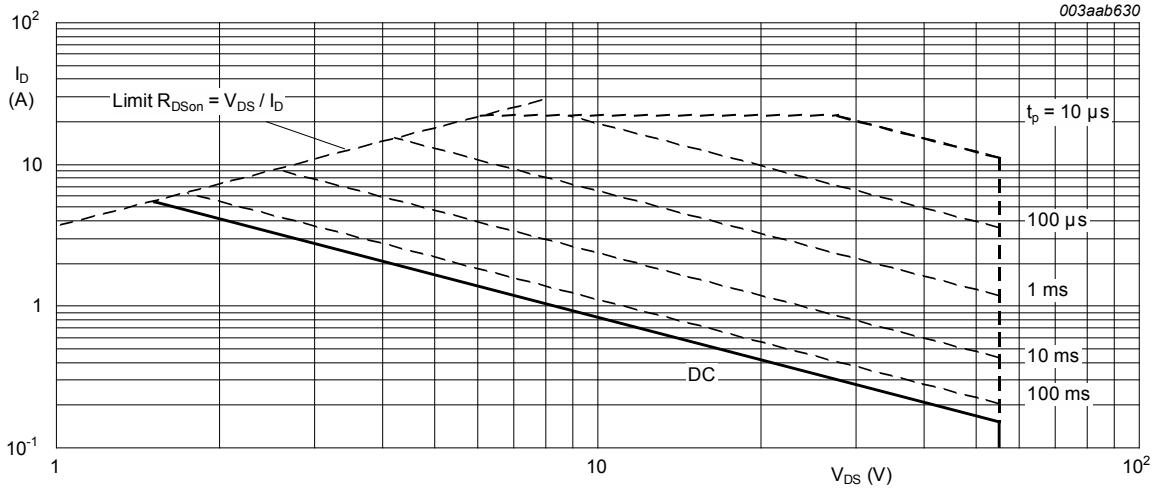


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25\text{ }^\circ\text{C}; I_{DM}$ is single pulse

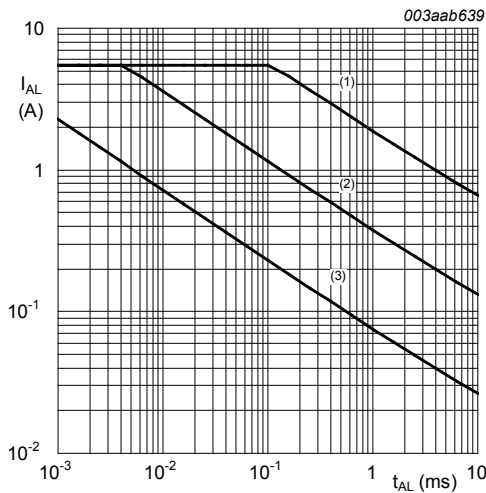


Fig. 4. Single-pulse and repetitive avalanche rating; avalanche current as a function of avalanche time

- (1) Single-pulse; $T_j = 25\text{ }^\circ\text{C}$.
- (2) Single-pulse; $T_j = 125\text{ }^\circ\text{C}$.
- (3) Repetitive.

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	Fig. 5	-	-	15	K/W

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient		-	120	-	K/W

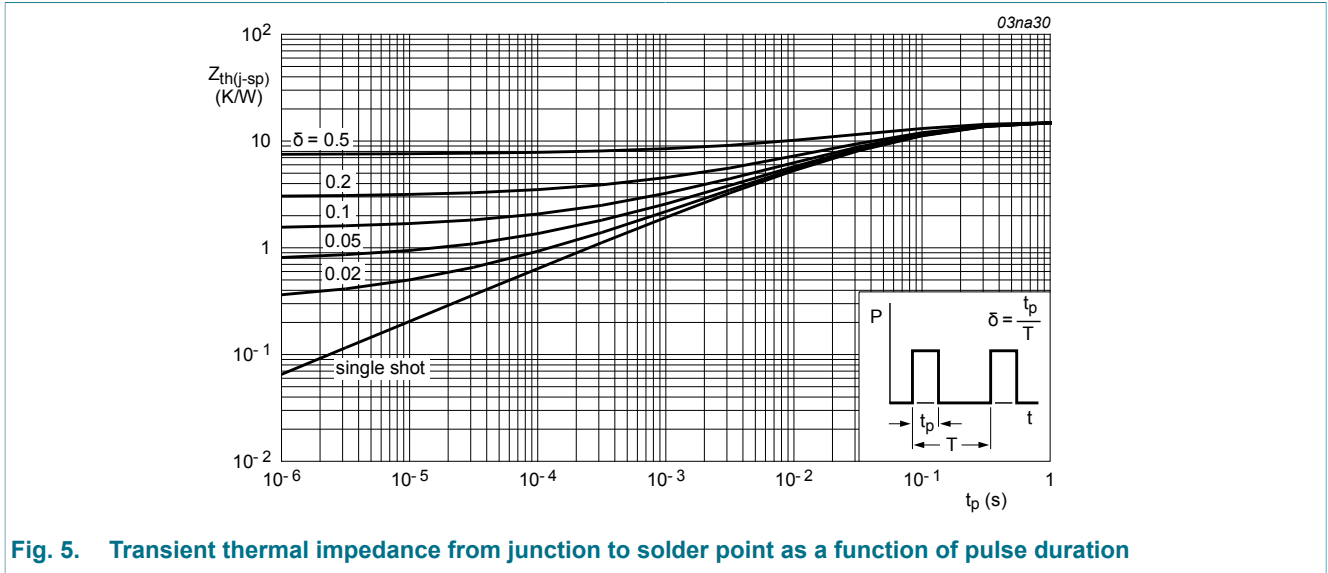


Fig. 5. Transient thermal impedance from junction to solder point as a function of pulse duration

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	50	-	-	V
		$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	55	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ Fig. 11	1	1.5	2	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 150 \text{ }^\circ\text{C};$ Fig. 11	0.6	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ Fig. 11	-	-	2.3	V
I_{DSS}	drain leakage current	$V_{DS} = 55 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.05	10	μA
		$V_{DS} = 55 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 \text{ }^\circ\text{C}$	-	-	500	μA
I_{GSS}	gate leakage current	$V_{GS} = 15 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
		$V_{GS} = -15 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 5 \text{ V}; I_D = 5 \text{ A}; T_j = 150 \text{ }^\circ\text{C};$ Fig. 12; Fig. 13	-	-	276	m Ω
		$V_{GS} = 4.5 \text{ V}; I_D = 5 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	-	161	m Ω
		$V_{GS} = 10 \text{ V}; I_D = 5 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	116	137	m Ω

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		$V_{GS} = 5\text{ V}; I_D = 5\text{ A}; T_j = 25\text{ }^\circ\text{C};$ Fig. 12 ; Fig. 13	-	128	150	m Ω
Dynamic characteristics						
$Q_{G(\text{tot})}$	total gate charge	$I_D = 5\text{ A}; V_{DS} = 44\text{ V}; V_{GS} = 5\text{ V};$ $T_j = 25\text{ }^\circ\text{C};$ Fig. 14	-	5.3	-	nC
Q_{GS}	gate-source charge		-	1	-	nC
Q_{GD}	gate-drain charge		-	2.8	-	nC
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V}; f = 1\text{ MHz};$ $T_j = 25\text{ }^\circ\text{C};$ Fig. 15	-	240	320	pF
C_{oss}	output capacitance		-	53	64	pF
C_{rss}	reverse transfer capacitance		-	40	55	pF
$t_{d(\text{on})}$	turn-on delay time	$V_{DS} = 20\text{ V}; R_L = 3.3\text{ }\Omega; V_{GS} = 5\text{ V};$ $R_{G(\text{ext})} = 10\text{ }\Omega; T_j = 25\text{ }^\circ\text{C}$	-	8	-	ns
t_r	rise time		-	57	-	ns
$t_{d(\text{off})}$	turn-off delay time		-	16	-	ns
t_f	fall time		-	13	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 5\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C};$ Fig. 16	-	0.85	1.2	V
t_{rr}	reverse recovery time	$I_S = 5\text{ A}; dI_S/dt = -100\text{ A}/\mu\text{s};$	-	24	-	ns
Q_r	recovered charge	$V_{GS} = -10\text{ V}; V_{DS} = 30\text{ V}; T_j = 25\text{ }^\circ\text{C}$	-	30	-	nC

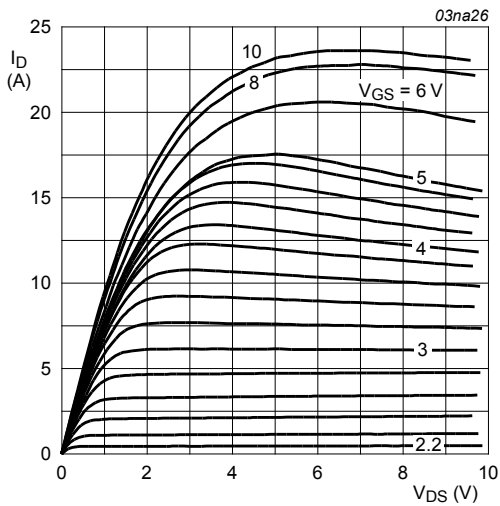


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

$T_j = 25\text{ }^\circ\text{C}; t_p = 300\mu\text{s}$

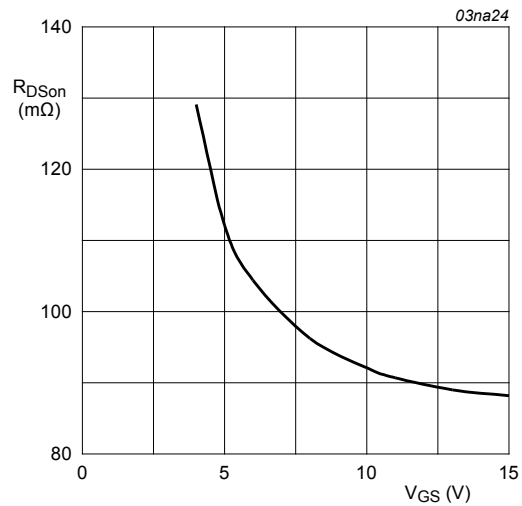


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25\text{ }^\circ\text{C}; I_D = 5\text{ A}$

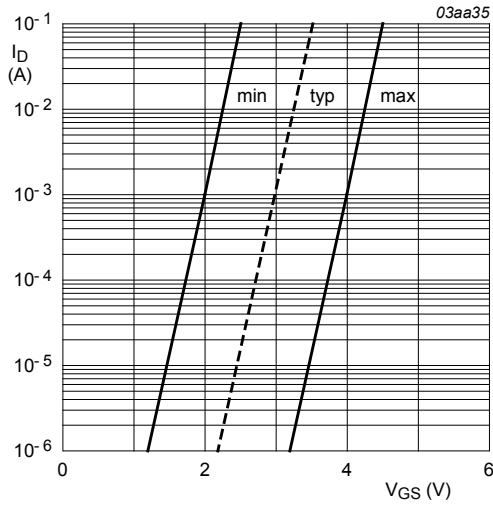


Fig. 8. Sub-threshold drain current as a function of gate-source voltage

$$T_j = 25^\circ\text{C}; V_{DS} = 5\text{V}$$

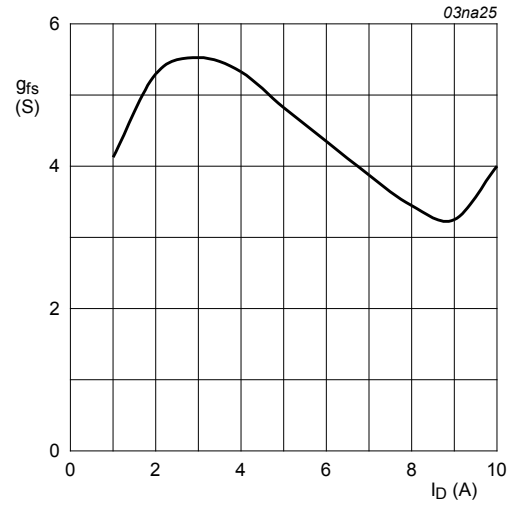


Fig. 9. Forward transconductance as a function of drain current; typical values

$$T_j = 25^\circ\text{C}; V_{DS} = 25\text{V}$$

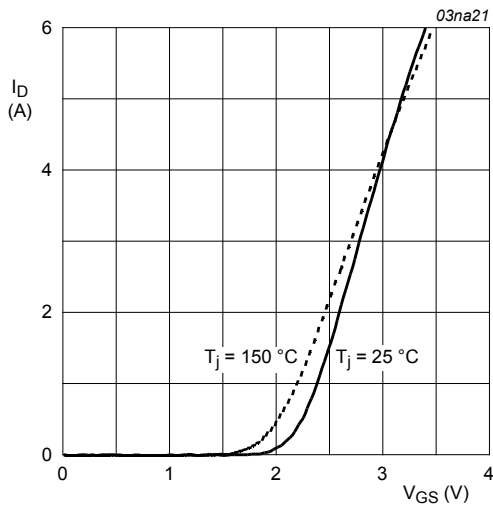


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

$$V_{DS} = 25\text{V}$$

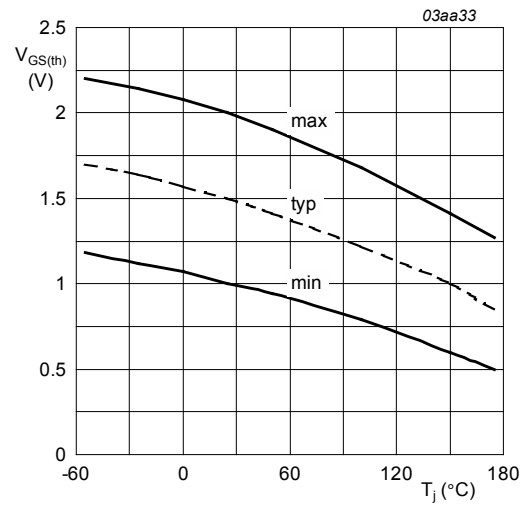


Fig. 11. Gate-source threshold voltage as a function of junction temperature

$$I_D = 1\text{mA}; V_{DS} = V_{GS}$$

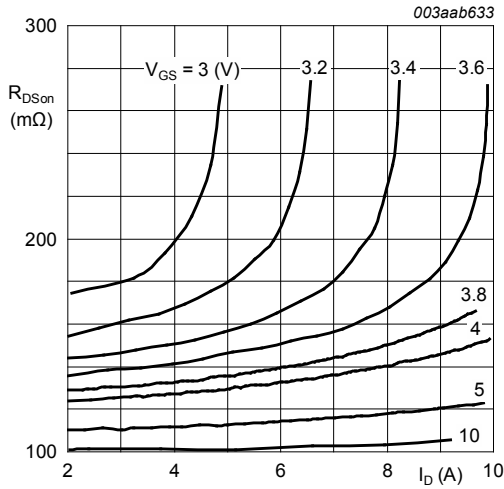


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

$T_j = 25^\circ\text{C}$

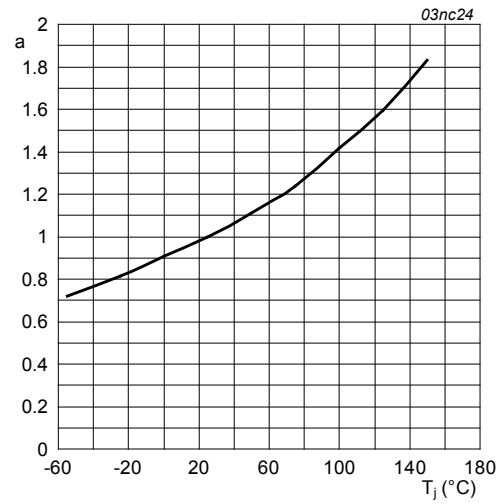


Fig. 13. Normalized drain source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

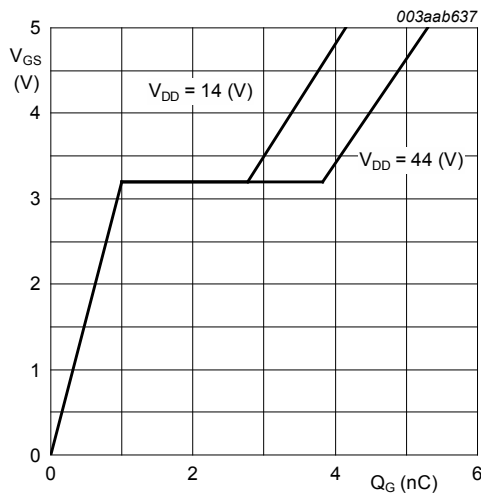


Fig. 14. Gate-source voltage as a function of gate charge; typical values

$T_j = 25^\circ\text{C}; I_D = 5\text{A}$

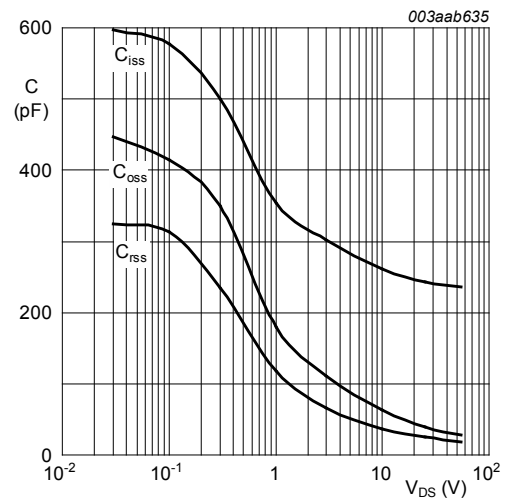


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS} = 0\text{V}; f = 1\text{MHz}$

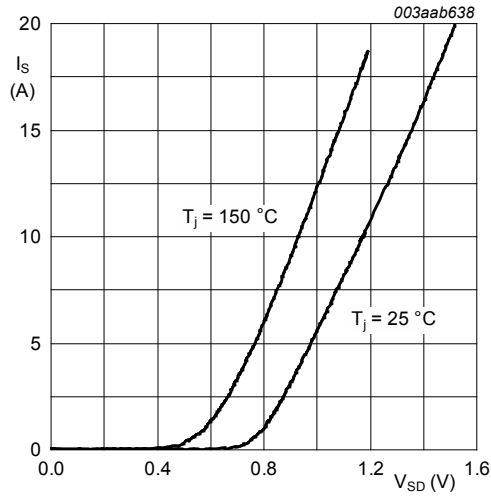


Fig. 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

$$V_{GS} = 0V$$

11. Package outline

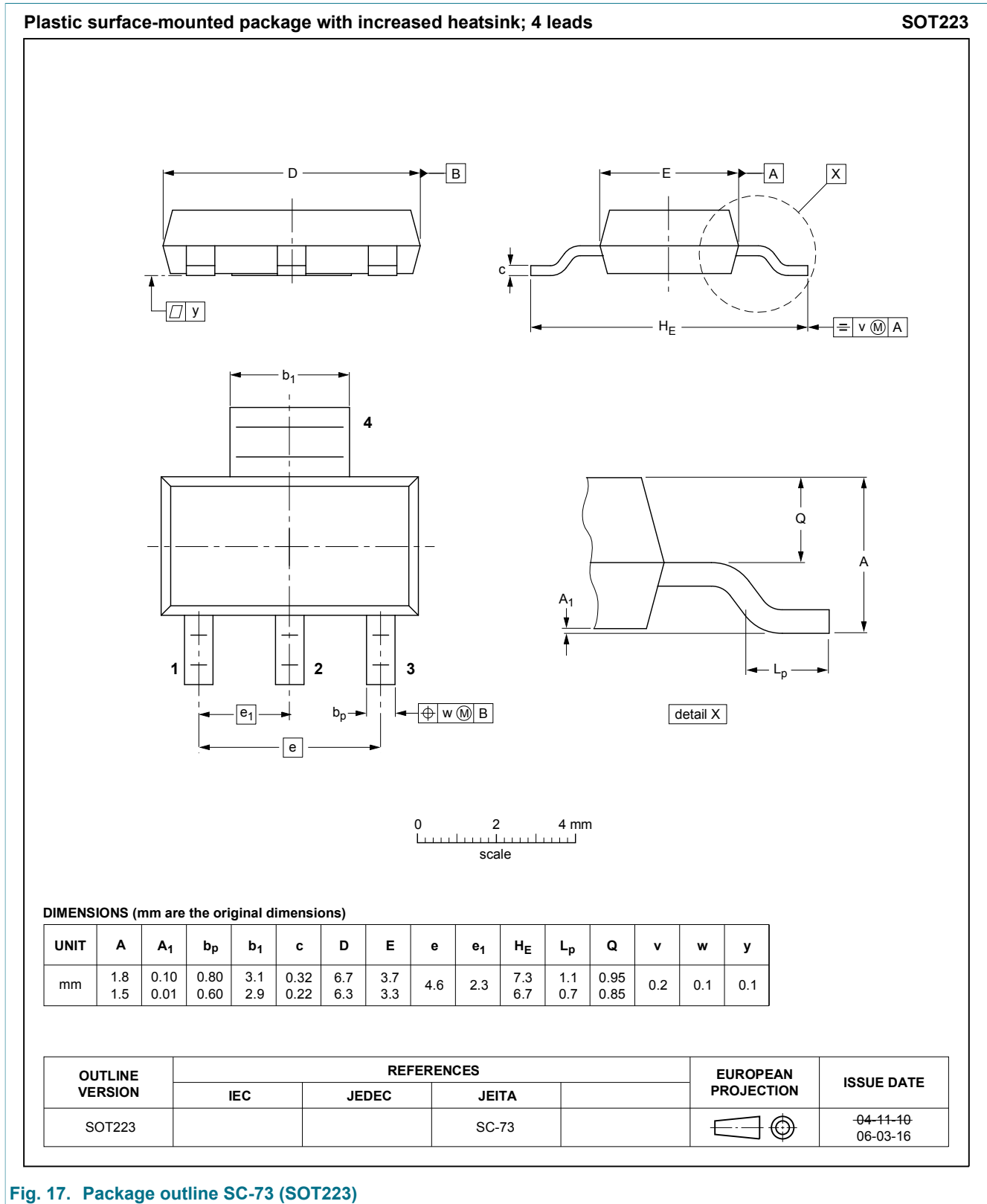


Fig. 17. Package outline SC-73 (SOT223)

12. Legal information

12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
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Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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