

# 74HC238; 74HCT238

3-to-8 line decoder/demultiplexer

Rev. 03 — 16 July 2007

Product data sheet

## 1. General description

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74HC238 and 74HCT238 are high-speed Si-gate CMOS devices and are pin compatible with Low-Power Schottky TTL (LSTTL).

The 74HC238/74HCT238 decoders accept three binary weighted address inputs (A0, A1, A2) and when enabled, provide 8 mutually exclusive active HIGH outputs (Y0 to Y7). The 74HC238/74HCT238 features three enable inputs: two active LOW ( $\bar{E}1$  and  $\bar{E}2$ ) and one active HIGH (E3). Every output will be LOW unless  $\bar{E}1$  and  $\bar{E}2$  are LOW and E3 is HIGH. This multiple enable function allows easy parallel expansion of the "238" to a 1-to-32 (5 lines to 32 lines) decoder with just four "238" ICs and one inverter. The "238" can be used as an eight output demultiplexer by using one of the active LOW enable inputs as the data input and the remaining enable inputs as strobes. Unused enable inputs must be permanently tied to their appropriate active HIGH or LOW state.

The 74HC238/74HCT238 is similar to the 74HC138/74HCT138 but has non-inverting outputs.

## 2. Features

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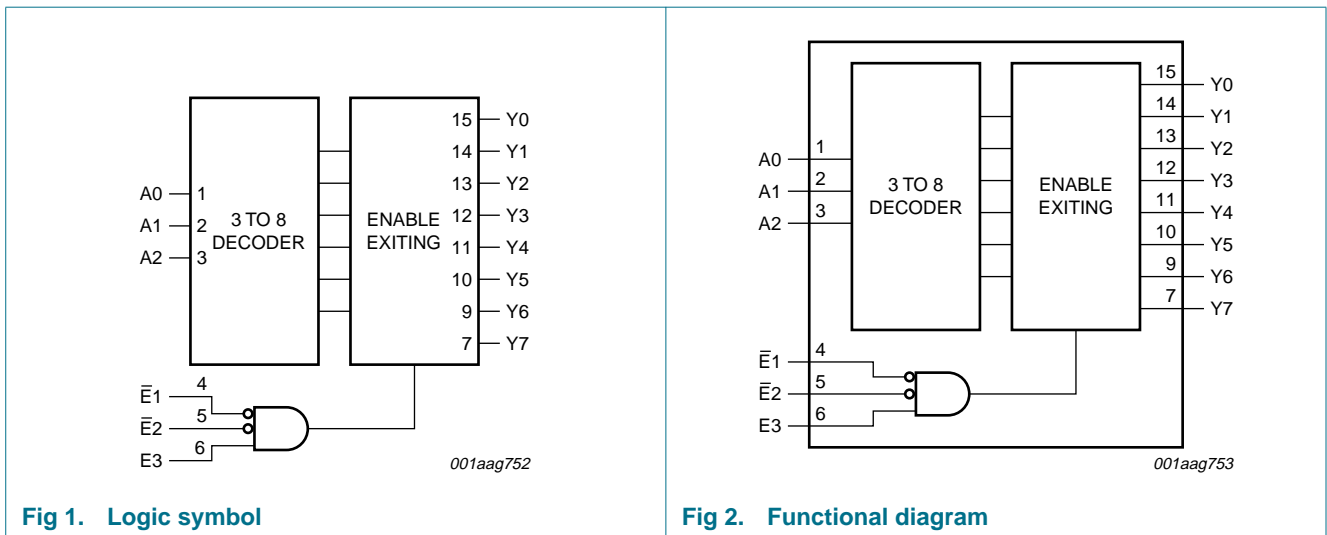
- Demultiplexing capability
- Multiple input enable for easy expansion
- Ideal for memory chip select decoding
- Active HIGH mutually exclusive outputs
- Multiple package options
- Complies with JEDEC standard no. 7A
- ESD protection:
  - ◆ HBM JESD22-A114E exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V
- Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$  and from  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$

### 3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC238N	-40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
74HC238D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC238DB	-40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HC238PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HC238BQ	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1
74HCT238N	-40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
74HCT238D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT238DB	-40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HCT238PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HCT238BQ	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

### 4. Functional diagram



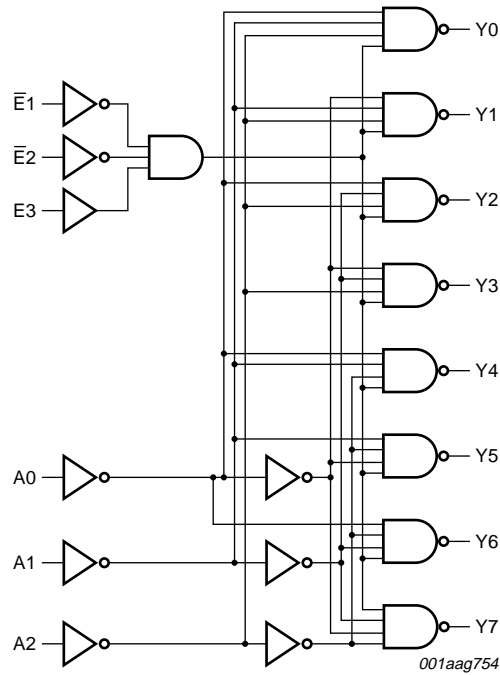


Fig 3. Logic diagram

## 5. Pinning information

### 5.1 Pinning

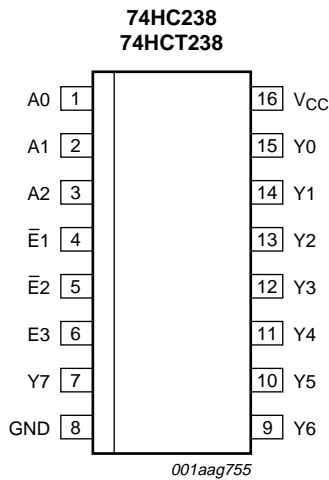
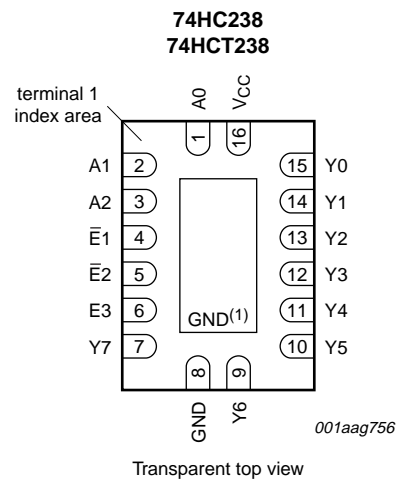


Fig 4. Pin configuration DIP16, SO16, (T)SSOP16



- (1) The die substrate is attached to this pad using conductive die attach material. It can not be used as supply pin or input

Fig 5. Pin configuration DHVQFN16

## 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
A[0:2]	1, 2, 3	address input
$\bar{E}1$	4	enable input (active LOW)
$\bar{E}2$	5	enable input (active LOW)
E3	6	enable input (active HIGH)
Y[0:7]	15, 14, 13, 12, 11, 10, 9, 7	output (active HIGH)
GND	8	ground (0 V)
V <sub>CC</sub>	16	supply voltage

## 6. Functional description

Table 3. Function table<sup>[1]</sup>

Inputs						Outputs							
$\bar{E}1$	$\bar{E}2$	E3	A0	A1	A2	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
H	X	X	X	X	X	L	L	L	L	L	L	L	L
X	H	X	X	X	X	L	L	L	L	L	L	L	L
X	X	L	X	X	X	L	L	L	L	L	L	L	L
L	L	H	L	L	L	H	L	L	L	L	L	L	L
L	L	H	H	L	L	L	H	L	L	L	L	L	L
L	L	H	L	H	L	L	L	H	L	L	L	L	L
L	L	H	H	H	L	L	L	L	H	L	L	L	L
L	L	H	L	L	H	L	L	L	L	H	L	L	L
L	L	H	H	L	H	L	L	L	L	L	H	L	L
L	L	H	L	H	H	L	L	L	L	L	L	H	L
L	L	H	H	H	H	L	L	L	L	L	L	L	H

[1] H = HIGH voltage level;  
 L = LOW voltage level;  
 X = don't care.

## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+7	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < -0.5 V or V <sub>I</sub> > V <sub>CC</sub> + 0.5 V	[1] -	±20	mA
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < -0.5 V or V <sub>O</sub> > V <sub>CC</sub> + 0.5 V	[1] -	±20	mA
I <sub>O</sub>	output current	-0.5 V < V <sub>O</sub> < V <sub>CC</sub> + 0.5 V	-	±25	mA
I <sub>CC</sub>	supply current		-	50	mA
I <sub>GND</sub>	ground current		-50	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	DIP16 package	[2] -	750	mW
		SO16, SSOP16, TSSOP16 and DHVQFN16 packages	[3] -	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For DIP16 packages: above 70 °C the value of P<sub>tot</sub> derates linearly at 12 mW/K.

[3] For SO16 packages: above 70 °C the value of P<sub>tot</sub> derates linearly at 8 mW/K.

For SSOP16 and TSSOP16 packages: above 60 °C the value of P<sub>tot</sub> derates linearly at 5.5 mW/K.

For DHVQFN16 packages: above 60 °C the value of P<sub>tot</sub> derates linearly at 4.5 mW/K.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74HC238			74HCT238			Unit
			Min	Typ	Max	Min	Typ	Max	
V <sub>CC</sub>	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V <sub>I</sub>	input voltage		0	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V
V <sub>O</sub>	output voltage		0	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V
T <sub>amb</sub>	ambient temperature		-40	-	+125	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 2.0 V	-	-	625	-	-	-	ns/V
		V <sub>CC</sub> = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V <sub>CC</sub> = 6.0 V	-	-	83	-	-	-	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74HC238</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V <sub>CC</sub> = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V <sub>CC</sub> = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V <sub>CC</sub> = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V <sub>CC</sub> = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I <sub>O</sub> = -4.0 mA; V <sub>CC</sub> = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	μA
		I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 6.0 V	-	-	8.0	-	80	-
C <sub>I</sub>	input capacitance		-	3.5	-	-	-	-	-	pF
<b>74HCT238</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = -20 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -4.0 mA	3.98	4.32	-	3.84	-	3.7	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = 20 μA	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA	-	0.16	0.26	-	0.33	-	0.4	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5 V	-	-	±0.1	-	±1.0	-	±1.0	μA

**Table 6. Static characteristics ...continued**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
$I_{CC}$	supply current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5$ V; $I_O = 0$ A	-	-	8.0	-	80	-	160	$\mu$ A
$\Delta I_{CC}$	additional supply current	per input pin; $V_I = V_{CC} - 2.1$ V; other inputs at $V_{CC}$ or GND; $V_{CC} = 4.5$ V to 5.5 V; $I_O = 0$ A								
		An inputs	-	70	252	-	315	-	343	$\mu$ A
		$\bar{E}1, \bar{E}2$ inputs	-	40	144	-	180	-	196	$\mu$ A
		E3 input	-	145	522	-	653	-	711	$\mu$ A
$C_I$	input capacitance		-	3.5	-	-	-	-	-	pF

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

$GND = 0$  V; test circuit see [Figure 8](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Max (85 °C)	Max (125 °C)	

### 74HC238

$t_{pd}$	propagation delay	An to $Y_n$ ; see <a href="#">Figure 6</a>	[1]						
		$V_{CC} = 2.0$ V	-	47	150	190	225	ns	
		$V_{CC} = 4.5$ V	-	17	30	38	45	ns	
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	14	-	-	-	ns	
		$V_{CC} = 6.0$ V	-	14	26	33	38	ns	
		E3 to $Y_n$ ; see <a href="#">Figure 6</a>	[1]						
		$V_{CC} = 2.0$ V	-	52	160	200	240	ns	
		$V_{CC} = 4.5$ V	-	19	32	40	48	ns	
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	16	-	-	-	ns	
		$V_{CC} = 6.0$ V	-	15	27	34	41	ns	
		$\bar{E}_n$ to $Y_n$ or see <a href="#">Figure 7</a>	[1]						
		$V_{CC} = 2.0$ V	-	50	155	195	235	ns	
		$V_{CC} = 4.5$ V	-	18	31	39	47	ns	
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	17	-	-	-	ns	
$V_{CC} = 6.0$ V	-	14	26	33	40	ns			
$t_t$	transition time	see <a href="#">Figure 6</a> and <a href="#">Figure 7</a>	[2]						
		$V_{CC} = 2.0$ V	-	19	75	95	110	ns	
		$V_{CC} = 4.5$ V	-	7	15	19	22	ns	
		$V_{CC} = 6.0$ V	-	6	13	16	19	ns	
$C_{PD}$	power dissipation capacitance	per package; $V_I = GND$ to $V_{CC}$	[3]	-	72	-	-	-	pF

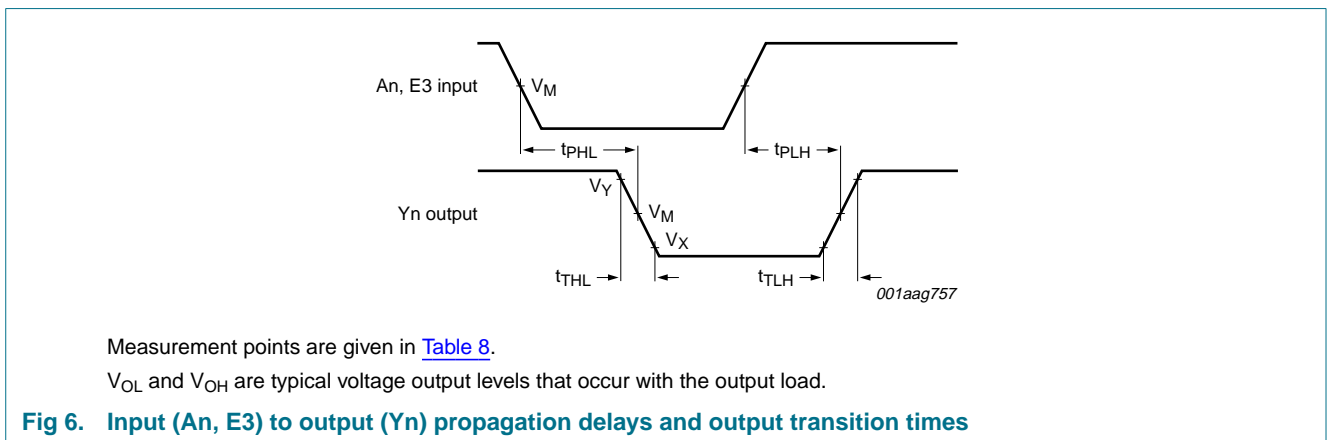
**Table 7. Dynamic characteristics**

$GND = 0\text{ V}$ ; test circuit see [Figure 8](#).

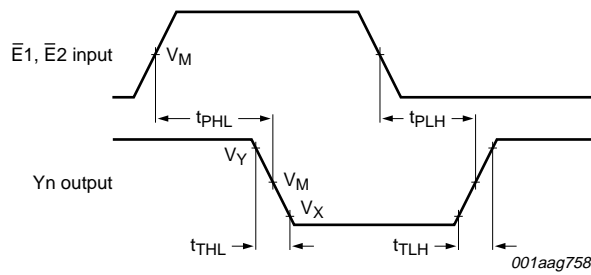
Symbol	Parameter	Conditions	25 °C			-40 °C to +125 °C		Unit	
			Min	Typ	Max	Max (85 °C)	Max (125 °C)		
<b>74HCT238</b>									
$t_{pd}$	propagation delay	An to $Y_n$ ; see <a href="#">Figure 6</a>	[1]						
		$V_{CC} = 4.5\text{ V}$	-	19	35	44	53	ns	
		$V_{CC} = 5.0\text{ V}$ ; $C_L = 15\text{ pF}$	-	18	-	-	-	ns	
		E3 to $Y_n$ ; see <a href="#">Figure 6</a>	[1]						
		$V_{CC} = 4.5\text{ V}$	-	20	37	46	56	ns	
		$V_{CC} = 5.0\text{ V}$ ; $C_L = 15\text{ pF}$	-	20	-	-	-	ns	
$t_t$	transition time	$\bar{E}_n$ to $Y_n$ or see <a href="#">Figure 7</a>	[1]						
		$V_{CC} = 4.5\text{ V}$	-	20	35	44	53	ns	
		$V_{CC} = 5.0\text{ V}$ ; $C_L = 15\text{ pF}$	-	21	-	-	-	ns	
$t_t$	transition time	$V_{CC} = 4.5\text{ V}$ ; see <a href="#">Figure 6</a> and <a href="#">Figure 7</a>	[2]	-	7	15	19	22	ns
$C_{PD}$	power dissipation capacitance	per package; $V_I = GND$ to $V_{CC} - 1.5\text{ V}$	[3]	-	76	-	-	-	pF

- [1]  $t_{pd}$  is the same as  $t_{PHL}$  and  $t_{PLH}$ .
- [2]  $t_t$  is the same as  $t_{THL}$  and  $t_{TLH}$ .
- [3]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$  where:  
 $f_i$  = input frequency in MHz;  
 $f_o$  = output frequency in MHz;  
 $C_L$  = output load capacitance in pF;  
 $V_{CC}$  = supply voltage in V;  
 $N$  = number of inputs switching;  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

## 11. Waveforms







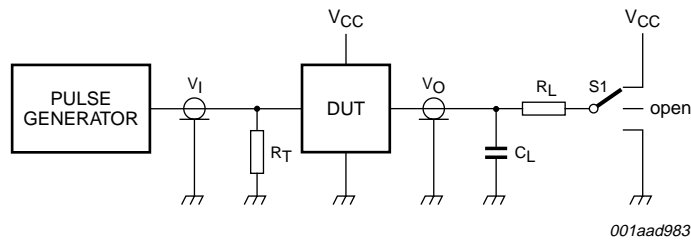
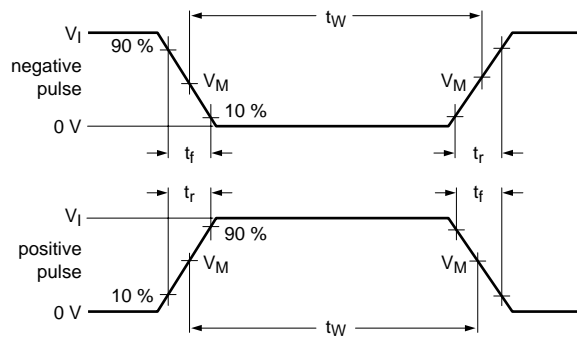
Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig 7. Input ( $\bar{E}1, \bar{E}2$ ) to output ( $Yn$ ) propagation delays and output transition times**

**Table 8. Measurement points**

Type	Input	Output		
	$V_M$	$V_M$	$V_X$	$V_Y$
74HC238	$0.5V_{CC}$	$0.5V_{CC}$	$0.1V_{CC}$	$0.9V_{CC}$
74HCT238	1.3 V	1.3 V	$0.1V_{CC}$	$0.9V_{CC}$



001aad983

Test data is given in [Table 9](#).

Definitions for test circuit:

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_L$  = Load resistance.

S1 = Test selection switch

**Fig 8. Load circuit for measuring switching times**

**Table 9. Test data**

Type	Input		Load		S1 position
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHL}, t_{PLH}$
74HC238	$V_{CC}$	6 ns	15 pF, 50 pF	1 k $\Omega$	open
74HCT238	3 V	6 ns	15 pF, 50 pF	1 k $\Omega$	open

12. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4

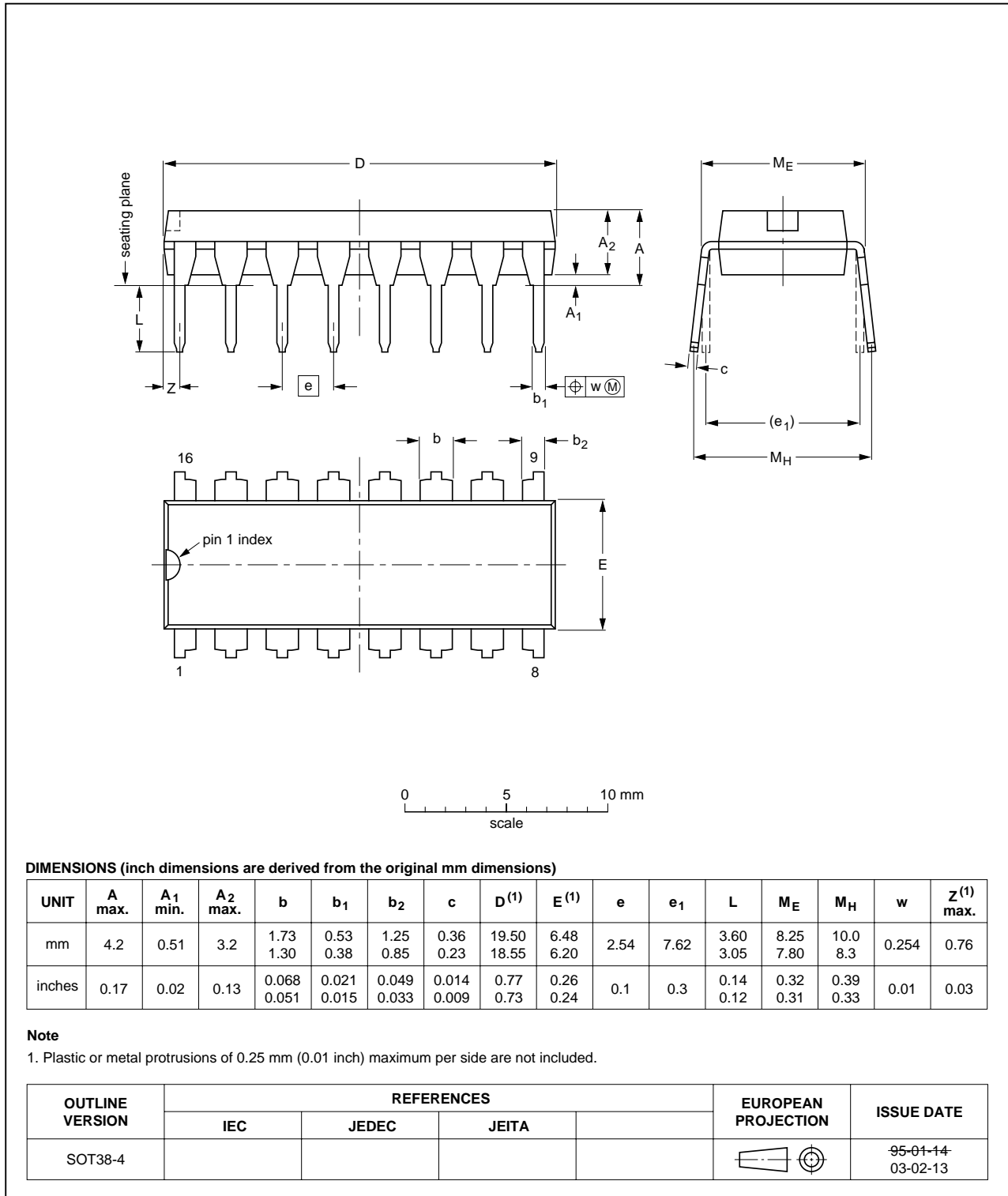


Fig 9. Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

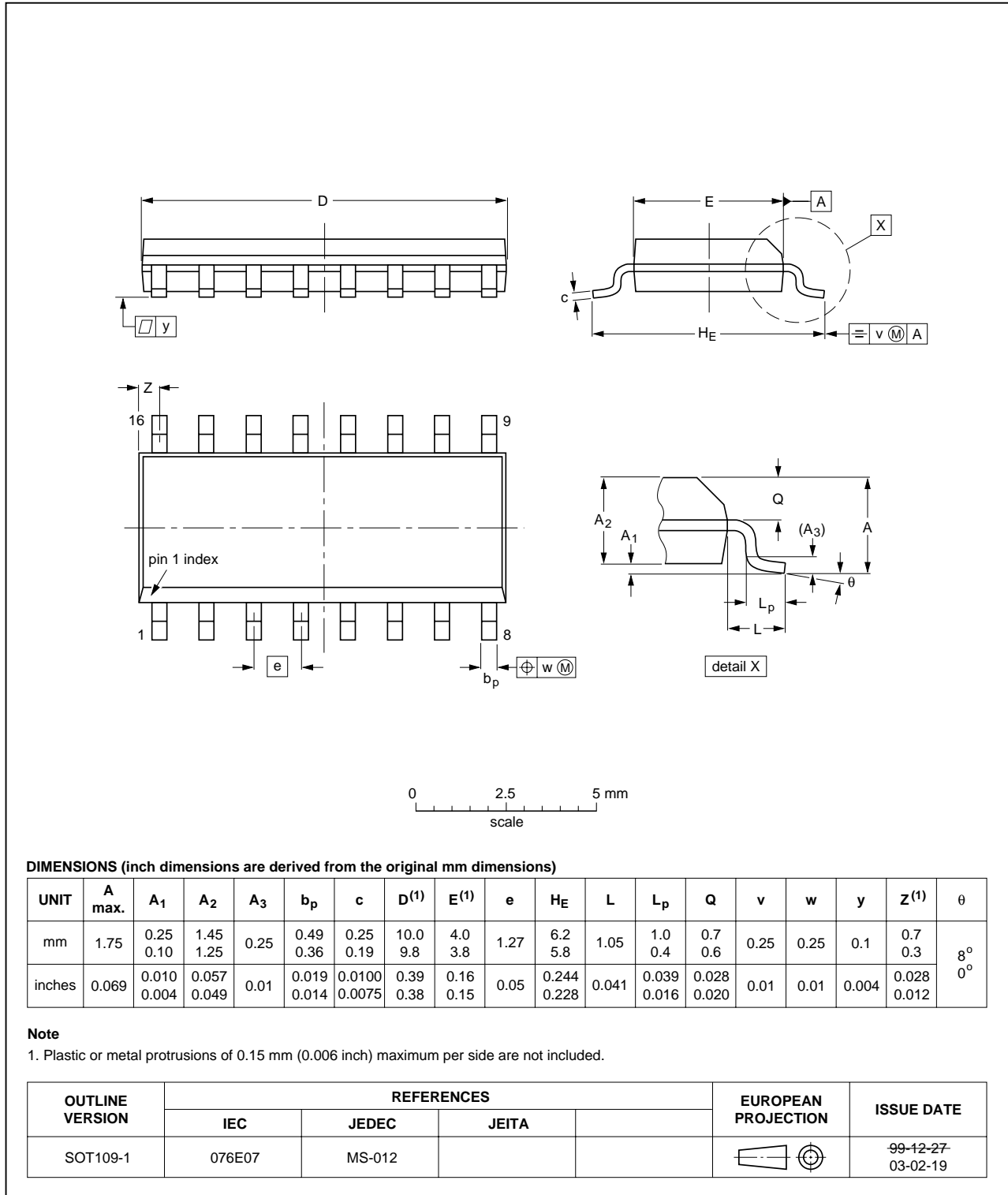


Fig 10. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

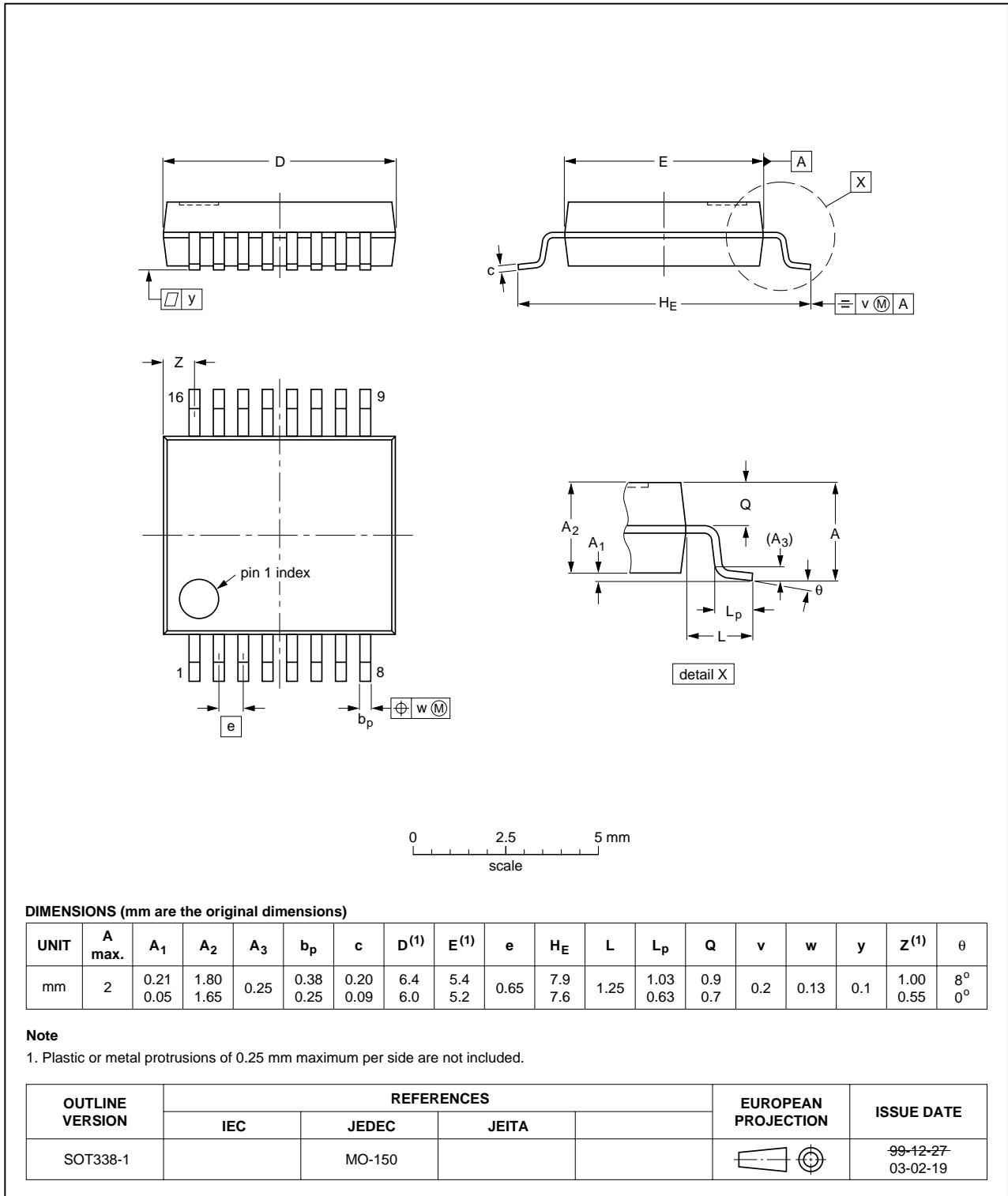


Fig 11. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

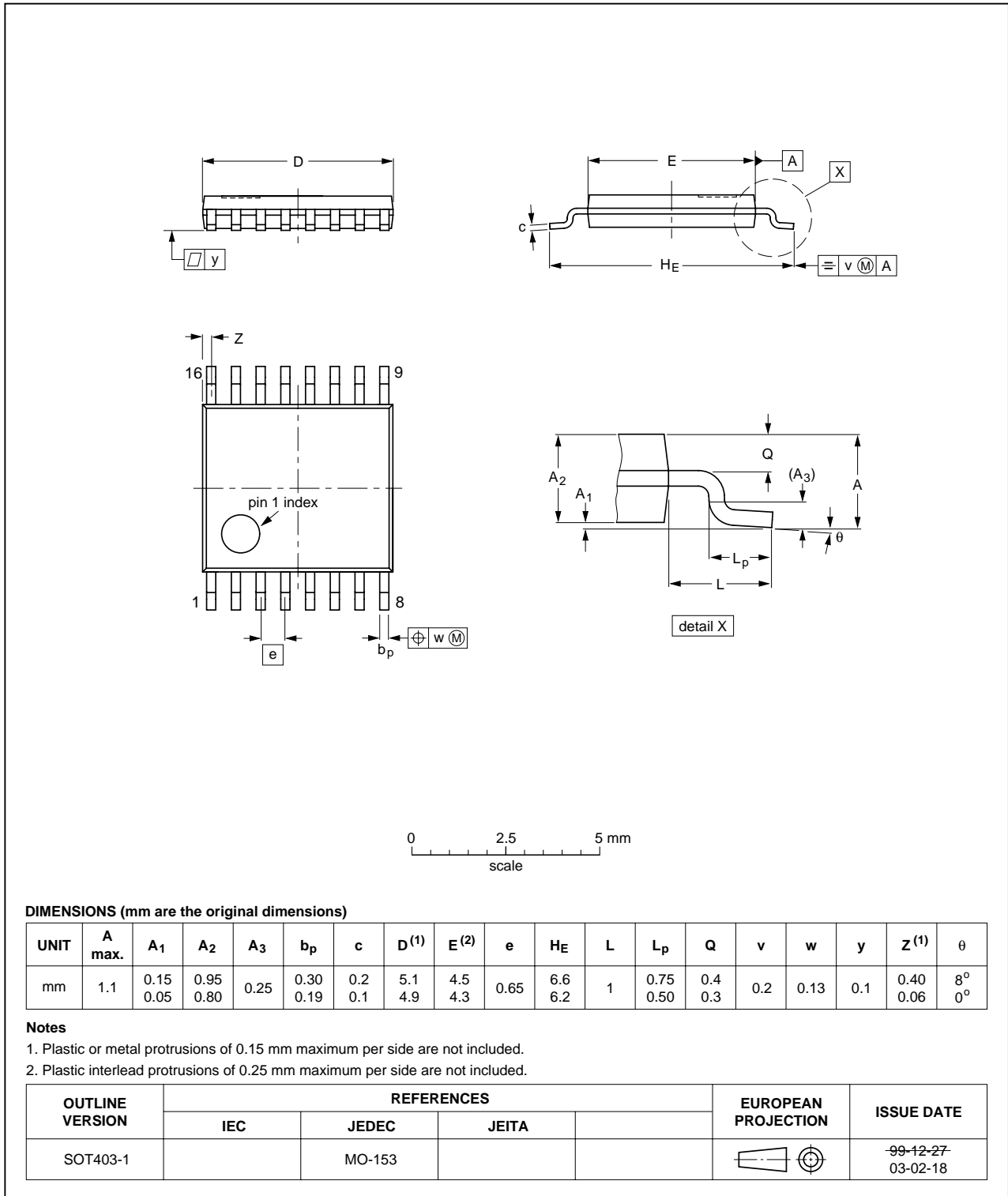


Fig 12. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

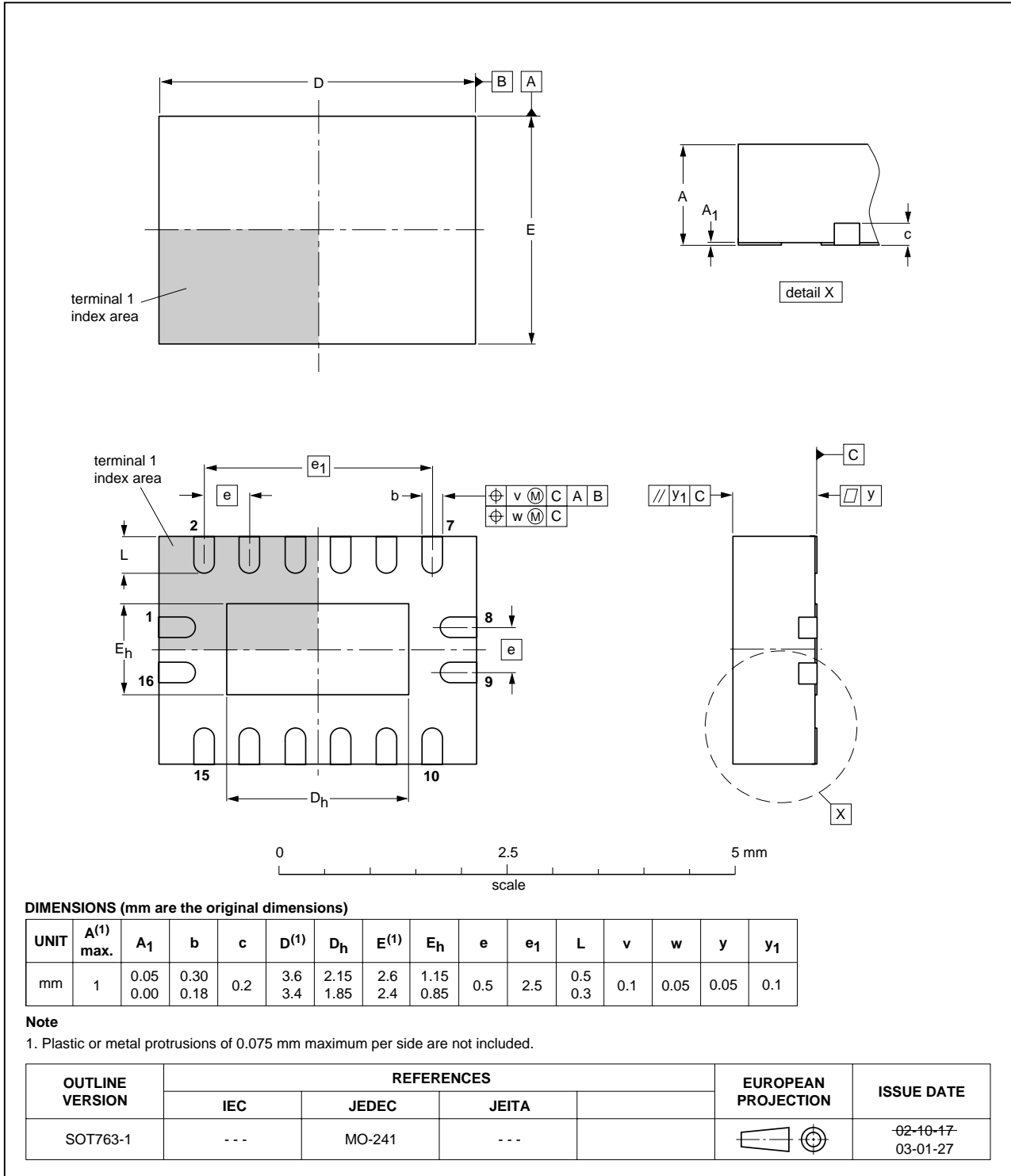


Fig 13. Package outline SOT763-1 (DHVQFN16)

## 13. Abbreviations

**Table 10. Abbreviations**

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 14. Revision history

**Table 11. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT238_3	20070716	Product data sheet	-	74HC_HCT238_CNV_2
Modifications:		<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Added type number 74HC238BQ and 74HCT238BQ (DHVQFN16 package)</li> </ul>		
74HC_HCT238_CNV_2	19970828	Product specification	-	-



## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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