

PMV117EN

μ TrenchMOS™ enhanced logic level FET

Rev. 02 — 7 April 2005

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS™ technology.

1.2 Features

- Logic level threshold
- Subminiature surface-mounted package
- Very fast switching

1.3 Applications

- Battery management
- High-speed switch
- Low power DC-to-DC converter

1.4 Quick reference data

- $V_{DS} \leq 30$ V
- $I_D \leq 2.5$ A
- $R_{DS(on)} \leq 117$ m Ω ($V_{GS} = 10$ V)
- $P_{tot} \leq 0.83$ W

2. Pinning information

Table 1: Pinning

Pin	Description	Simplified outline	Symbol
1	gate (G)	<p>SOT23</p>	<p>mbb076 S</p>
2	source (S)		
3	drain (D)		

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3. Ordering information

Table 2: Ordering information

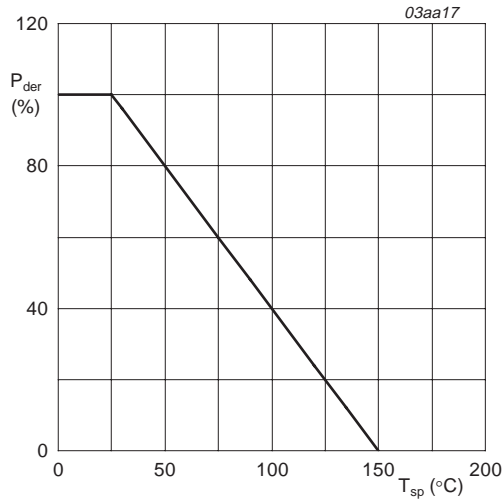
Type number	Package		
	Name	Description	Version
PMV117EN	TO-236AB	plastic surface mounted package; 3 leads	SOT23

4. Limiting values

Table 3: Limiting values

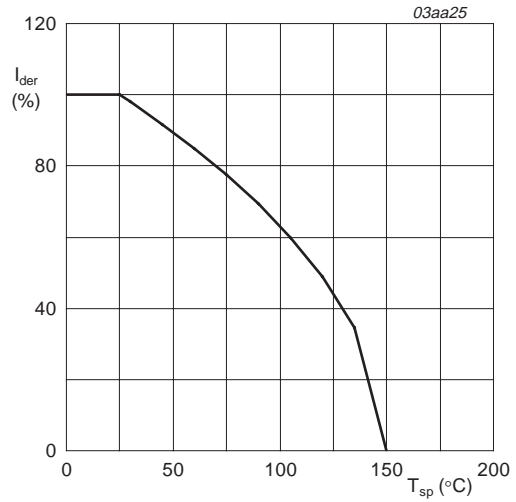
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	30	V
V_{DGR}	drain-gate voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	30	V
V_{GS}	gate-source voltage (DC)		-	± 20	V
I_D	drain current (DC)	$T_{sp} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; Figure 2 and 3	-	2.5	A
		$T_{sp} = 100\text{ °C}$; $V_{GS} = 10\text{ V}$; Figure 2	-	1.6	A
I_{DM}	peak drain current	$T_{sp} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; Figure 3	-	10	A
P_{tot}	total power dissipation	$T_{sp} = 25\text{ °C}$; Figure 1	-	0.83	W
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature		-65	+150	°C
Source-drain diode					
I_S	source (diode forward) current (DC)	$T_{sp} = 25\text{ °C}$	-	0.8	A
I_{SM}	peak source (diode forward) current	$T_{sp} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	3.3	A



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100\%$$

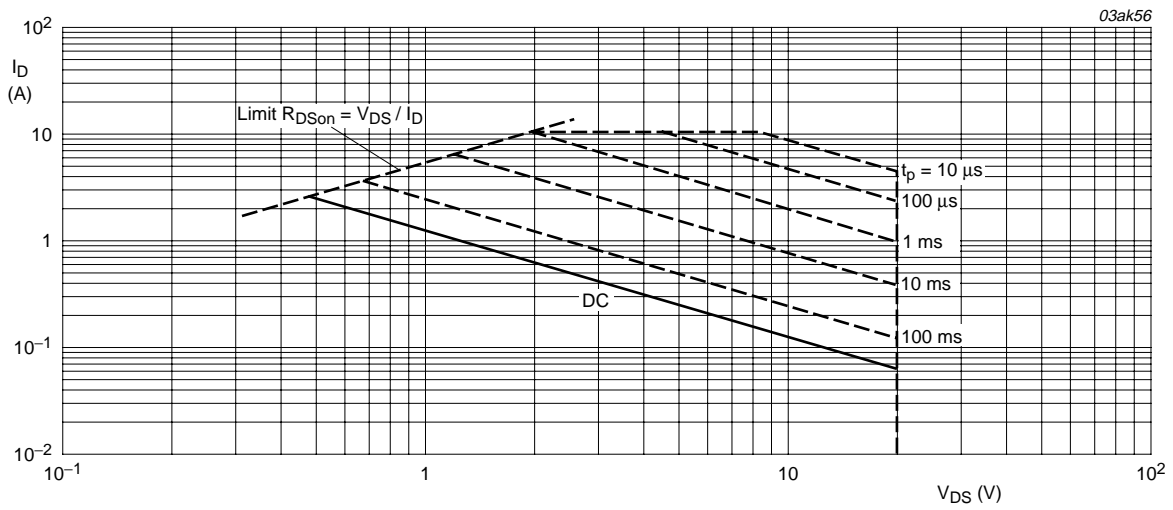
Fig 1. Normalized total power dissipation as a function of solder point temperature



$$V_{GS} \geq 10\text{ V}$$

$$I_{der} = \frac{I_D}{I_{D(25^\circ C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of solder point temperature



$T_{sp} = 25^\circ\text{C}$; I_{DM} is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	Figure 4	-	-	100	K/W

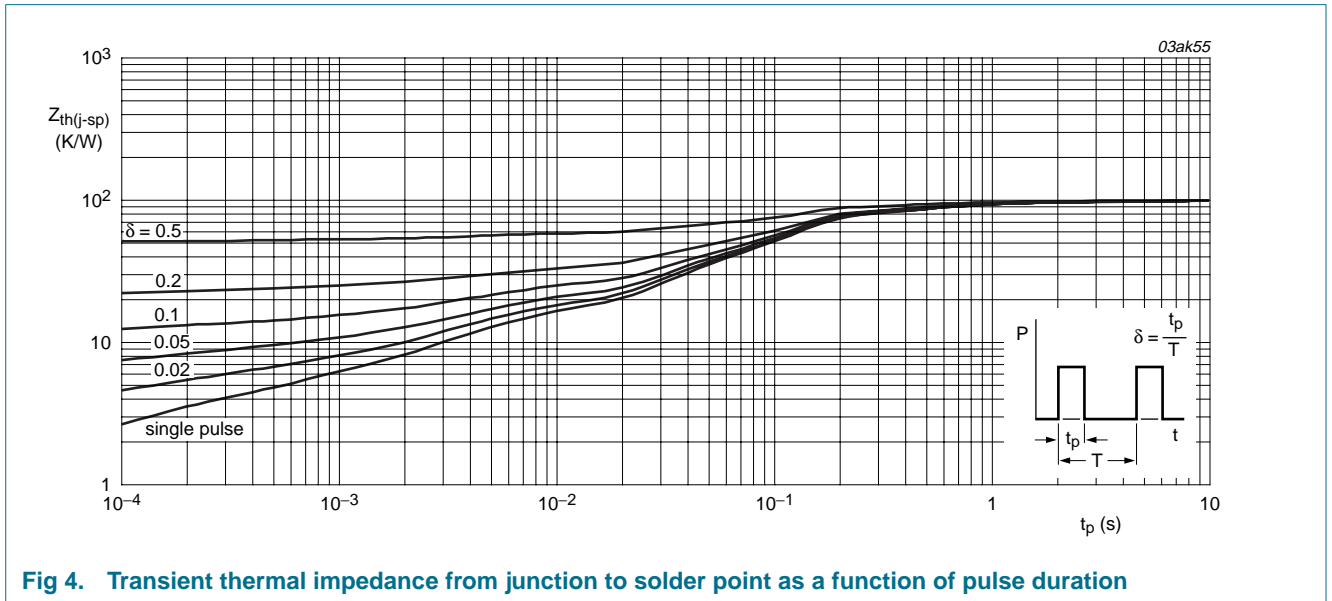


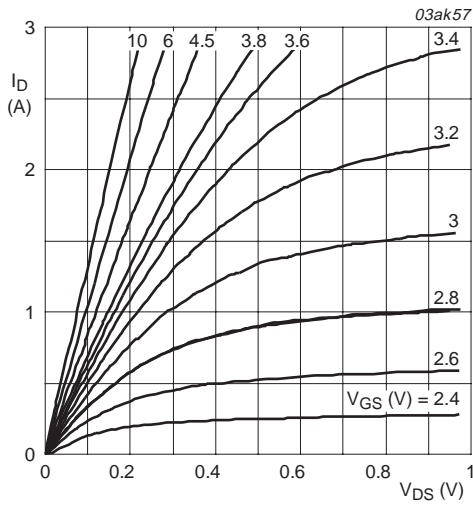
Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration

6. Characteristics

Table 5: Characteristics

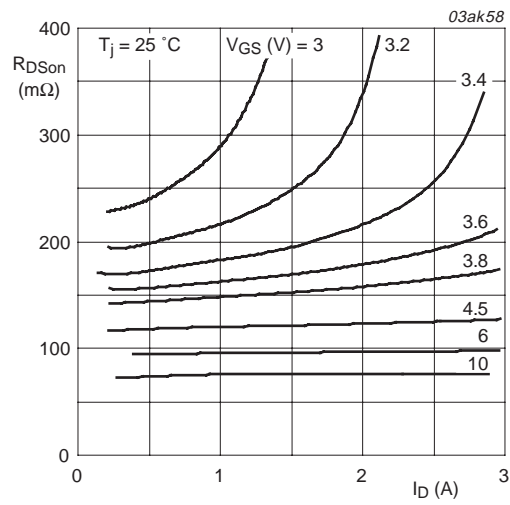
$T_j = 25\text{ °C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 10\ \mu\text{A}; V_{GS} = 0\ \text{V}$ $T_j = 25\text{ °C}$ $T_j = -55\text{ °C}$	30	37	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\ \text{mA}; V_{DS} = V_{GS}$; Figure 9 and 10 $T_j = 25\text{ °C}$ $T_j = 150\text{ °C}$ $T_j = -55\text{ °C}$	1.5	2	-	V
I_{DSS}	drain-source leakage current	$V_{DS} = 24\ \text{V}; V_{GS} = 0\ \text{V}$ $T_j = 25\text{ °C}$ $T_j = 150\text{ °C}$	-	0.01	0.5	μA
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 20\ \text{V}; V_{DS} = 0\ \text{V}$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\ \text{V}; I_D = 500\ \text{mA}$; Figure 6 and 8 $T_j = 25\text{ °C}$ $V_{GS} = 4.5\ \text{V}; I_D = 500\ \text{mA}$; Figure 6 and 8 $T_j = 25\text{ °C}$ $T_j = 150\text{ °C}$	-	74	117	mΩ
Dynamic characteristics						
$Q_{g(tot)}$	total gate charge	$I_D = 0.5\ \text{A}; V_{DD} = 15\ \text{V}; V_{GS} = 10\ \text{V}$; Figure 11	-	4.6	-	nC
Q_{gs}	gate-source charge		-	0.6	-	nC
Q_{gd}	gate-drain (Miller) charge		-	1.35	-	nC
C_{iss}	input capacitance	$V_{GS} = 0\ \text{V}; V_{DS} = 10\ \text{V}; f = 1\ \text{MHz}$; Figure 13	-	147	-	pF
C_{oss}	output capacitance		-	65	-	pF
C_{riss}	reverse transfer capacitance		-	41	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DD} = 15\ \text{V}; R_L = 15\ \Omega; V_{GS} = 10\ \text{V}$	-	4	-	ns
t_r	rise time		-	7.5	-	ns
$t_{d(off)}$	turn-off delay time		-	18	-	ns
t_f	fall time		-	13	-	ns
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	$I_S = 0.83\ \text{A}; V_{GS} = 0\ \text{V}$; Figure 12	-	0.7	1.2	V
t_{rr}	reverse recovery time	$I_S = 1\ \text{A}; dI_S/dt = -100\ \text{A}/\mu\text{s}; V_{GS} = 0\ \text{V}$; $V_{DS} = 25\ \text{V}$	-	69	-	ns



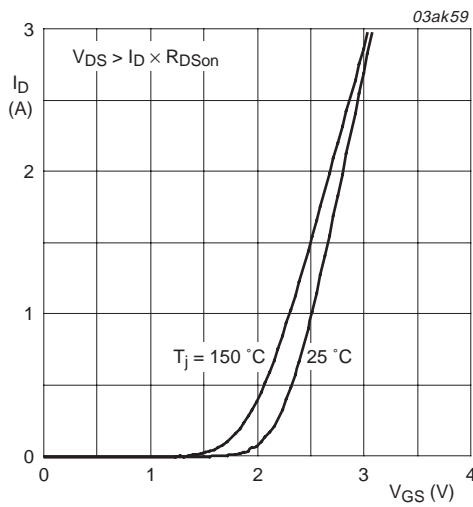
$T_j = 25\text{ }^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



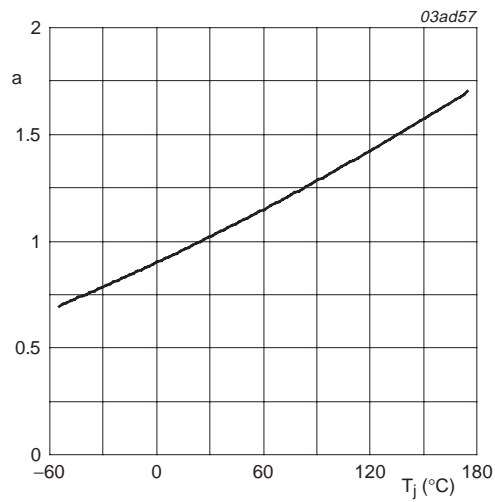
$T_j = 25\text{ }^\circ\text{C}$

Fig 6. Drain-source on-state resistance as a function of drain current; typical values



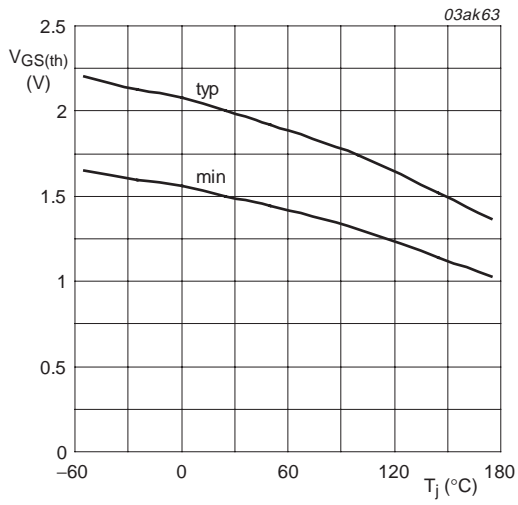
$T_j = 25\text{ }^\circ\text{C}$ and $150\text{ }^\circ\text{C}$; $V_{DS} > I_D \times R_{DSon}$

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values



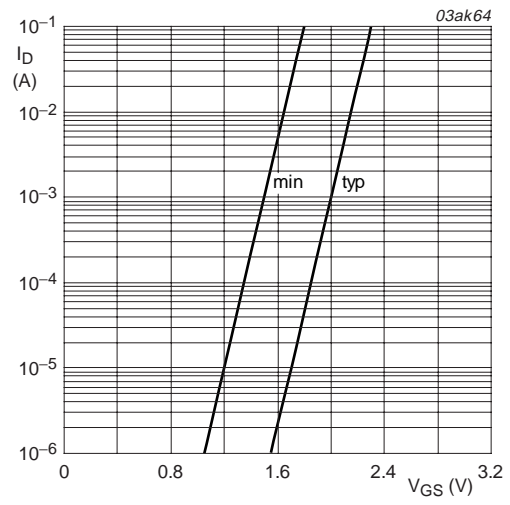
$$a = \frac{R_{DSon}}{R_{DSon(25\text{ }^\circ\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature



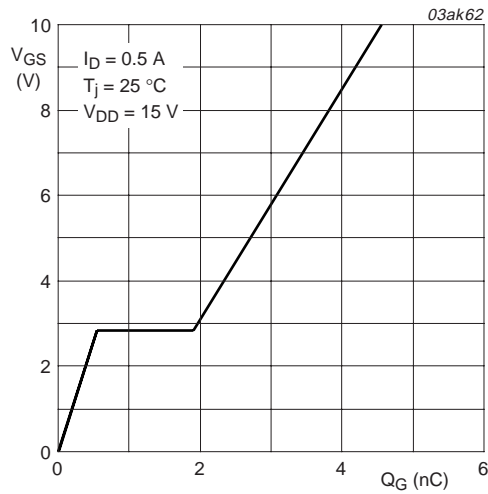
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig. 9. Gate-source threshold voltage as a function of junction temperature



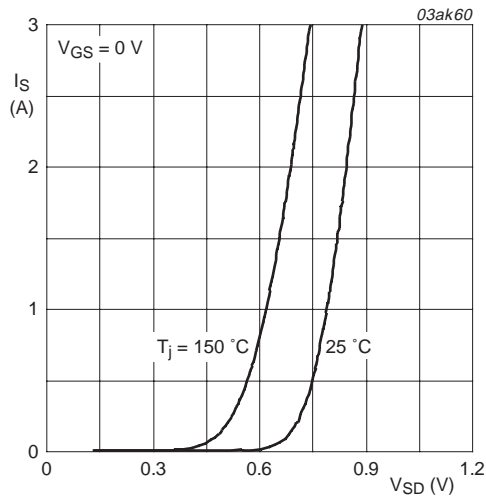
$T_j = 25 \text{ °C}; V_{DS} = 5 \text{ V}$

Fig. 10. Sub-threshold drain current as a function of gate-source voltage



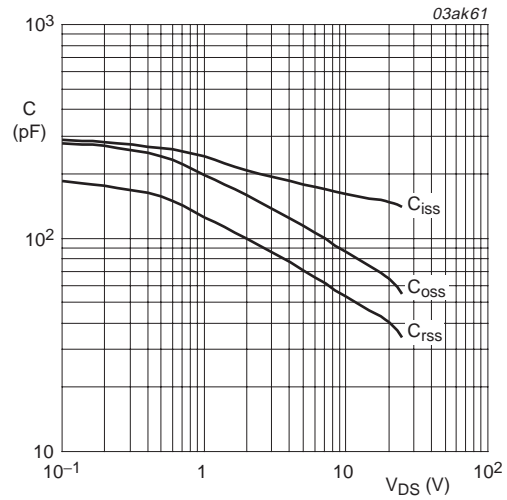
$I_D = 0.5 \text{ A}; V_{DD} = 15 \text{ V}$

Fig. 11. Gate-source voltage as a function of gate charge; typical values



$T_j = 25\text{ }^\circ\text{C}$ and $150\text{ }^\circ\text{C}$; $V_{GS} = 0\text{ V}$

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values



$V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$

Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

7. Package outline

Plastic surface mounted package; 3 leads

SOT23

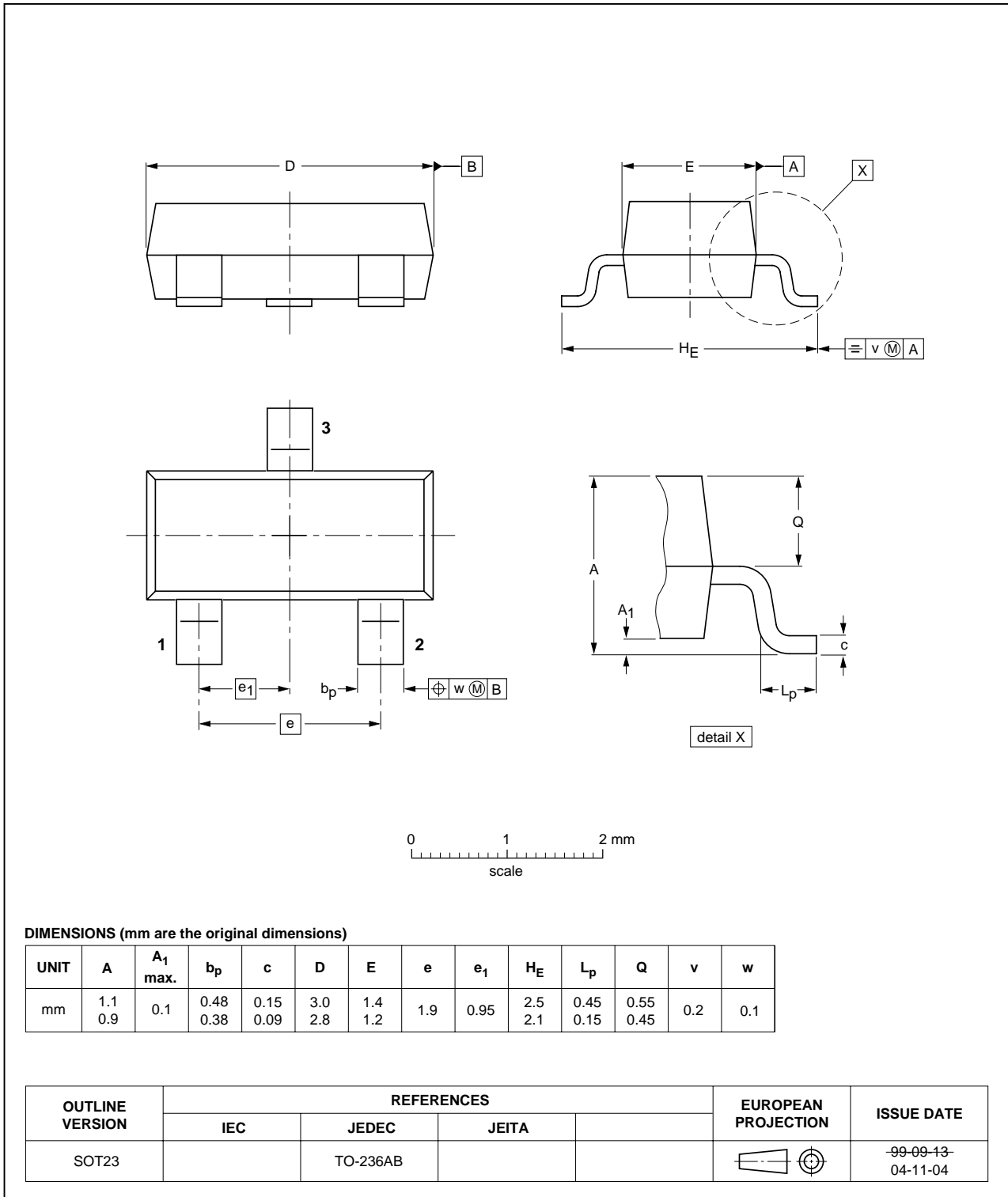


Fig 14. Package outline SOT23

8. Revision history

Table 6: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
PMV117EN_2	20050407	Product data sheet	-	9397 750 14709	PMV117EN-01
Modifications:					
			<ul style="list-style-type: none">• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors.• Table 5 “Characteristics”; correction to $V_{GS(th)}$ data• Table 2 “Ordering information”: added		
PMV117EN-01	20030226	Product data	-	9397 750 11095	-

9. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2] [3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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