PCF8591

8-bit A/D and D/A converter

Rev. 7 — 27 June 2013 Product data sheet

1. General description

The PCF8591 is a single-chip, single-supply low-power 8-bit CMOS data acquisition device with four analog inputs, one analog output and a serial I^2C-bus interface. Three address pins A0, A1 and A2 are used for programming the hardware address, allowing the use of up to eight devices connected to the I^2C-bus without additional hardware. Address, control and data to and from the device are transferred serially via the two-line bidirectional I^2C-bus.

The functions of the device include analog input multiplexing, on-chip track and hold function, 8-bit analog-to-digital conversion and an 8-bit digital-to-analog conversion. The maximum conversion rate is given by the maximum speed of the I^2C-bus.

2. Features and benefits

- Single power supply
- Operating supply voltage 2.5 V to 6.0 V
- Low standby current
- Serial input and output via I^2C-bus
- I^2C address selection by 3 hardware address pins
- Max sampling rate given by I^2C-bus speed
- 4 analog inputs configurable as single ended or differential inputs
- Auto-incremented channel selection
- Analog voltage range from V_{SS} to V_{DD}
- On-chip track and hold circuit
- 8-bit successive approximation A/D conversion
- Multiplying DAC with one analog output.

3. Applications

- Supply monitoring
- Reference setting
- Analog control loops

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCF8591P	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
PCF8591T	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1

4.1 Ordering options

Table 2. Ordering options

Product type number	Sales item (12NC)	Orderable part number	IC revision	Delivery form
PCF8591P	933768130112	PCF8591P,112	1	tube
PCF8591T/2	935276541512	PCF8591T/2,512	1	tube, dry pack
	935276541518	PCF8591T/2,518	1	tape and reel, dry pack, 13 inch

5. Marking

Table 3. Marking codes

Type number	Marking code
PCF8591P	PCF8591P
PCF8591T	PCF8591T

6. Block diagram

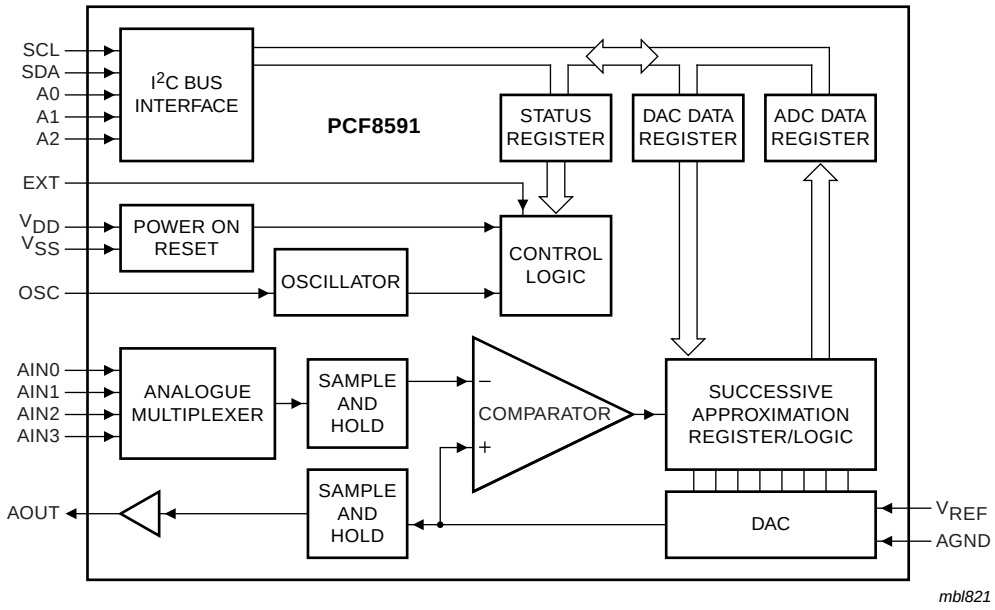
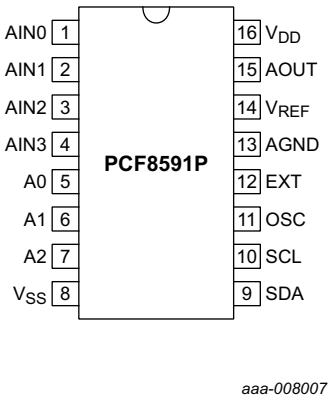


Fig 1. Block diagram of PCF8591

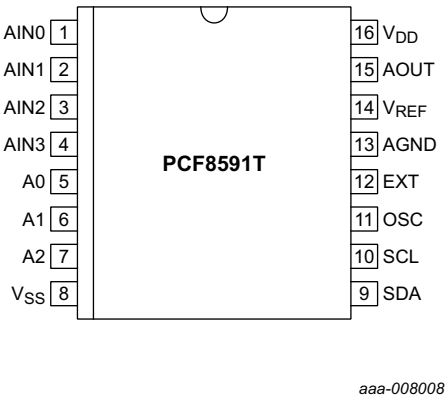
7. Pinning information

7.1 Pinning



Top view. For mechanical details, see Figure 22 on page 21.

Fig 2. Pin configuration for PCF8591P (DIP16)



Top view. For mechanical details, see Figure 23 on page 22.

Fig 3. Pin configuration for PCF8591T (SO16)

7.2 Pin description

Table 4. Pin description

Symbol	Pin	Description
AIN0	1	analog inputs (A/D converter)
AIN1	2	
AIN2	3	
AIN3	4	
A0	5	hardware slave address
A1	6	
A2	7	
V_{SS}	8	ground supply voltage
SDA	9	I^2C-bus serial data input and output
SCL	10	I^2C-bus serial clock input
OSC	11	oscillator input/output
EXT	12	external/internal switch for oscillator input
AGND	13	analog ground supply
V_{REF}	14	voltage reference input
AOUT	15	analog output (D/A converter)
V_{DD}	16	supply voltage

8. Functional description

8.1 Addressing

Each PCF8591 device in an I^2C-bus system is activated by sending a valid address to the device. The address consists of a fixed part and a programmable part. The programmable part must be set according to the address pins A0, A1 and A2. The address is always sent as the first byte after the start condition in the I^2C-bus protocol. The last bit of the address byte is the read/write-bit which sets the direction of the following data transfer (see Table 5 on page 13, Figure 15 on page 13 and Figure 16 on page 13).

8.2 Control byte

The second byte sent to a PCF8591 device is stored in its control register and is required to control the device function. The upper nibble of the control register is used for enabling the analog output, and for programming the analog inputs as single-ended or differential inputs. The lower nibble selects one of the analog input channels defined by the upper nibble (see Figure 4). If the auto-increment flag is set, the channel number is incremented automatically after each A/D conversion.

If the auto-increment mode is desired in applications where the internal oscillator is used, the analog output enable flag must be set in the control byte (bit 6). This allows the internal oscillator to run continuously, by this means preventing conversion errors resulting from oscillator start-up delay. The analog output enable flag can be reset at other times to reduce quiescent power consumption.

The selection of a non-existing input channel results in the highest available channel number being allocated. Therefore, if the auto-increment flag is set, the next selected channel is always channel 0. The most significant bits of both nibbles are reserved for possible future functions and must be set to logic 0. After a Power-On Reset (POR) condition, all bits of the control register are reset to logic 0. The D/A converter and the oscillator are disabled for power saving. The analog output is switched to a high-impedance state.

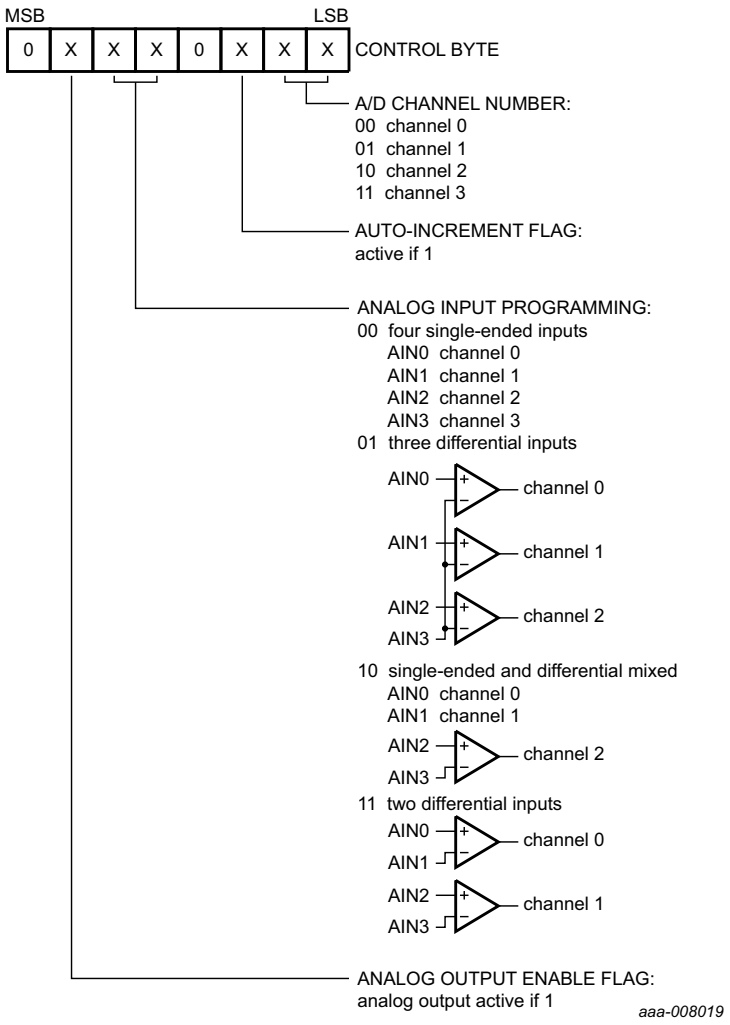


Fig 4. Control byte

8.3 D/A conversion

The third byte sent to a PCF8591 device is stored in the DAC data register and is converted to the corresponding analog voltage using the on-chip D/A converter. This D/A converter consists of a resistor divider chain connected to the external reference voltage with 256 taps and selection switches. The tap-decoder switches one of these taps to the DAC output line (see Figure 5).

The analog output voltage is buffered by an auto-zeroed unity gain amplifier. Setting the analog output enable flag of the control register switches this buffer amp on or off. In the active state, the output voltage is held until a further data byte is sent.

The on-chip D/A converter is also used for successive approximation A/D conversion. In order to release the DAC for an A/D conversion cycle the unity gain amplifier is equipped with a track and hold circuit. This circuit holds the output voltage while executing the A/D conversion.

The formula for the output voltage supplied to the analog output AOUT is shown in Figure 6. The waveforms of a D/A conversion sequence are shown in Figure 7.

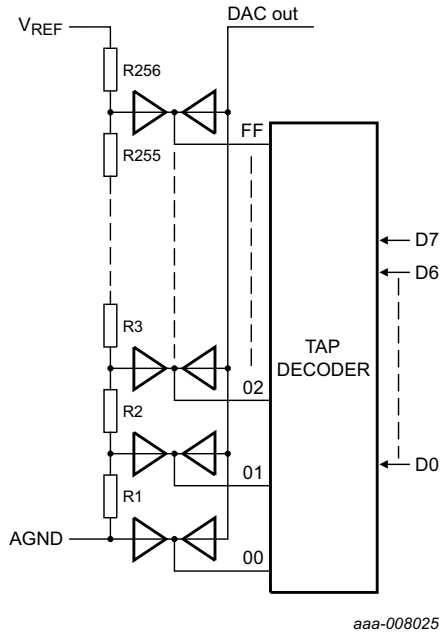


Fig 5. DAC resistor divider chain

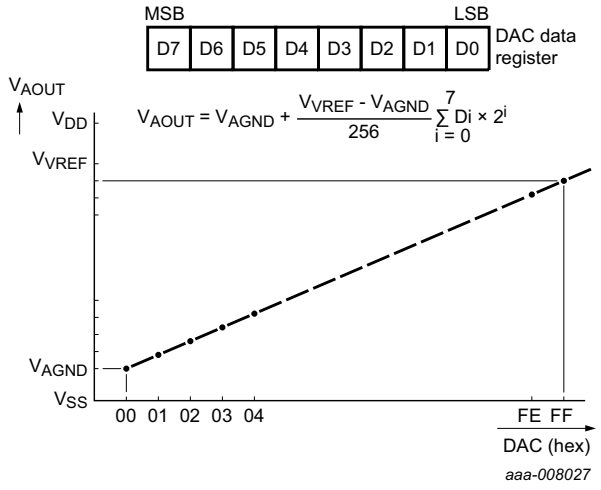


Fig 6. DAC data and DC conversion characteristics

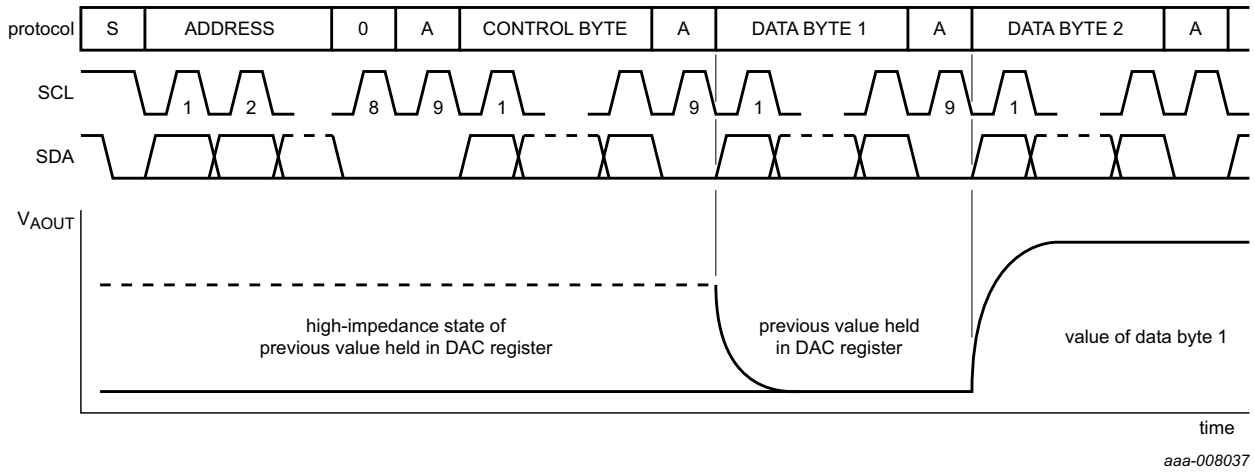


Fig 7. D/A conversion sequence

8.4 A/D conversion

The A/D converter uses the successive approximation conversion technique. The on-chip D/A converter and a high-gain comparator are used temporarily during an A/D conversion cycle.

An A/D conversion cycle is always started after sending a valid read mode address to a PCF8591 device. The A/D conversion cycle is triggered at the trailing edge of the acknowledge clock pulse and is executed while transmitting the result of the previous conversion (see Figure 8).

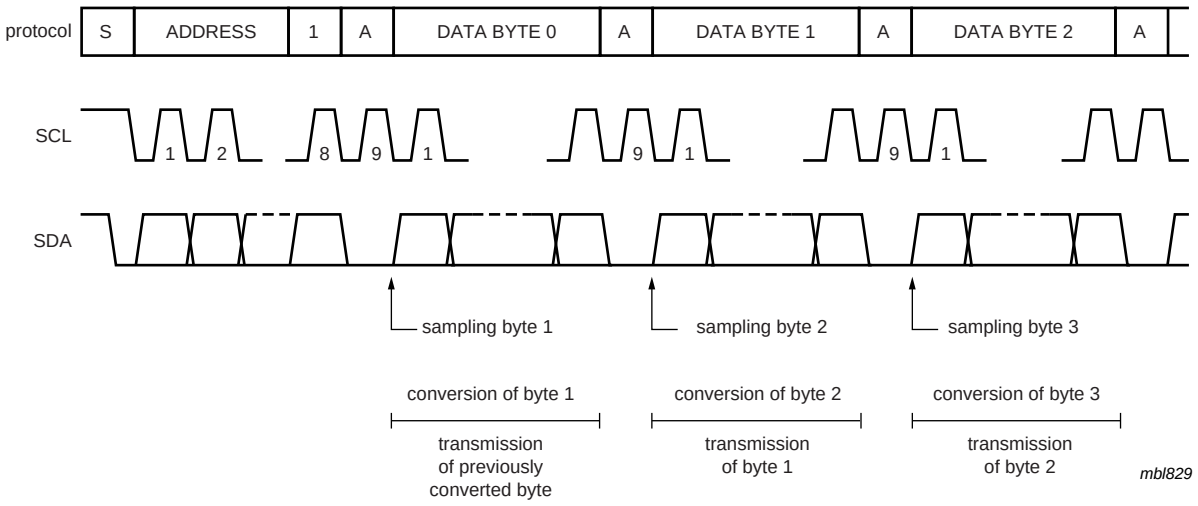


Fig 8. A/D conversion sequence

Once a conversion cycle is triggered, an input voltage sample of the selected channel is stored on the chip and is converted to the corresponding 8-bit binary code. Samples picked up from differential inputs are converted to an 8-bit two's complement code (see Figure 9 and Figure 10).

The conversion result is stored in the ADC data register and awaits transmission. If the auto-increment flag is set, the next channel is selected.

The first byte transmitted in a read cycle contains the conversion result code of the previous read cycle. After a POR condition, the first byte read is 80h. The protocol of an I^2C-bus read cycle is shown in Section 9.

The maximum A/D conversion rate is given by the actual speed of the I^2C-bus.

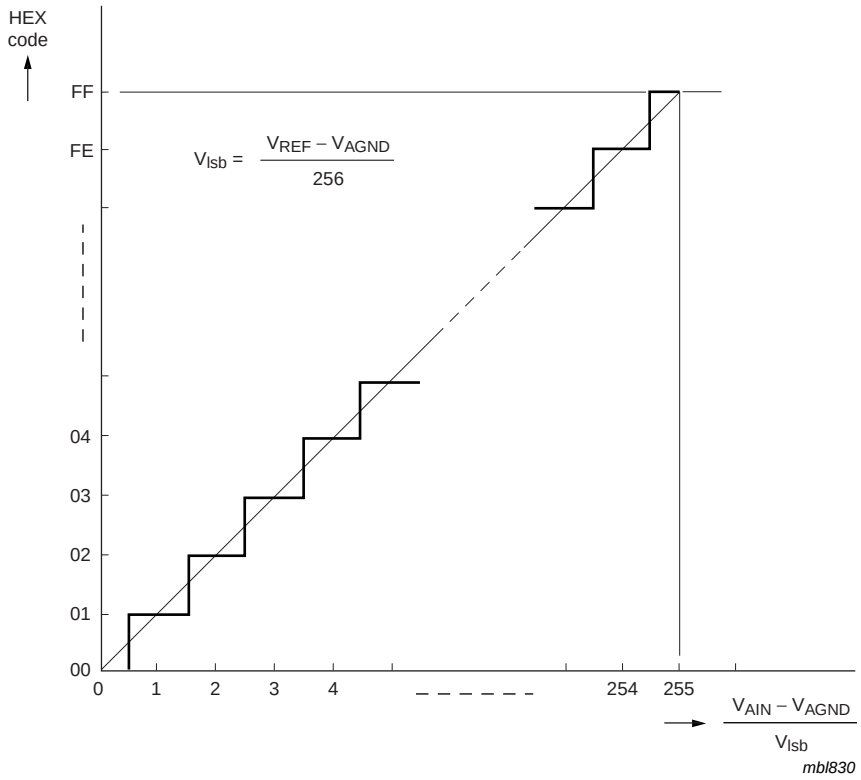


Fig 9. A/D conversion characteristics of single ended inputs

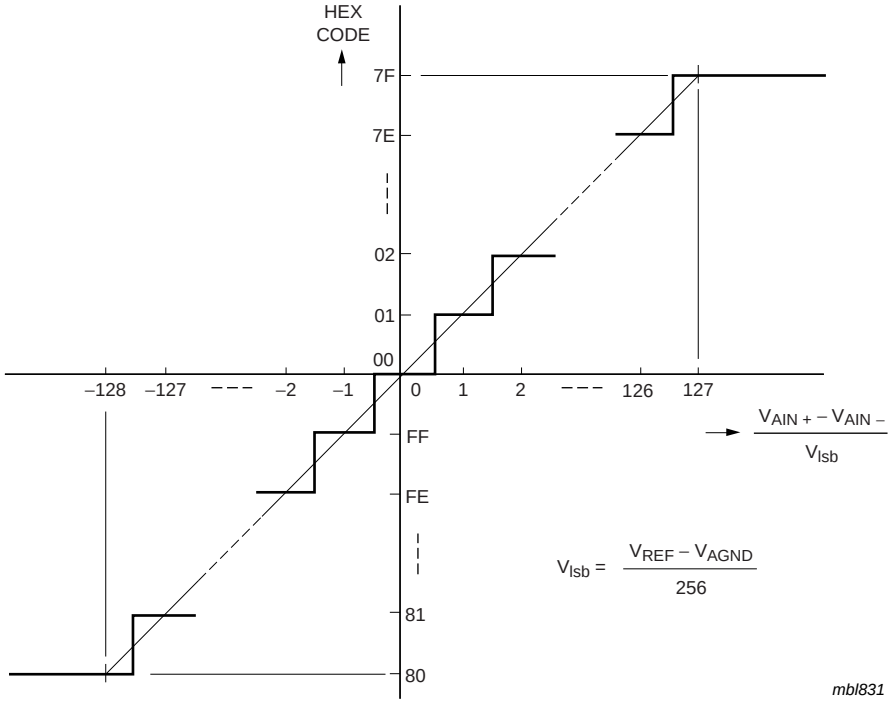


Fig 10. A/D conversion characteristics of differential inputs

8.5 Reference voltage

For the D/A and A/D conversion, either a stable external voltage reference or the supply voltage must be applied to the resistor divider chain (pins V_{REF} and AGND). The AGND pin has to be connected to the system analog ground. It may have a DC off-set with reference to V_{SS}.

A low frequency can be applied to the V_{REF} and AGND pins. This allows the use of the D/A converter as a one-quadrant multiplier (see Section 10 and Figure 6)

The A/D converter can also be used as a one or two quadrant analog divider. The analog input voltage is divided by the reference voltage. The result is converted to a binary code. In this application, the reference voltage must be kept stable during the conversion cycle.

8.6 Oscillator

An on-chip oscillator generates the clock signal required for the A/D conversion cycle and for refreshing the auto-zeroed buffer amplifier. When using this oscillator the EXT pin must be connected to V_{SS}. The oscillator frequency is available at the OSC pin.

If the EXT pin is connected to V_{DD}, the oscillator output OSC is switched to a high-impedance state allowing to feed an external clock signal to OSC.

9. Characteristics of the I²C bus

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial DAta line (SDA) and a Serial CLock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

9.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse, as changes in the data line at this time are interpreted as a control signal (see Figure 11).

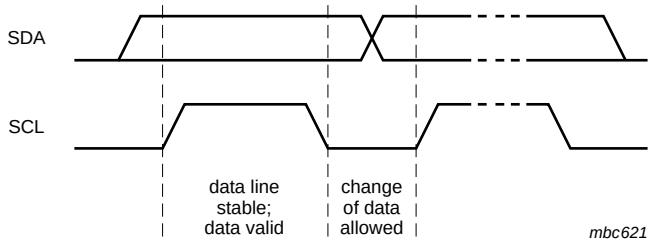


Fig 11. Bit transfer

9.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy.

A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition - S.

A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition - P (see Figure 12).

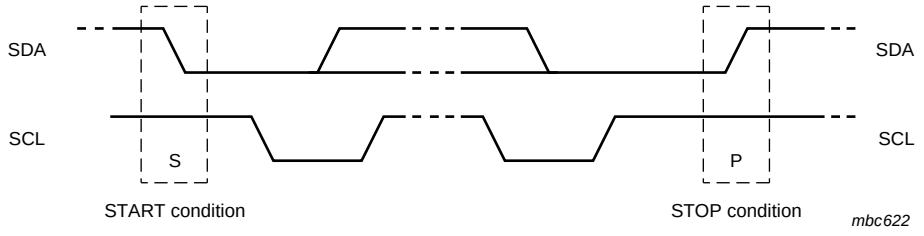


Fig 12. Definition of START and STOP conditions

9.3 System configuration

A device generating a message is a transmitter; a device receiving a message is a receiver. The device that controls the message is the master; and the devices which are controlled by the master are the slaves (see Figure 13).

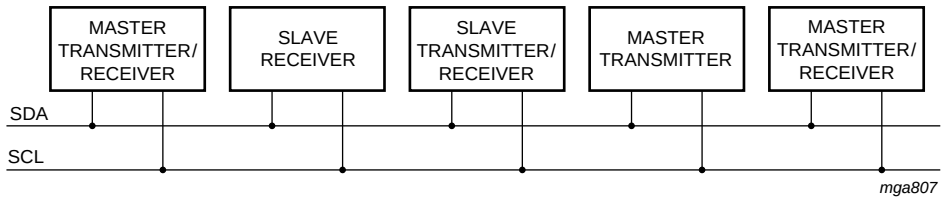


Fig 13. System configuration

9.4 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of 8 bits is followed by an acknowledge cycle.

- A slave receiver, which is addressed, must generate an acknowledge after the reception of each byte
- Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter
- The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be considered)
- A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition

Acknowledgement on the I^{2}C-bus is shown in Figure 14.

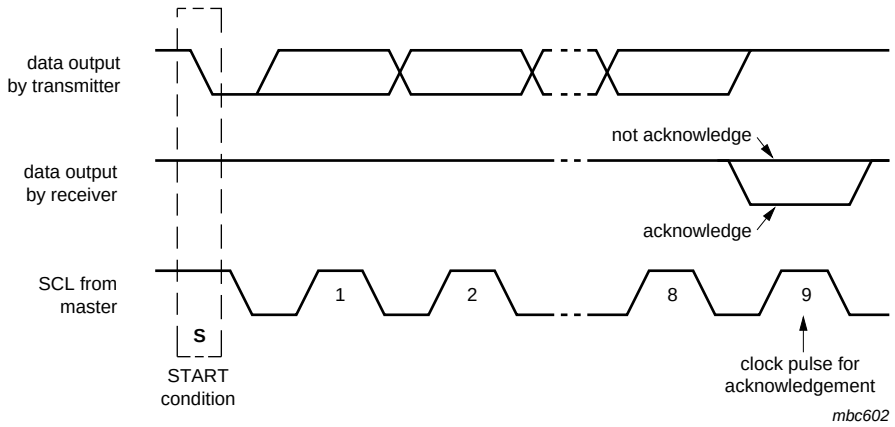


Fig 14. Acknowledgement on the I^{2}C-bus

9.5 I^{2}C bus protocol

After a START condition, the I^{2}C slave address has to be sent to the PCF8591 device.

Eight different I²C-bus slave addresses can be used to address the PCF8591 (see Table 5).

Table 5. I²C slave address byte

Bit	Slave address							
	7 MSB	6	5	4	3	2	1	0 LSB
slave address	1	0	0	1	A2	A1	A0	R/$\overline{W}$

The least significant bit of the slave address byte is bit R/$\overline{W}$ (see Table 6).

Table 6. R/$\overline{W}$-bit description

R/$\overline{W}$	Description
0	write data
1	read data

Bit 1 to bit 3 of the slave address are defined by connecting the input pins A0 to A2 to either V_{SS} (logic 0) or V_{DD} (logic 1). Therefore, eight instances of PCF8591 can be distinguished on the same I²C-bus.

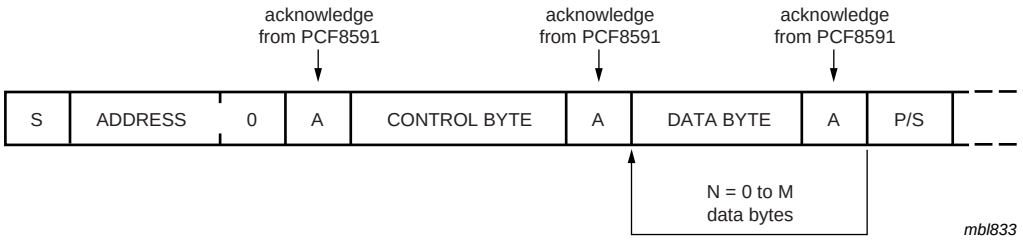


Fig 15. Bus protocol for write mode, D/A conversion

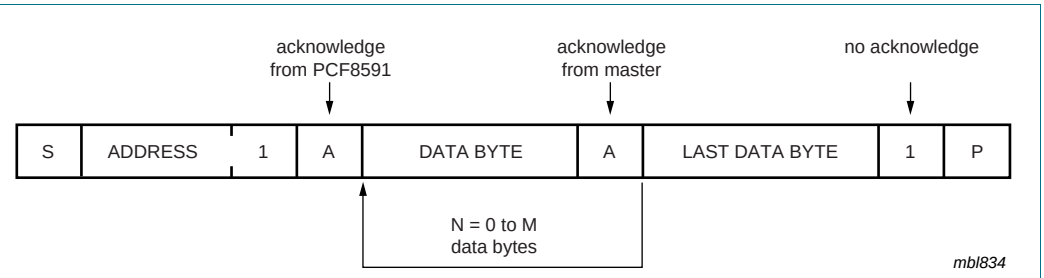


Fig 16. Bus protocol for read mode, A/D conversion

10. Application design-in information

Inputs must be connected to V_{SS} or V_{DD} when not in use. Analog inputs may also be connected to AGND or V_{REF}.

In order to prevent excessive ground and supply noise and to minimize crosstalk of the digital to analog signal paths the printed-circuit board layout must be very carefully designed. Supply lines common to a PCF8591 device and noisy digital circuits and ground loops should be avoided. Decoupling capacitors (>10 μF) are recommended for power supply and reference voltage inputs.

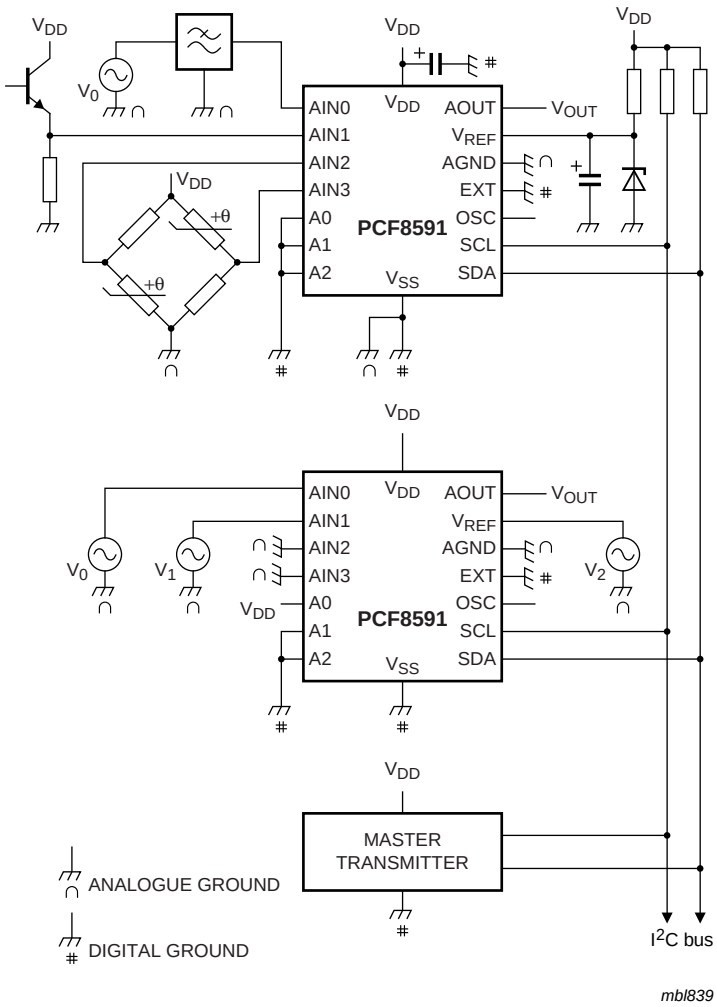


Fig 17. Application diagram

11. Internal circuitry

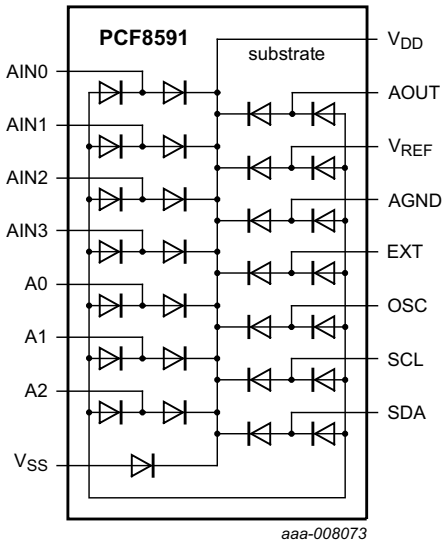


Fig 18. Device protection diagram

12. Safety notes

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

13. Limiting values

Table 7. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			–0.5	+8.0	V
V_I	input voltage	any input		–0.5	V_{DD} + 0.5	V
I_I	input current			-	±10	mA
I_O	output current			-	±20	mA
I_{DD}	supply current			-	±50	mA
I_{SS}	ground supply current			-	±50	mA
P_{tot}	total power dissipation	per package		-	300	mW
P/out	power dissipation per output			-	100	mW
V_{ESD}	electrostatic discharge voltage	HBM	[1]	-	±3000	V
		MM	[2]	-	±300	V
I_{lu}	latch-up current		[3]	-	200	mA
T_{amb}	ambient temperature	operating device		–40	+85	°C
T_{stg}	storage temperature		[4]	–65	+150	°C

[1] Pass level; Human Body Model (HBM), according to Ref. 6 “JESD22-A114”.

[2] Pass level; Machine Model (MM), according to Ref. 7 “JESD22-A115”.

[3] Pass level; latch-up testing according to Ref. 8 “JESD78” at maximum ambient temperature ($T_{amb(max)}$).

[4] According to the store and transport requirements (see Ref. 12 “UM10569”) the devices have to be stored at a temperature of +8 °C to +45 °C and a humidity of 25 % to 75 %.

14. Characteristics

14.1 Static characteristics

Table 8. Characteristics

V_{DD} = 2.5 V to 6.0 V; V_{SS} = 0; T_{amb} = −40 °C to +85 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supply							
V_{DD}	supply voltage			2.5	-	6.0	V
I_{DD}	supply current						
		standby; $V_I = V_{SS}$ or V_{DD}; no load		-	1	15	μA
		operating; f_{SCL} = 100 kHz					
		AOUT off		-	125	250	μA
		AOUT active		-	0.45	1.0	mA
V_{POR}	power-on reset voltage		[1]	0.8	-	2.0	V
Digital in- and outputs: SCL, SDA, A0, A1, A2							
V_{IL}	LOW-level input voltage			0	-	$0.3 \times V_{DD}$	V
V_{IH}	HIGH-level input voltage			$0.7 \times V_{DD}$	-	V_{DD}	V
I_L	leakage current	$V_I = V_{SS}$ to V_{DD}					
		A0, A1, A2		−250	-	+250	nA
		SCL, SDA		−1	-	+1	μA
C_i	input capacitance			-	-	5	pF
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		3.0	-	-	mA
Reference voltage inputs							
V_{ref}	reference voltage	$V_{ref} > V_{AGND}$	[2]	V_{SS} + 1.6	-	V_{DD}	V
V_{AGND}	voltage on pin AGND	$V_{ref} > V_{AGND}$	[2]	V_{SS}	-	V_{DD} − 0.8	V
I_{LI}	input leakage current			−250	-	+250	nA
R_{ref}	reference resistance	pins V_{REF} and AGND		-	100	-	kΩ
Oscillator: OSC, EXT							
I_{LI}	input leakage current			-	-	250	nA
f_{OSC}	oscillator frequency			0.75	-	1.25	MHz

[1] The power-on reset circuit resets the I^2C-bus logic when V_{DD} is less than V_{POR}.

[2] A further extension of the range is possible, if the following conditions are fulfilled: $\frac{V_{ref} + V_{AGND}}{2} \geq 0.8$ V,

$V_{DD} - \frac{V_{ref} + V_{AGND}}{2} \geq 0.4$ V.

14.2 D/A characteristics

Table 9. D/A characteristics

V_{DD} = 5.0 V; V_{SS} = 0; V_{REF} =5.0 V; V_{AGND} = 0 V; R_L = 10 kΩ; C_L = 100 pF; T_{amb} = −40 °C to +85 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Analog output						
V_{oa}	analog output voltage	no resistive load	V_{SS}	-	V_{DD}	V
		R_L = 10 kΩ	V_{SS}	-	0.9 × V_{DD}	V
I_{LO}	output leakage current	AOUT disabled	-	-	250	nA
Accuracy						
E_O	offset error	T_{amb} = 25 °C	-	-	50	mV
E_L	linearity error		-	-	±1.5	LSB
E_G	gain error	no resistive load	-	-	1	%
$t_{s(DAC)}$	DAC settling time	to 1/2 LSB full scale	-	-	90	µs
$f_{c(DAC)}$	DAC conversion frequency		-	-	11.1	kHz
SNRR	supply noise rejection ratio	f = 100 Hz; V_{DDN} = 0.1 × V_{PP}	-	40	-	dB

14.3 A/D characteristics

Table 10. A/D characteristics

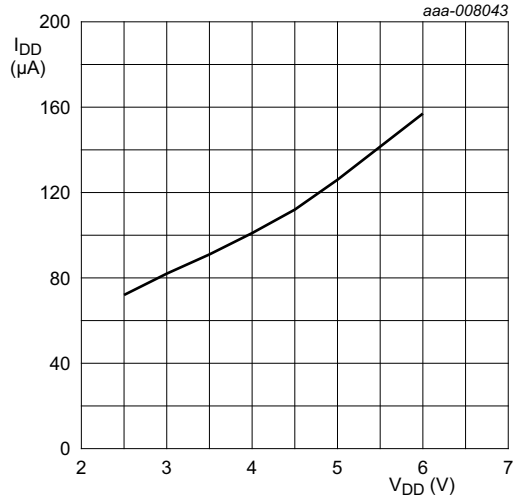
V_{DD} = 5.0 V; V_{SS} = 0; V_{REF} =5.0 V; V_{AGND} = 0 V; R_S = 10 kΩ; T_{amb} = −40 °C to +85 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Analog inputs						
V_{ia}	analog input voltage		V_{SS}	-	V_{DD}	V
I_{LIA}	analog input leakage current		-	-	100	nA
$C_{i(a)}$	analog input capacitance		-	10	-	pF
$C_{i(dif)}$	differential input capacitance		-	10	-	pF
$V_{i(se)}$	single-ended input voltage	measuring range	V_{AGND}	-	V_{REF}	V
$V_{i(dif)}$	differential input voltage	measuring range: V_{FS} = V_{REF} - V_{AGND}	$\frac{-V_{FS}}{2}$	-	$\frac{+V_{FS}}{2}$	V
Accuracy						
E_O	offset error	T_{amb} = 25 °C	-	-	20	mV
E_L	linearity error		-	-	±1.5	LSB
E_G	gain error		-	-	1	%
		small signal; ΔV_i = 16 LSB	-	-	5	%
CMRR	common mode rejection ratio		-	60	-	dB

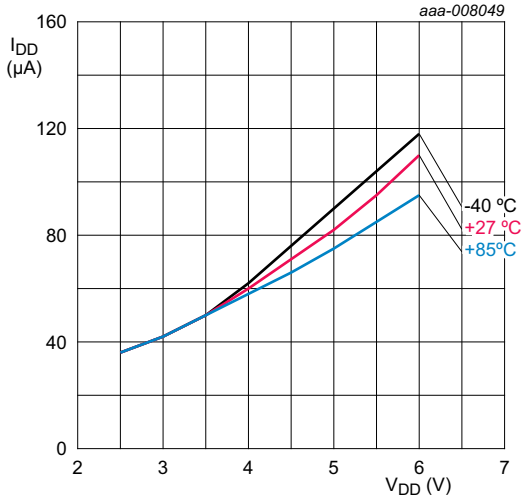
Table 10. A/D characteristics *...continued*

V_{DD} = 5.0 V; V_{SS} = 0; V_{REF} =5.0 V; V_{AGND} = 0 V; R_S = 10 kΩ; T_{amb} = −40 °C to +85 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SNRR	supply noise rejection ratio	f = 100 Hz; $V_{DDN} = 0.1 \times V_{PP}$	-	40	-	dB
t_{conv}	conversion time		-	-	90	µs
f_s	sampling frequency		-	-	11.1	kHz

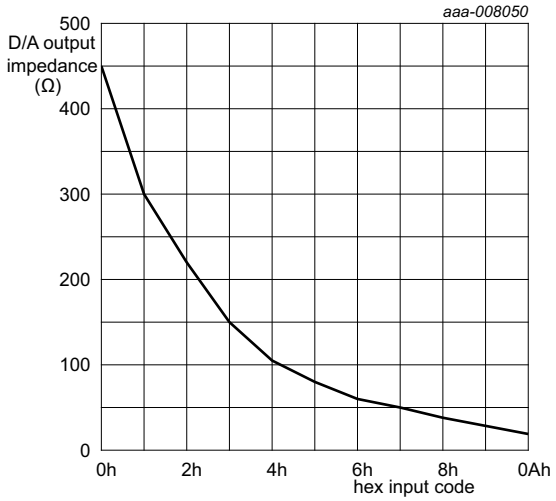


a. internal oscillator; T_{amb} = +27 °C

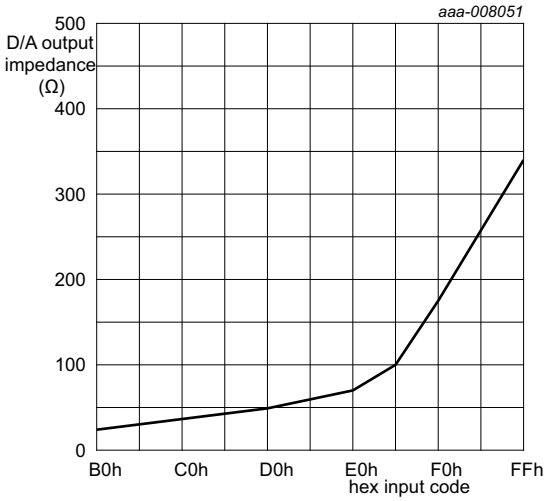


b. External oscillator

Fig 19. Operating supply current as a function of supply voltage (analog output disabled)



a. Output impedance near negative power rail; T_{amb} = +27 × °C



b. Output impedance near positive power rail; T_{amb} = +27 × °C

Fig 20. Output impedance of analog output buffer (near power rails)

14.4 Dynamic characteristics

Table 11. Dynamic characteristics

All timing characteristics are valid within the operating supply voltage and ambient temperature range and reference to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

Symbol	Parameter		Min	Typ	Max	Unit
I^2C bus timing (see Figure 21)		[1]				
f_{SCL}	SCL clock frequency		-	-	100	kHz
t_{SP}	pulse width of spikes that must be suppressed by the input filter		-	-	100	ns
t_{BUF}	bus free time between a STOP and START condition		4.7	-	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	-	-	µs
$t_{HD;STA}$	hold time (repeated) START condition		4.0	-	-	µs
t_{LOW}	LOW period of the SCL clock		4.7	-	-	µs
t_{HIGH}	HIGH period of the SCL clock		4.0	-	-	µs
t_r	rise time of both SDA and SCL signals		-	-	1.0	µs
t_f	fall time of both SDA and SCL signals		-	-	0.3	µs
$t_{SU;DAT}$	data set-up time		250	-	-	µs
$t_{HD;DAT}$	data hold time		0	-	-	µs
$t_{VD;DAT}$	data valid time		-	-	3.4	µs
$t_{SU;STO}$	set-up time for STOP condition		4.0	-	-	µs

[1] A detailed description of the I^2C bus specification, with applications, is given in Ref. 11 “UM10204”.

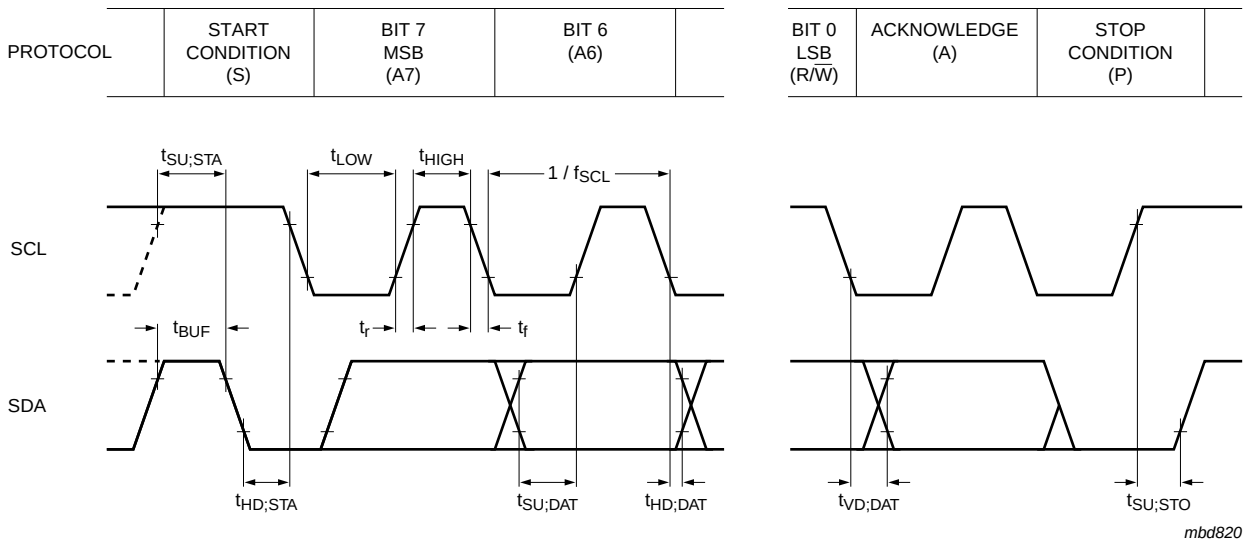
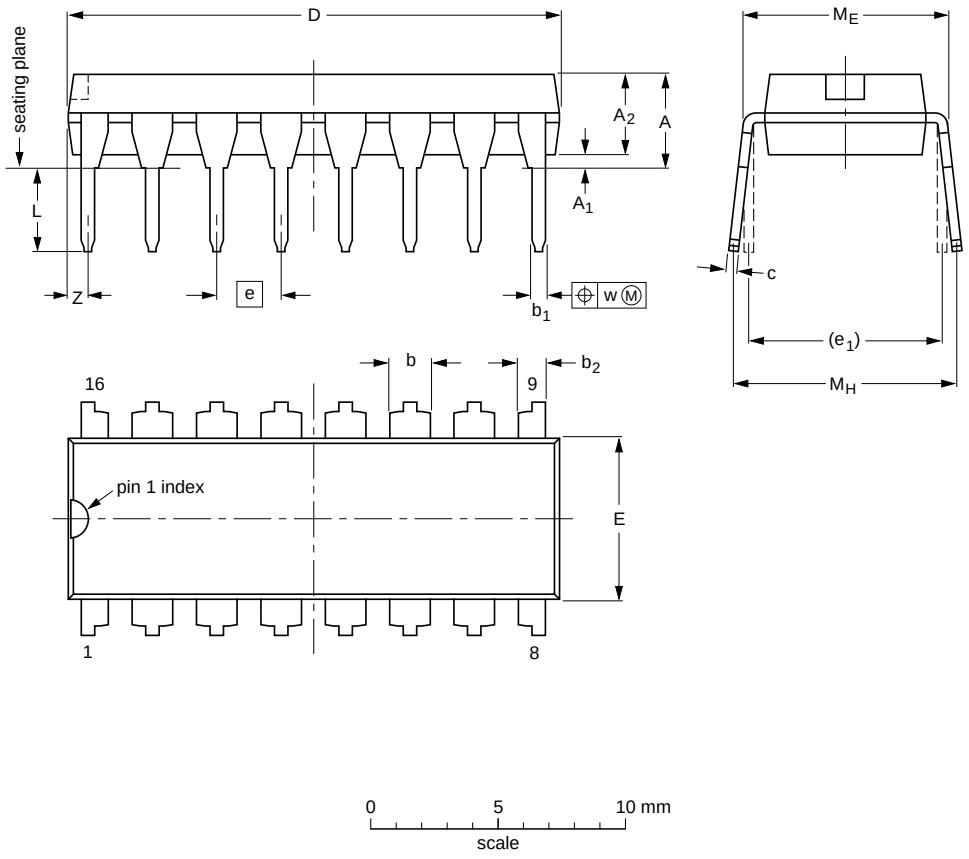


Fig 21. I^2C bus timing diagram; rise and fall times refer to V_{IL} and V_{IH}

15. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil) **SOT38-4**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.03

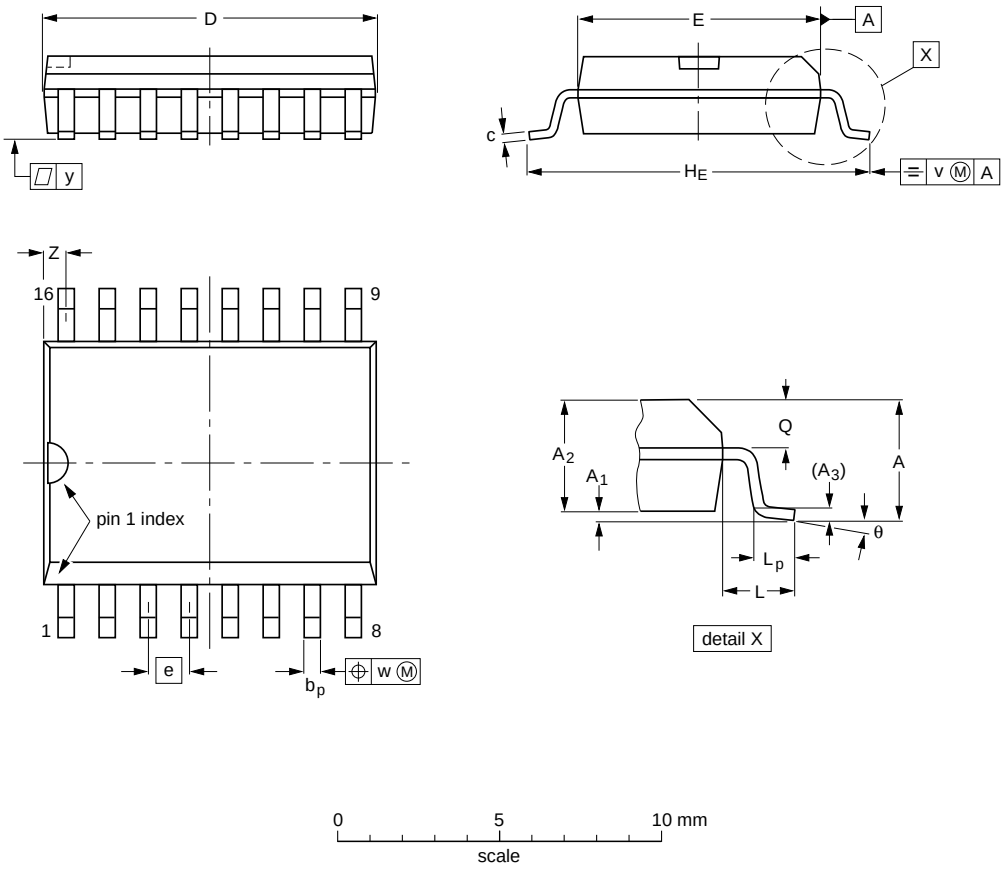
Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT38-4						~~95-01-14~~ 03-02-13

Fig 22. DIP16: plastic dual in-line package; 16 leads (300 mil)

SO16: plastic small outline package; 16 leads; body width 7.5 mm **SOT162-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	10.5 10.1	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.41 0.40	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT162-1	075E03	MS-013				~~99-12-27~~ 03-02-19

Fig 23. SO16: plastic small outline package; 16 leads: body width 7.5 mm

16. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 24) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 12 and 13

Table 12. SnPb eutectic process (from J-STD-020D)

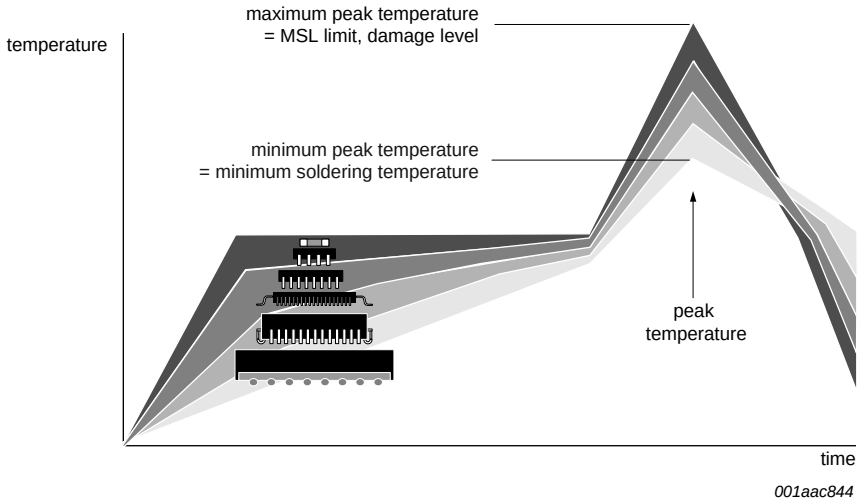
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 13. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 24.



MSL: Moisture Sensitivity Level

Fig 24. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

17. References

[1] **AN10365 —** Surface mount reflow soldering description

[2] **AN10853 —** ESD and EMC sensitivity of IC

[3] **IEC 60134 —** Rating systems for electronic tubes and valves and analogous semiconductor devices

[4] **IEC 61340-5 —** Protection of electronic devices from electrostatic phenomena

[5] **IPC/JEDEC J-STD-020D —** Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices

[6] **JESD22-A114 —** Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)

[7] **JESD22-A115 —** Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM)

[8] **JESD78 —** IC Latch-Up Test

[9] **JESD625-A —** Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices

[10] **SNV-FA-01-02 —** Marking Formats Integrated Circuits

[11] **UM10204 —** I^2C-bus specification and user manual

[12] **UM10569 —** Store and transport requirements

18. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCF8591 v.7	20130627	Product data sheet	-	PCF8591 v.6
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate.			
PCF8591 v.6	20030127	Product data sheet	-	PCF8591 v.5
PCF8591 v.5	20011213	Product data sheet	-	PCF8591 v.4
PCF8591 v.4	19980702	Product data sheet	-	PCF8591 v.3
PCF8591 v.3	19970402	Product data sheet	-	PCF8591 v.2
PCF8591 v.2	19910901	Product data sheet	-	PCF8591 v.1
PCF8591 v.1	19860627	Product data sheet	-	-

19. Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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21. Tables

22. Figures

23. Contents

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