

74HC165-Q100; 74HCT165-Q100

8-bit parallel-in/serial out shift register

Rev. 1 — 17 July 2012

Product data sheet

1. General description

The 74HC165-Q100; 74HCT165-Q100 are high-speed Si-gate CMOS devices that comply with JEDEC standard no. 7A. They are pin compatible with Low-power Schottky TTL (LSTTL).

The 74HC165-Q100; 74HCT165-Q100 are 8-bit parallel-load or serial-in shift registers with complementary serial outputs (Q_7 and $\overline{Q_7}$) available from the last stage. When the parallel load (\overline{PL}) input is LOW, parallel data from the D0 to D7 inputs are loaded into the register asynchronously.

When \overline{PL} is HIGH, data enters the register serially at the DS input and shifts one place to the right ($Q_0 \rightarrow Q_1 \rightarrow Q_2$, etc.) with each positive-going clock transition. This feature allows parallel-to-serial converter expansion by tying the Q_7 output to the DS input of the succeeding stage.

The clock input is a gated-OR structure which allows one input to be used as an active LOW clock enable (\overline{CE}) input. The pin assignment for the CP and \overline{CE} inputs is arbitrary and can be reversed for layout convenience. The LOW-to-HIGH transition of input \overline{CE} should only take place while CP HIGH for predictable operation. Either the CP or the \overline{CE} should be HIGH before the LOW-to-HIGH transition of PL to prevent shifting the data when PL is activated.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - ◆ Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$
- Asynchronous 8-bit parallel load
- Synchronous serial input
- Complies with JEDEC standard no. 7A
- ESD protection:
 - ◆ MIL-STD-883, method 3015 exceeds 2000 V
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V ($C = 200\text{ pF}$, $R = 0\text{ }\Omega$)
- Multiple package options

3. Applications

- Parallel-to-serial data conversion

4. Ordering information

Table 1. Ordering information

| Type number | Package | | | Version |
|-----------------------------------|-------------------|----------|--|----------|
| | Temperature range | Name | Description | |
| 74HC165D-Q100 74HCT165D-Q100 | -40 °C to +125 °C | SO16 | plastic small outline package; 16 leads; body width 3.9 mm | SOT109-1 |
| 74HC165PW-Q100 74HCT165PW-Q100 | -40 °C to +125 °C | TSSOP16 | plastic thin shrink small outline package; 16 leads; body width 4.4 mm | SOT403-1 |
| 74HC165BQ-Q100 74HCT165BQ-Q100 | -40 °C to +125 °C | DHVQFN16 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm | SOT763-1 |

5. Functional diagram

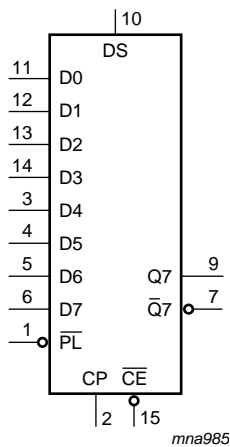


Fig 1. Logic symbol

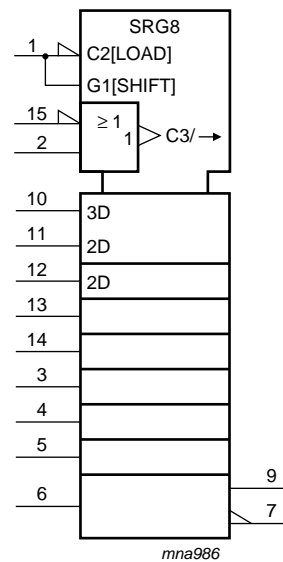


Fig 2. IEC logic symbol

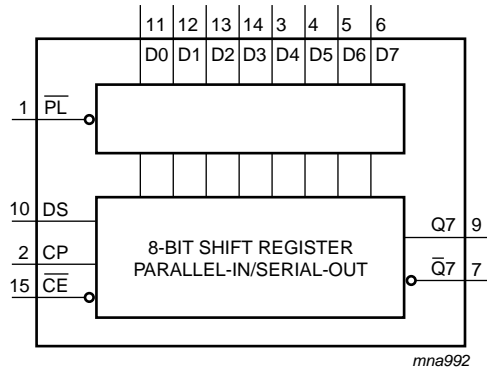


Fig 3. Functional diagram

6. Pinning information

6.1 Pinning

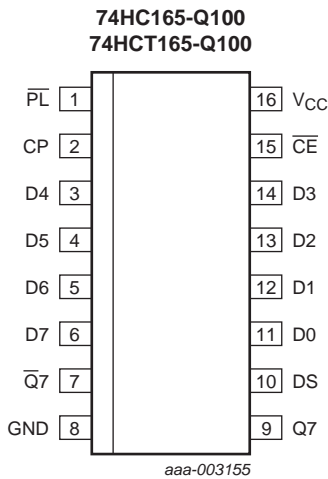
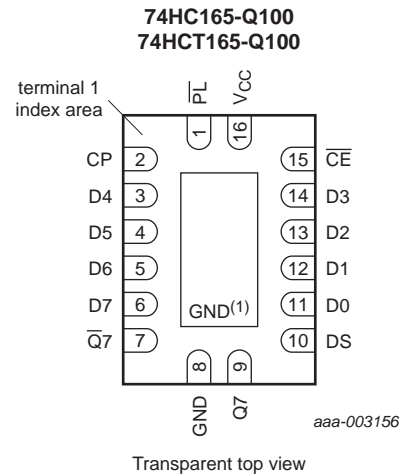


Fig 4. Pin configuration SO16 and TSSOP16



- (1) This is not a supply pin. The substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However, if it is soldered, the solder land should remain floating or be connected to GND.

Fig 5. Pin configuration DHVQFN16

6.2 Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|------------------------|----------------------------|--|
| $\overline{\text{PL}}$ | 1 | asynchronous parallel load input (active LOW) |
| CP | 2 | clock input (LOW-to-HIGH edge-triggered) |
| $\overline{\text{Q7}}$ | 7 | complementary output from the last stage |
| GND | 8 | ground (0 V) |
| Q7 | 9 | serial output from the last stage |
| DS | 10 | serial data input |
| D0 to D7 | 11, 12, 13, 14, 3, 4, 5, 6 | parallel data inputs (also referred to as D _n) |
| $\overline{\text{CE}}$ | 15 | clock enable input (active LOW) |
| V _{CC} | 16 | positive supply voltage |

7. Functional description

Table 3. Function table^[1]

| Operating modes | Inputs | | | | | Qn registers | | Outputs | |
|-------------------|------------------------|------------------------|----|----|----------|--------------|----------|---------|------------------------|
| | $\overline{\text{PL}}$ | $\overline{\text{CE}}$ | CP | DS | D0 to D7 | Q0 | Q1 to q6 | Q7 | $\overline{\text{Q7}}$ |
| parallel load | L | X | X | X | L | L | L to L | L | H |
| | L | X | X | X | H | H | H to H | H | L |
| serial shift | H | L | ↑ | l | X | L | q0 to q5 | q6 | $\overline{\text{q6}}$ |
| | H | L | ↑ | h | X | H | q0 to q5 | q6 | $\overline{\text{q6}}$ |
| | H | ↑ | L | l | X | L | q0 to q5 | q6 | $\overline{\text{q6}}$ |
| | H | ↑ | L | h | X | H | q0 to q5 | q6 | $\overline{\text{q6}}$ |
| hold "do nothing" | H | H | X | X | X | q0 | q1 to q6 | q7 | $\overline{\text{q7}}$ |
| | H | X | H | X | X | q0 | q1 to q6 | q7 | $\overline{\text{q7}}$ |

- [1] H = HIGH voltage level;
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;
 L = LOW voltage level;
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;
 q = state of the referenced output one set-up time prior to the LOW-to-HIGH clock transition;
 X = don't care;
 ↑ = LOW-to-HIGH clock transition.

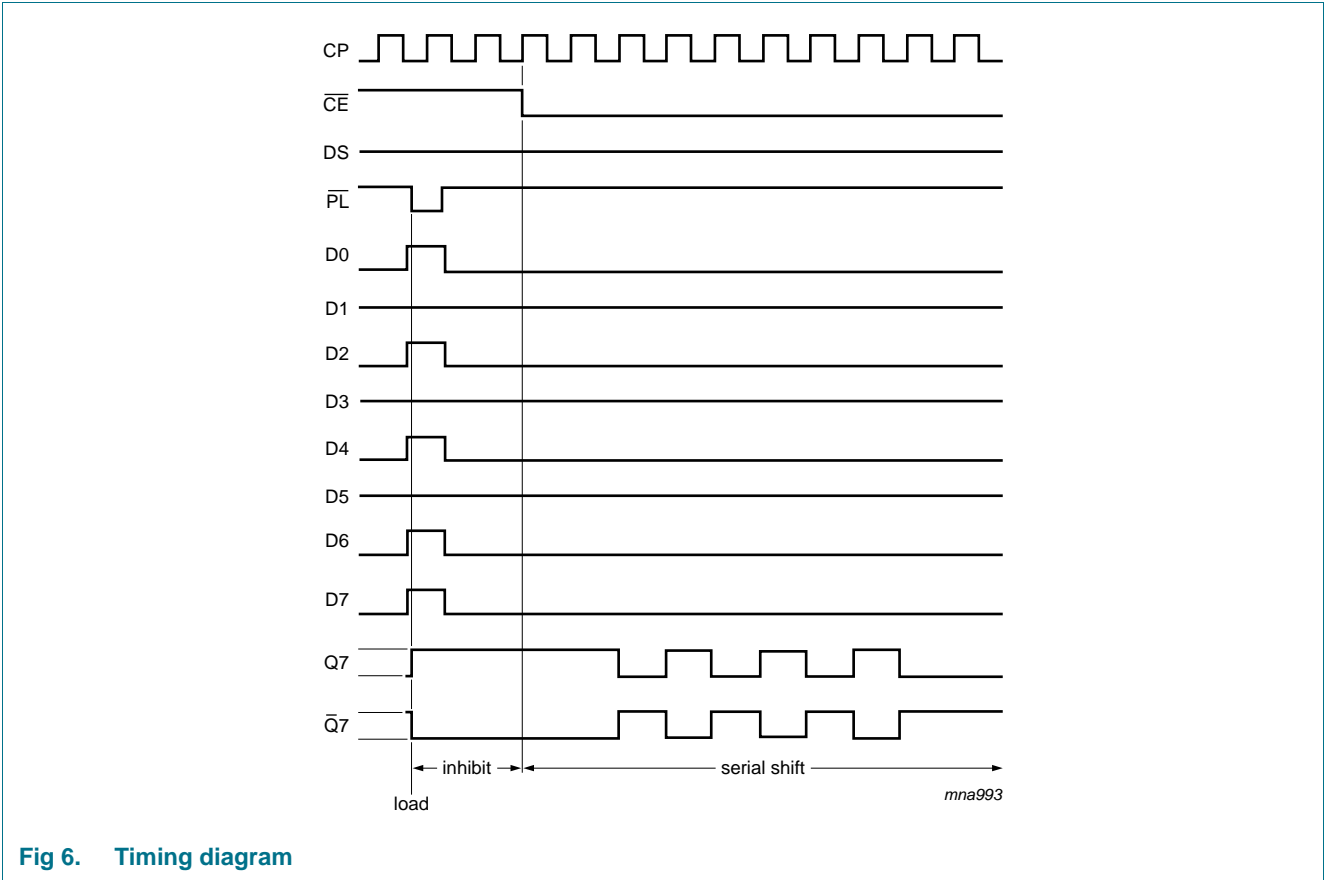


Fig 6. Timing diagram

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V)

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-------------------------|--|-------|------|------|
| V_{CC} | supply voltage | | -0.5 | +7 | V |
| I_{IK} | input clamping current | $V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$ | [1] - | ±20 | mA |
| I_{OK} | output clamping current | $V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$ | [1] - | ±20 | mA |
| I_O | output current | $-0.5\text{ V} < V_O < V_{CC} + 0.5\text{ V}$ | - | ±25 | mA |
| I_{CC} | supply current | | - | 50 | mA |
| I_{GND} | ground current | | -50 | - | mA |
| T_{stg} | storage temperature | | -65 | +150 | °C |
| P_{tot} | total power dissipation | $T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$ | [2] - | 500 | mW |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

For TSSOP16 package: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

For DHVQFN16 package: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

| Symbol | Parameter | Conditions | 74HC165-Q100 | | | 74HCT165-Q100 | | | Unit |
|------------------|-------------------------------------|-------------------------|--------------|------|-----------------|---------------|------|-----------------|------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| V _{CC} | supply voltage | | 2.0 | 5.0 | 6.0 | 4.5 | 5.0 | 5.5 | V |
| V _I | input voltage | | 0 | - | V _{CC} | 0 | - | V _{CC} | V |
| V _O | output voltage | | 0 | - | V _{CC} | 0 | - | V _{CC} | V |
| T _{amb} | ambient temperature | | -40 | - | +125 | -40 | - | +125 | °C |
| Δt/ΔV | input transition rise and fall rate | V _{CC} = 2.0 V | - | - | 625 | - | - | - | ns/V |
| | | V _{CC} = 4.5 V | - | 1.67 | 139 | - | 1.67 | 139 | ns/V |
| | | V _{CC} = 6.0 V | - | - | 83 | - | - | - | ns/V |

10. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|---------------------|---------------------------|--|-------|------|------|------------------|------|-------------------|------|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| 74HC165-Q100 | | | | | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 2.0 V | 1.5 | 1.2 | - | 1.5 | - | 1.5 | - | V |
| | | V _{CC} = 4.5 V | 3.15 | 2.4 | - | 3.15 | - | 3.15 | - | V |
| | | V _{CC} = 6.0 V | 4.2 | 3.2 | - | 4.2 | - | 4.2 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 2.0 V | - | 0.8 | 0.5 | - | 0.5 | - | 0.5 | V |
| | | V _{CC} = 4.5 V | - | 2.1 | 1.35 | - | 1.35 | - | 1.35 | V |
| | | V _{CC} = 6.0 V | - | 2.8 | 1.8 | - | 1.8 | - | 1.8 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | | | |
| | | I _O = -20 μA; V _{CC} = 2.0 V | 1.9 | 2.0 | - | 1.9 | - | 1.9 | - | V |
| | | I _O = -20 μA; V _{CC} = 4.5 V | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | I _O = -20 μA; V _{CC} = 6.0 V | 5.9 | 6.0 | - | 5.9 | - | 5.9 | - | V |
| | | I _O = -4.0 mA; V _{CC} = 4.5 V | 3.98 | 4.32 | - | 3.84 | - | 3.7 | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | | | |
| | | I _O = 20 μA; V _{CC} = 2.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 20 μA; V _{CC} = 4.5 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 20 μA; V _{CC} = 6.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 4.0 mA; V _{CC} = 4.5 V | - | 0.15 | 0.26 | - | 0.33 | - | 0.4 | V |
| I _I | input leakage current | V _I = V _{CC} or GND; V _{CC} = 6.0 V | - | - | ±0.1 | - | ±1 | - | ±1 | μA |
| | | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V | - | - | 8.0 | - | 80 | - | 160 | μA |

Table 6. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|----------------------|---------------------------|--|-------|------|------|------------------|-------|-------------------|-------|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| C _I | input capacitance | | - | 3.5 | - | - | - | - | - | pF |
| 74HCT165-Q100 | | | | | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 4.5 V to 5.5 V | 2.0 | 1.6 | - | 2.0 | - | 2.0 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 4.5 V to 5.5 V | - | 1.2 | 0.8 | - | 0.8 | - | 0.8 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V | | | | | | | | |
| | | I _O = -20 µA | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | I _O = -4.0 mA | 3.98 | 4.32 | - | 3.84 | - | 3.7 | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V | | | | | | | | |
| | | I _O = 20 µA; V _{CC} = 4.5 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 5.2 mA; V _{CC} = 6.0 V | - | 0.16 | 0.26 | - | 0.33 | - | 0.4 | V |
| I _I | input leakage current | V _I = V _{CC} or GND; V _{CC} = 6.0 V | - | - | ±0.1 | - | ±1 | - | ±1 | µA |
| I _{CC} | supply current | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V | - | - | 8.0 | - | 80 | - | 160 | µA |
| ΔI _{CC} | additional supply current | per input pin; V _I = V _{CC} - 2.1 V; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V | | | | | | | | |
| | | Dn and DS inputs | - | 35 | 126 | - | 157.5 | - | 171.5 | µA |
| | | CP \overline{CE} , and \overline{PL} inputs | - | 65 | 234 | - | 292.5 | - | 318.5 | µA |
| C _I | input capacitance | | - | 3.5 | - | - | - | - | - | pF |

11. Dynamic characteristics

Table 7. Dynamic characteristics

GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit, see [Figure 12](#)

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit | |
|---------------------------------|-------------------|--|---------------|---|-----|------------------|-----|-------------------|-----|------|---|
| | | | Min | Typ | Max | Min | Max | Min | Max | | |
| 74HC165-Q100 | | | | | | | | | | | |
| t_{pd} | propagation delay | CP or \overline{CE} to Q7, $\overline{Q7}$; see Figure 7 ^[1] | | | | | | | | | |
| | | $V_{CC} = 2.0$ V | - | 52 | 165 | - | 205 | - | 250 | ns | |
| | | $V_{CC} = 4.5$ V | - | 19 | 33 | - | 41 | - | 50 | ns | |
| | | $V_{CC} = 6.0$ V | - | 15 | 28 | - | 35 | - | 43 | ns | |
| | | $V_{CC} = 5.0$ V; $C_L = 15$ pF | - | 16 | - | - | - | - | - | ns | |
| | | \overline{PL} to Q7, $\overline{Q7}$; see Figure 8 | | | | | | | | | |
| | | $V_{CC} = 2.0$ V | - | 50 | 165 | - | 205 | - | 250 | ns | |
| | | $V_{CC} = 4.5$ V | - | 18 | 33 | - | 41 | - | 50 | ns | |
| | | $V_{CC} = 6.0$ V | - | 14 | 28 | - | 35 | - | 43 | ns | |
| | | $V_{CC} = 5.0$ V; $C_L = 15$ pF | - | 15 | - | - | - | - | - | ns | |
| | | D7 to Q7, $\overline{Q7}$; see Figure 9 | | | | | | | | | |
| | | $V_{CC} = 2.0$ V | - | 36 | 120 | - | 150 | - | 180 | ns | |
| | | $V_{CC} = 4.5$ V | - | 13 | 24 | - | 30 | - | 36 | ns | |
| | | $V_{CC} = 6.0$ V | - | 10 | 20 | - | 26 | - | 31 | ns | |
| $V_{CC} = 5.0$ V; $C_L = 15$ pF | - | 11 | - | - | - | - | - | ns | | | |
| t_t | transition time | Q7, $\overline{Q7}$ output; see Figure 7 ^[2] | | | | | | | | | |
| | | $V_{CC} = 2.0$ V | - | 19 | 75 | - | 95 | - | 110 | ns | |
| | | $V_{CC} = 4.5$ V | - | 7 | 15 | - | 19 | - | 22 | ns | |
| | | $V_{CC} = 6.0$ V | - | 6 | 13 | - | 16 | - | 19 | ns | |
| t_W | pulse width | CP input HIGH or LOW; see Figure 7 | | | | | | | | | |
| | | $V_{CC} = 2.0$ V | 80 | 17 | - | 100 | - | 120 | - | ns | |
| | | $V_{CC} = 4.5$ V | 16 | 6 | - | 20 | - | 24 | - | ns | |
| | | $V_{CC} = 6.0$ V | 14 | 5 | - | 17 | - | 20 | - | ns | |
| | | \overline{PL} input LOW; see Figure 8 | | | | | | | | | |
| | | $V_{CC} = 2.0$ V | 80 | 14 | - | 100 | - | 120 | - | ns | |
| | | $V_{CC} = 4.5$ V | 16 | 5 | - | 20 | - | 24 | - | ns | |
| | | $V_{CC} = 6.0$ V | 14 | 4 | - | 17 | - | 20 | - | ns | |
| | | t_{rec} | recovery time | \overline{PL} to CP, \overline{CE} ; see Figure 8 | | | | | | | |
| | | | | $V_{CC} = 2.0$ V | 100 | 22 | - | 125 | - | 150 | - |
| $V_{CC} = 4.5$ V | 20 | | | 8 | - | 25 | - | 30 | - | ns | |
| $V_{CC} = 6.0$ V | 17 | | | 6 | - | 21 | - | 26 | - | ns | |

Table 7. Dynamic characteristics ...continuedGND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit, see [Figure 12](#)

| Symbol | Parameter | Conditions | 25 °C | | | −40 °C to +85 °C | | −40 °C to +125 °C | | Unit | |
|-----------|-------------------------------|--|--|-----|-----|------------------|-----|-------------------|-----|------|----|
| | | | Min | Typ | Max | Min | Max | Min | Max | | |
| t_{su} | set-up time | DS to CP, \overline{CE} ; see Figure 10 | | | | | | | | | |
| | | $V_{CC} = 2.0$ V | 80 | 11 | - | 100 | - | 120 | - | ns | |
| | | $V_{CC} = 4.5$ V | 16 | 4 | - | 20 | - | 24 | - | ns | |
| | | | $V_{CC} = 6.0$ V | 14 | 3 | - | 17 | - | 20 | - | ns |
| | | | \overline{CE} to CP and CP to \overline{CE} ; see Figure 10 | | | | | | | | |
| | | | $V_{CC} = 2.0$ V | 80 | 17 | - | 100 | - | 120 | - | ns |
| | | | $V_{CC} = 4.5$ V | 16 | 6 | - | 20 | - | 24 | - | ns |
| | | | $V_{CC} = 6.0$ V | 14 | 5 | - | 17 | - | 20 | - | ns |
| | | | Dn to \overline{PL} ; see Figure 11 | | | | | | | | |
| | | | $V_{CC} = 2.0$ V | 80 | 22 | - | 100 | - | 120 | - | ns |
| | | | $V_{CC} = 4.5$ V | 16 | 8 | - | 20 | - | 24 | - | ns |
| | | | $V_{CC} = 6.0$ V | 14 | 6 | - | 17 | - | 20 | - | ns |
| t_h | hold time | DS to CP, \overline{CE} and Dn to \overline{PL} ; see Figure 10 | | | | | | | | | |
| | | $V_{CC} = 2.0$ V | 5 | 6 | - | 5 | - | 5 | - | ns | |
| | | $V_{CC} = 4.5$ V | 5 | 2 | - | 5 | - | 5 | - | ns | |
| | | | $V_{CC} = 6.0$ V | 5 | 2 | - | 5 | - | 5 | - | ns |
| | | | \overline{CE} to CP and CP to \overline{CE} ; see Figure 10 | | | | | | | | |
| | | | $V_{CC} = 2.0$ V | 5 | −17 | - | 5 | - | 5 | - | ns |
| | | | $V_{CC} = 4.5$ V | 5 | −6 | - | 5 | - | 5 | - | ns |
| | | $V_{CC} = 6.0$ V | 5 | −5 | - | 5 | - | 5 | - | ns | |
| f_{max} | maximum frequency | CP input; see Figure 7 | | | | | | | | | |
| | | $V_{CC} = 2.0$ V | 6 | 17 | - | 5 | - | 4 | - | MHz | |
| | | $V_{CC} = 4.5$ V | 30 | 51 | - | 24 | - | 20 | - | MHz | |
| | | $V_{CC} = 6.0$ V | 35 | 61 | - | 28 | - | 24 | - | MHz | |
| | | $V_{CC} = 5.0$ V; $C_L = 15$ pF | - | 56 | - | - | - | - | - | MHz | |
| C_{PD} | power dissipation capacitance | per package; $V_I = \text{GND to } V_{CC}$ | 3 | - | 35 | - | - | - | - | pF | |

Table 7. Dynamic characteristics ...continuedGND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit, see [Figure 12](#)

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|---------------------------------|-------------------|--|-------|-----|-----|------------------|-----|-------------------|-----|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| 74HCT165-Q100 | | | | | | | | | | |
| t_{pd} | propagation delay | \overline{CE} , CP to Q7, $\overline{Q7}$; see Figure 7 [1] | - | 17 | 34 | - | 43 | - | 51 | ns |
| | | $V_{CC} = 4.5$ V | - | 17 | 34 | - | 43 | - | 51 | ns |
| | | $V_{CC} = 5.0$ V; $C_L = 15$ pF | - | 14 | - | - | - | - | - | ns |
| | | \overline{PL} to Q7, $\overline{Q7}$; see Figure 8 | - | 20 | 40 | - | 50 | - | 60 | ns |
| | | $V_{CC} = 4.5$ V | - | 20 | 40 | - | 50 | - | 60 | ns |
| | | $V_{CC} = 5.0$ V; $C_L = 15$ pF | - | 17 | - | - | - | - | - | ns |
| | | D7 to Q7, $\overline{Q7}$; see Figure 9 | - | 14 | 28 | - | 35 | - | 42 | ns |
| $V_{CC} = 4.5$ V | - | 14 | 28 | - | 35 | - | 42 | ns | | |
| $V_{CC} = 5.0$ V; $C_L = 15$ pF | - | 11 | - | - | - | - | - | ns | | |
| t_t | transition time | Q7, $\overline{Q7}$ output; see Figure 7 [2] | - | 7 | 15 | - | 19 | - | 22 | ns |
| | | $V_{CC} = 4.5$ V | - | 7 | 15 | - | 19 | - | 22 | ns |
| t_W | pulse width | CP input; see Figure 7 | 16 | 6 | - | 20 | - | 24 | - | ns |
| | | $V_{CC} = 4.5$ V | 16 | 6 | - | 20 | - | 24 | - | ns |
| | | \overline{PL} input; see Figure 8 | 20 | 9 | - | 25 | - | 30 | - | ns |
| $V_{CC} = 4.5$ V | 20 | 9 | - | 25 | - | 30 | - | ns | | |
| t_{rec} | recovery time | \overline{PL} to CP, \overline{CE} ; see Figure 8 | 20 | 8 | - | 25 | - | 30 | - | ns |
| | | $V_{CC} = 4.5$ V | 20 | 8 | - | 25 | - | 30 | - | ns |
| t_{su} | set-up time | DS to CP, \overline{CE} ; see Figure 10 | 20 | 2 | - | 25 | - | 30 | - | ns |
| | | $V_{CC} = 4.5$ V | 20 | 2 | - | 25 | - | 30 | - | ns |
| | | \overline{CE} to CP and CP to \overline{CE} ; see Figure 10 | 20 | 7 | - | 25 | - | 30 | - | ns |
| | | $V_{CC} = 4.5$ V | 20 | 7 | - | 25 | - | 30 | - | ns |
| | | Dn to \overline{PL} ; see Figure 11 | 20 | 10 | - | 25 | - | 30 | - | ns |
| $V_{CC} = 4.5$ V | 20 | 10 | - | 25 | - | 30 | - | ns | | |
| t_h | hold time | DS to CP, \overline{CE} and Dn to \overline{PL} ; see Figure 10 | 7 | -1 | - | 9 | - | 11 | - | ns |
| | | $V_{CC} = 4.5$ V | 7 | -1 | - | 9 | - | 11 | - | ns |
| | | \overline{CE} to CP and CP to \overline{CE} ; see Figure 10 | 0 | -7 | - | 0 | - | 0 | - | ns |
| | | $V_{CC} = 4.5$ V | 0 | -7 | - | 0 | - | 0 | - | ns |
| f_{max} | maximum frequency | CP input; see Figure 7 | 26 | 44 | - | 21 | - | 17 | - | MHz |
| | | $V_{CC} = 4.5$ V | 26 | 44 | - | 21 | - | 17 | - | MHz |
| | | $V_{CC} = 5.0$ V; $C_L = 15$ pF | - | 48 | - | - | - | - | - | MHz |

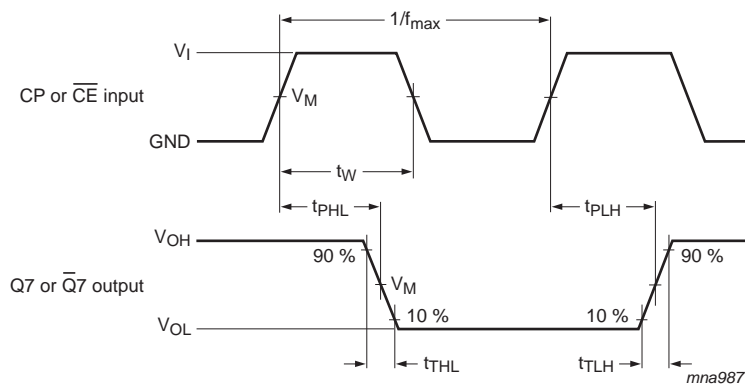
Table 7. Dynamic characteristics ...continued

GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit, see [Figure 12](#)

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|----------|-------------------------------|---|-------|-----|-----|------------------|-----|-------------------|-----|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| C_{PD} | power dissipation capacitance | per package; $V_I = GND$ to $V_{CC} - 1.5$ V | [3] | 35 | - | - | - | - | - | pF |

- [1] t_{pd} is the same as t_{PHL} and t_{PLH} .
- [2] t_t is the same as t_{THL} and t_{TLH} .
- [3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in V.

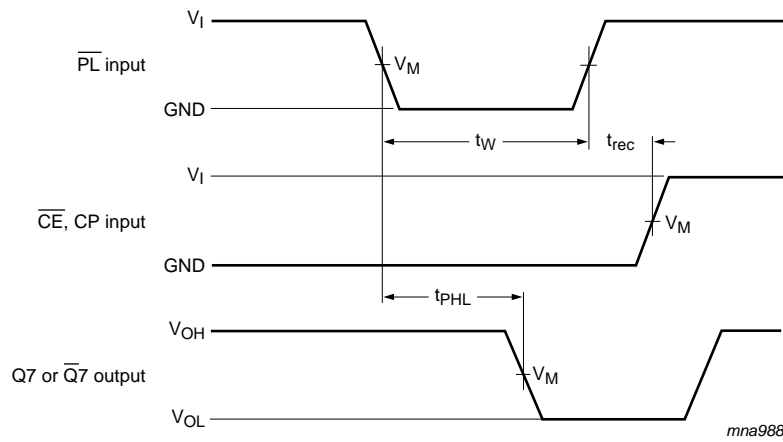
12. Waveforms



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

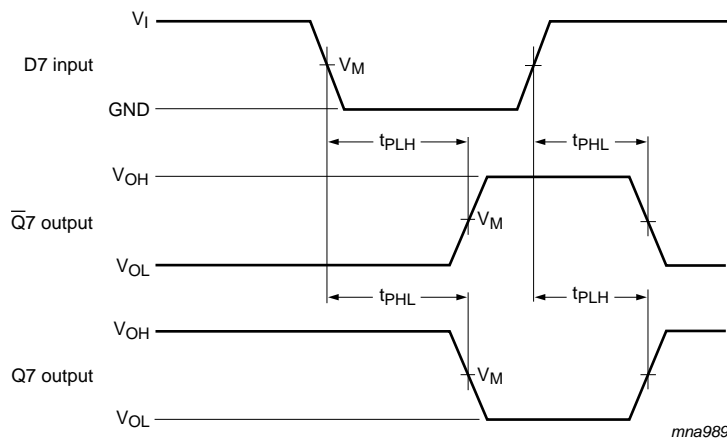
Fig 7. Clock (CP) or clock enable (CE) to output (Q7 or Q7) propagation delays, clock pulse width, maximum clock frequency and output transition times



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

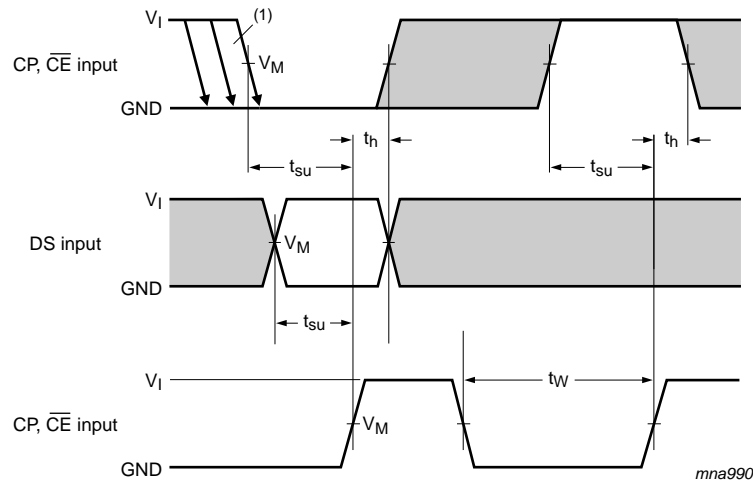
Fig 8. Parallel load (\overline{PL}) pulse width, parallel load to output (Q7 or $\overline{Q7}$) propagation delays, parallel load to clock (CP) and clock enable (\overline{CE}) recovery time



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 9. Data input (D7) to output (Q7 or $\overline{Q7}$) propagation delays when \overline{PL} is LOW

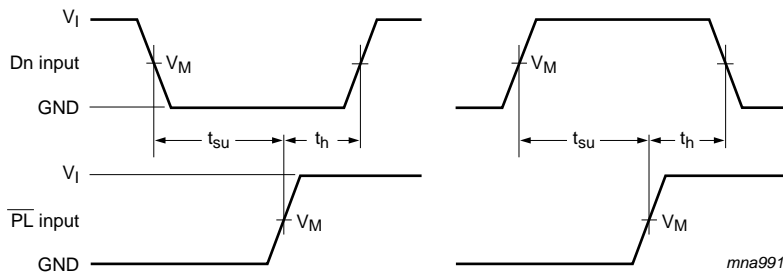


The shaded areas indicate when the input is permitted to change for predictable output performance. Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

(1) \overline{CE} may change only from HIGH-to-LOW while CP is LOW, see [Section 1](#).

Fig 10. Waveforms showing set-up and hold times



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 11. The set-up and hold times from the data inputs (Dn) to the parallel load input (\overline{PL})

Table 8. Measurement points

| Type | Input | | Output |
|---------------|----------|-------------|-------------|
| | V_I | V_M | V_M |
| 74HC165-Q100 | V_{CC} | $0.5V_{CC}$ | $0.5V_{CC}$ |
| 74HCT165-Q100 | 3 V | 1.3 V | 1.3 V |

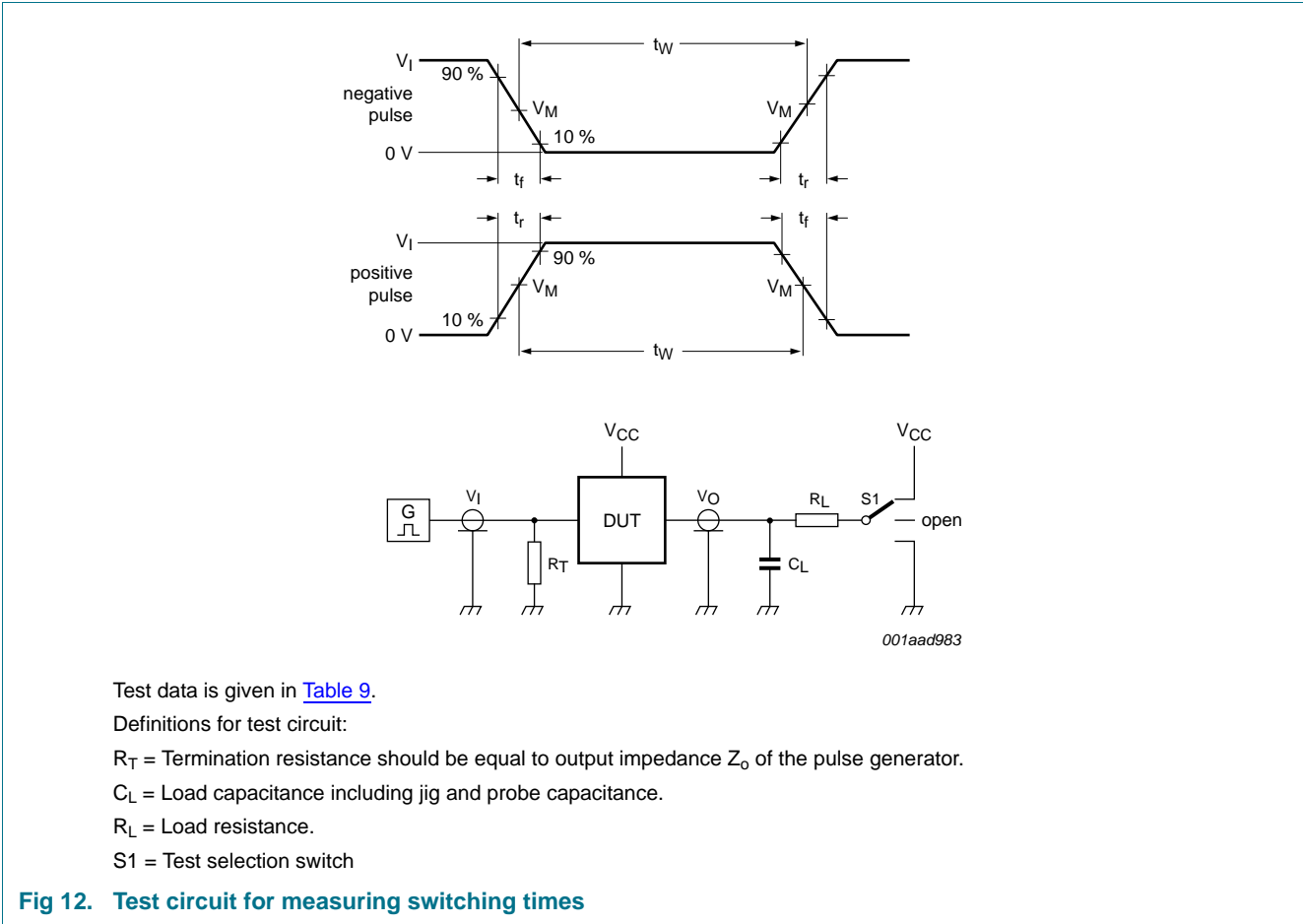


Table 9. Test data

| Type | Input | | Load | | | S1 position |
|---------------|----------|------------|--------------|--------------|--------------------|-------------|
| | V_I | t_r, t_f | C_L | R_L | t_{PHL}, t_{PLH} | |
| 74HC165-Q100 | V_{CC} | 6 ns | 15 pF, 50 pF | 1 k Ω | open | |
| 74HCT165-Q100 | 3 V | 6 ns | 15 pF, 50 pF | 1 k Ω | open | |

13. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

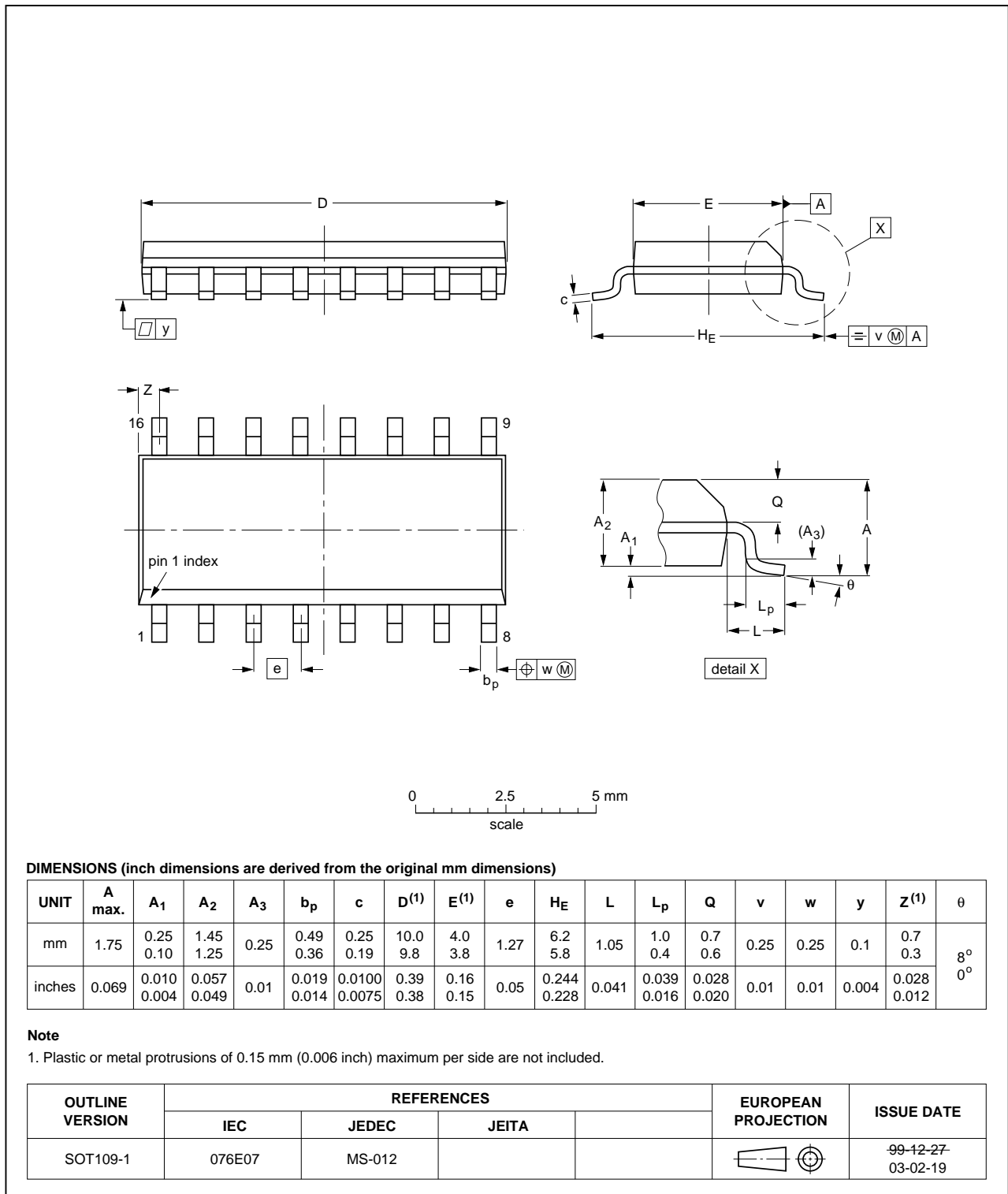


Fig 13. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

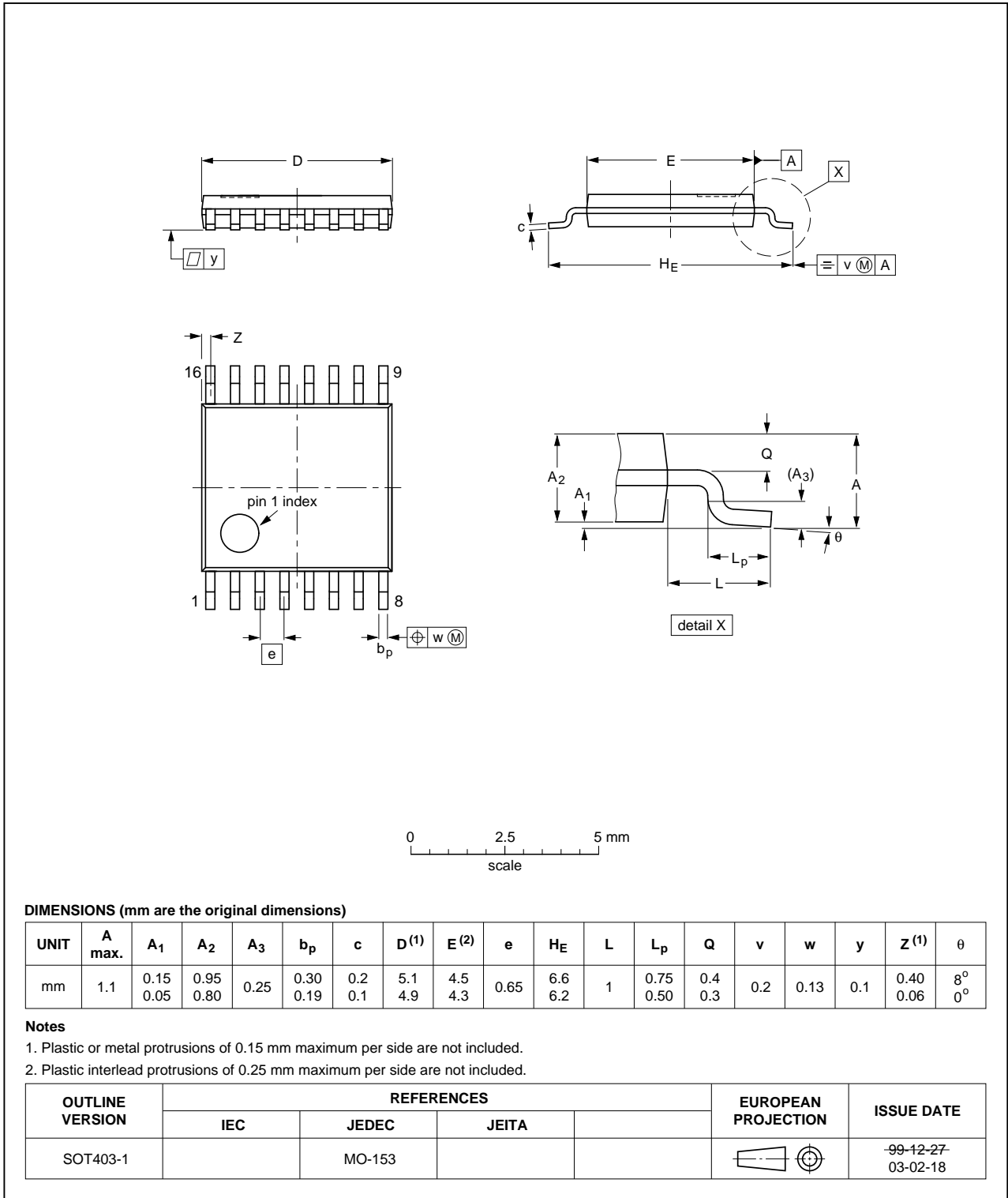


Fig 14. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

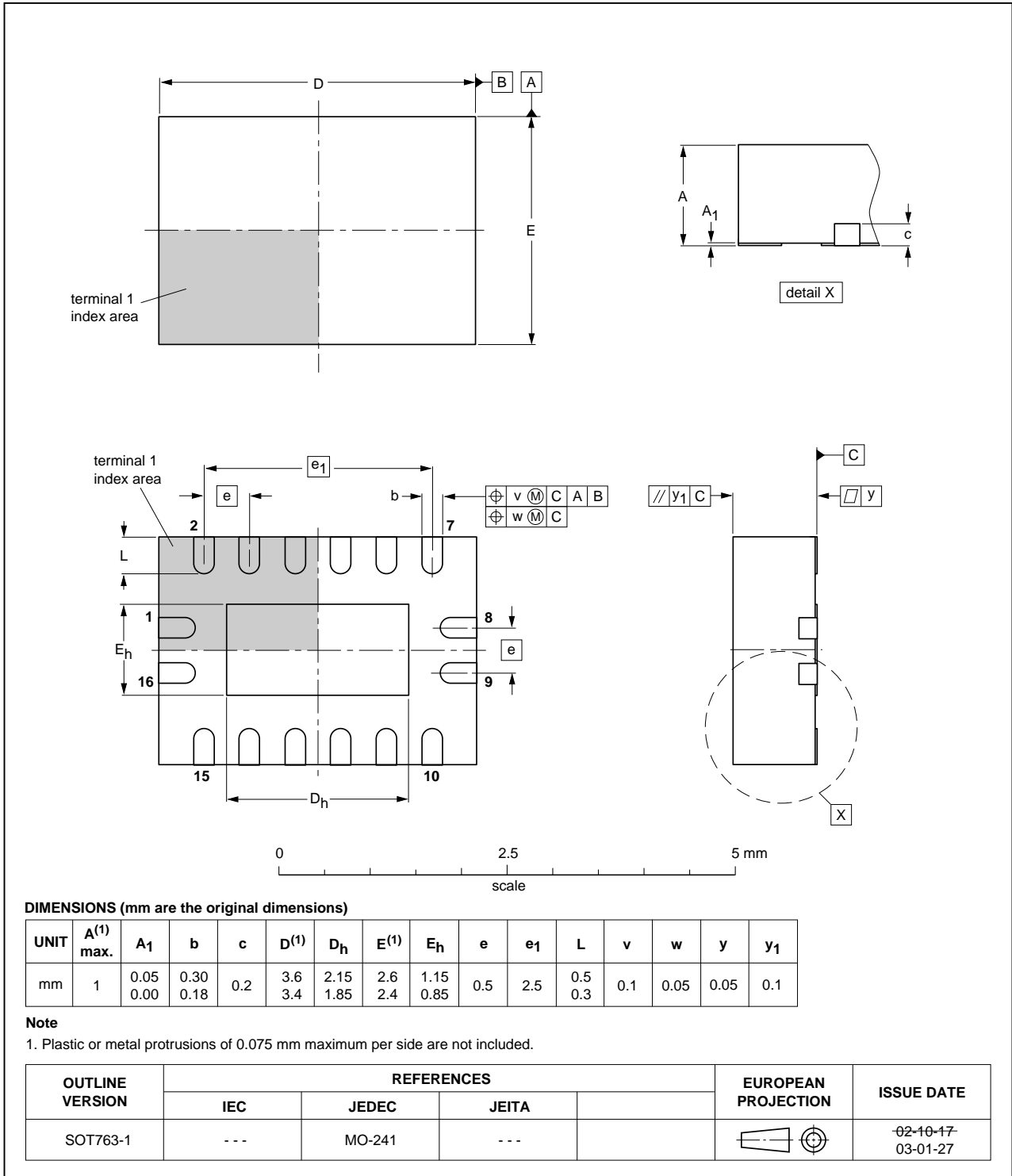


Fig 15. Package outline SOT763-1 (DHVQFN16)

14. Abbreviations

Table 10. Abbreviations

| Acronym | Description |
|---------|---|
| CMOS | Complementary Metal-Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |
| MIL | Military |

15. Revision history

Table 11. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|----------------------|--------------|--------------------|---------------|------------|
| 74HC_HCT165_Q100 v.1 | 20120717 | Product data sheet | - | - |

16. Legal information

16.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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