

74LVCH32373A

32-bit transparent D-type latch with 5 V tolerant inputs/outputs; 3-state

Rev. 5 — 17 December 2015

Product data sheet

1. General description

The 74LVCH32373A is a 32-bit transparent D-type latch featuring separate D-type inputs for each latch and 3-state outputs for bus-oriented applications. One latch enable input (nLE) and one output enable input ($\overline{\text{nOE}}$) are provided for each octal. Inputs can be driven from either 3.3 V or 5 V devices.

The device consists of 4 sections of eight D-type transparent latches with 3-state true outputs. When input nLE is HIGH, data at the nDn inputs enter the latches. In this condition, the latches are transparent, i.e. a latch output changes each time its corresponding D-input changes.

When input nLE is LOW, the latches store the information that was present at the D-inputs one set-up time preceding the HIGH-to-LOW transition of nLE. When input $\overline{\text{nOE}}$ is LOW, the contents of the eight latches are available at the outputs. When input $\overline{\text{nOE}}$ is HIGH, the outputs go to the high-impedance OFF-state. Operation of the $\overline{\text{nOE}}$ input does not affect the state of the latches.

The inputs can be driven from either 3.3 V or 5 V devices. In 3-state operation, outputs can handle 5 V. These features allow the use of these devices in a mixed 3.3 V and 5 V environment.

Bus hold on data inputs eliminates the need for external pull-up resistors to hold unused inputs.

2. Features and benefits

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- Multibyte flow-through standard pinout architecture
- Multiple low inductance supply pins for minimum noise and ground bounce
- Direct interface with TTL levels
- All data inputs have bus hold
- High impedance when $V_{CC} = 0$ V
- Complies with JEDEC standard:
 - ◆ JESD8-7A (1.65 V to 1.95 V)
 - ◆ JESD8-5A (2.3 V to 2.7 V)
 - ◆ JESD8-C/JESD36 (2.7 V to 3.6 V)



- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-B exceeds 200 V
 - ◆ CDM JESD22-C101E exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C
- Packaged in plastic fine-pitch ball grid array package

3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74LVCH32373AEC	-40 °C to +125 °C	LFPGA96	plastic low profile fine-pitch ball grid array package; 96 balls; body 13.5 × 5.5 × 1.05 mm	SOT536-1

4. Functional diagram

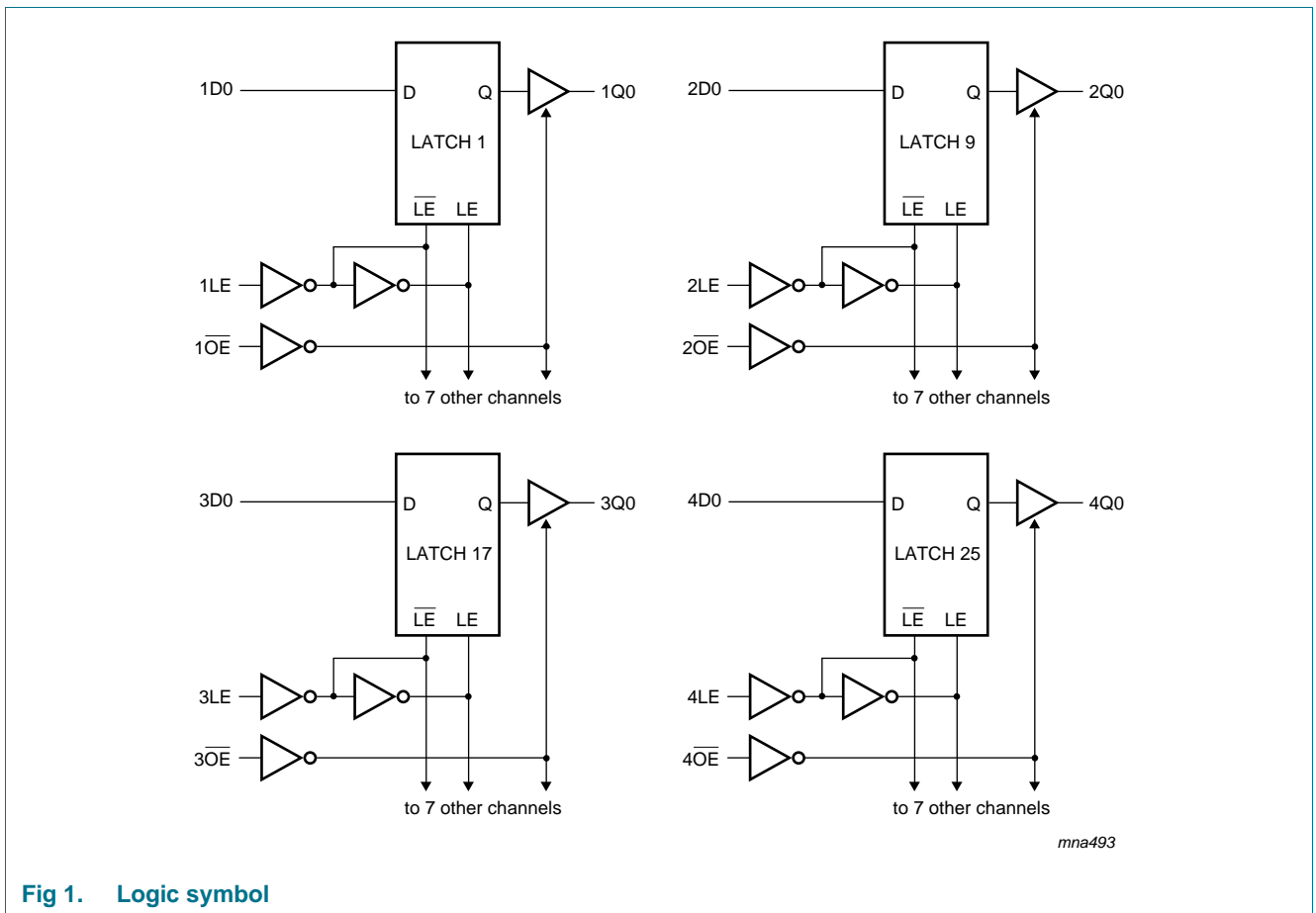


Fig 1. Logic symbol

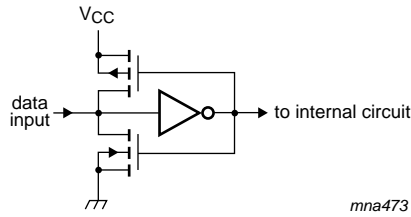


Fig 2. Bus hold circuit

5. Pinning information

5.1 Pinning

mna492

6	1D1	1D3	1D5	1D7	2D1	2D3	2D5	2D6	3D1	3D3	3D5	3D7	4D1	4D3	4D5	4D6
5	1D0	1D2	1D4	1D6	2D0	2D2	2D4	2D7	3D0	3D2	3D4	3D6	4D0	4D2	4D4	4D7
4	1LE	GND	V _{CC}	GND	GND	V _{CC}	GND	2LE	3LE	GND	V _{CC}	GND	GND	V _{CC}	GND	4LE
3	1OE	GND	V _{CC}	GND	GND	V _{CC}	GND	2OE	3OE	GND	V _{CC}	GND	GND	V _{CC}	GND	4OE
2	1Q0	1Q2	1Q4	1Q6	2Q0	2Q2	2Q4	2Q7	3Q0	3Q2	3Q4	3Q6	4Q0	4Q2	4Q4	4Q7
1	1Q1	1Q3	1Q5	1Q7	2Q1	2Q3	2Q5	2Q6	3Q1	3Q3	3Q5	3Q7	4Q1	4Q3	4Q5	4Q6
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T

Fig 3. Pin configuration

5.2 Pin description

Table 2. Pin description

Symbol	Ball	Description
\overline{nOE} (n = 1 to 4)	A3, H3, J3, T3	output enable input (active LOW)
nLE (n = 1 to 4)	A4, H4, J4, T4	latch enable input (active HIGH)
1D[0:7]	A5, A6, B5, B6, C5, C6, D5, D6	data input
2D[0:7]	E5, E6, F5, F6, G5, G6, H6, H5	data input
3D[0:7]	J5, J6, K5, K6, L5, L6, M5, M6	data input
4D[0:7]	N5, N6, P5, P6, R5, R6, T6, T5	data input
1Q[0:7]	A2, A1, B2, B1, C2, C1, D2, D1	data output
2Q[0:7]	E2, E1, F2, F1, G2, G1, H1, H2	data output
3Q[0:7]	J2, J1, K2, K1, L2, L1, M2, M1	data output
4Q[0:7]	N2, N1, P2, P1, R2, R1, T1, T2	data output
GND	B3, B4, D3, D4, E3, E4, G3, G4, K3, K4, M3, M4, N3, N4, R3, R4	ground (0 V)
V _{CC}	C3, C4, F3, F4, L3, L4, P3, P4	supply voltage

6. Functional description

Table 3. Function table^[1]

Operating modes	Inputs			Internal latch	Output nQn
	nOE	nLE	nDn		
Enable and read register (transparent mode)	L	H	L	L	L
	L	H	H	H	H
Latch and read register	L	L	l	L	L
	L	L	h	H	H
Latch register and disable outputs	H	L	l	L	Z
	H	L	h	H	Z

- [1] H = HIGH voltage level;
 h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition;
 L = LOW voltage level;
 l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition;
 Z = High impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V	-50	-	mA
V_I	input voltage		[1] -0.5	+6.5	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	±50	mA
V_O	output voltage	output HIGH or LOW state	[2] -0.5	$V_{CC} + 0.5$	V
		output 3-state	[2] -0.5	+6.5	V
I_O	output current	$V_O = 0$ V to V_{CC}	-	±50	mA
I_{CC}	supply current		-	200	mA
I_{GND}	ground current		-200	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C	[3] -	1000	mW

- [1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.
 [2] The output voltage ratings may be exceeded if the output current ratings are observed.
 [3] Above 70 °C, the value of P_{tot} derates linearly with 1.8 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	supply voltage		1.65	-	3.6	V
		functional	1.2	-	3.6	V
V _I	input voltage		0	-	5.5	V
V _O	output voltage	output HIGH or LOW state	0	-	V _{CC}	V
		output 3-state	0	-	5.5	V
T _{amb}	ambient temperature	in free air	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 1.65 V to 2.7 V	-	-	20	ns/V
		V _{CC} = 2.7 V to 3.6 V	-	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 1.2 V	1.08	-	-	1.08	-	V
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}	-	-	0.65 × V _{CC}	-	V
		V _{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.2 V	-	-	0.12	-	0.12	V
		V _{CC} = 1.65 V to 1.95 V	-	-	0.35 × V _{CC}	-	0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = -100 μA; V _{CC} = 1.65 V to 3.6 V	V _{CC} - 0.2	-	-	V _{CC} - 0.3	-	V
		I _O = -4 mA; V _{CC} = 1.65 V	1.2	-	-	1.05	-	V
		I _O = -8 mA; V _{CC} = 2.3 V	1.8	-	-	1.65	-	V
		I _O = -12 mA; V _{CC} = 2.7 V	2.2	-	-	2.05	-	V
		I _O = -18 mA; V _{CC} = 3.0 V	2.4	-	-	2.25	-	V
		I _O = -24 mA; V _{CC} = 3.0 V	2.2	-	-	2.0	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = 100 μA; V _{CC} = 1.65 V to 3.6 V	-	-	0.2	-	0.3	V
		I _O = 4 mA; V _{CC} = 1.65 V	-	-	0.45	-	0.65	V
		I _O = 8 mA; V _{CC} = 2.3 V	-	-	0.6	-	0.8	V
		I _O = 12 mA; V _{CC} = 2.7 V	-	-	0.4	-	0.6	V
		I _O = 24 mA; V _{CC} = 3.0 V	-	-	0.55	-	0.8	V
I _I	input leakage current	V _{CC} = 3.6 V; V _I = 5.5 V or GND ^[2]	-	±0.1	±5	-	±20	μA

Table 6. Static characteristics ...continued

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _{CC} = 3.6 V; V _O = 5.5 V or GND ^[2]	-	±0.1	±5	-	±20	µA
I _{OFF}	power-off leakage current	V _{CC} = 0 V; V _I or V _O = 5.5 V	-	±0.1	±10	-	±20	µA
I _{CC}	supply current	V _{CC} = 3.6 V; V _I = V _{CC} or GND; I _O = 0 A	-	0.1	40	-	160	µA
ΔI _{CC}	additional supply current	per input pin; V _{CC} = 2.7 V to 3.6 V; V _I = V _{CC} - 0.6 V; I _O = 0 A	-	5	500	-	5000	µA
C _I	input capacitance	V _{CC} = 0 V to 3.6 V; V _I = GND to V _{CC}	-	5.0	-	-	-	pF
I _{BHL}	bus hold LOW current	V _{CC} = 1.65; V _I = 0.58 V ^{[3][4]}	10	-	-	10	-	µA
		V _{CC} = 2.3; V _I = 0.7 V	30	-	-	25	-	µA
		V _{CC} = 3.0; V _I = 0.8 V	75	-	-	60	-	µA
I _{BHH}	bus hold HIGH current	V _{CC} = 1.65; V _I = 1.07 V ^{[3][4]}	-10	-	-	-10	-	µA
		V _{CC} = 2.3; V _I = 1.7 V	-30	-	-	-25	-	µA
		V _{CC} = 3.0; V _I = 2.0 V	-75	-	-	-60	-	µA
I _{BHLO}	bus hold LOW overdrive current	V _{CC} = 1.95 V ^{[3][5]}	200	-	-	200	-	µA
		V _{CC} = 2.7 V	300	-	-	300	-	µA
		V _{CC} = 3.6 V	500	-	-	500	-	µA
I _{BHHO}	bus hold HIGH overdrive current	V _{CC} = 1.95 V ^{[3][5]}	-200	-	-	-200	-	µA
		V _{CC} = 2.7 V	-300	-	-	-300	-	µA
		V _{CC} = 3.6 V	-500	-	-	-500	-	µA

- [1] All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.
- [2] The bus hold circuit is switched off when V_I > V_{CC} allowing 5.5 V on the input pin.
- [3] Valid for data inputs only. Control inputs do not have a bus hold circuit.
- [4] The specified sustaining current at the data input holds the input below the specified V_I level.
- [5] The specified overdrive current at the data input forces the data input to the opposite logic input state.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 8](#).

Symbol	Parameter	Conditions	T _{amb} = -40 °C to +85 °C			-40 °C to +125 °C		Unit	
			Min	Typ ^[1]	Max	Min	Max		
t _{pd}	propagation delay	Dn to Qn; see Figure 4	[2]						
		V _{CC} = 1.2 V		-	12	-	-	-	ns
		V _{CC} = 1.65 V to 1.95 V		1.5	5.4	11.4	1.5	13.2	ns
		V _{CC} = 2.3 V to 2.7 V		1.0	2.9	5.7	1.0	6.6	ns
		V _{CC} = 2.7 V		1.5	2.9	4.9	1.5	6.5	ns
		V _{CC} = 3.0 V to 3.6 V		1.0	2.4	4.4	1.0	5.9	ns
		LE to Qn; see Figure 5							
		V _{CC} = 1.2 V		-	14	-	-	-	ns
		V _{CC} = 1.65 V to 1.95 V		2.0	6.4	12.4	2.0	14.4	ns
		V _{CC} = 2.3 V to 2.7 V		1.5	3.4	6.1	1.5	7.1	ns
		V _{CC} = 2.7 V		1.5	3.0	5.3	1.5	7.0	ns
V _{CC} = 3.0 V to 3.6 V		1.5	2.9	4.8	1.5	6.0	ns		
t _{en}	enable time	OE to Qn; see Figure 7	[2]						
		V _{CC} = 1.2 V		-	18	-	-	-	ns
		V _{CC} = 1.65 V to 1.95 V		1.5	5.5	12.4	1.5	14.3	ns
		V _{CC} = 2.3 V to 2.7 V		1.0	3.1	6.6	1.0	7.6	ns
		V _{CC} = 2.7 V		1.5	3.3	5.7	1.5	7.5	ns
		V _{CC} = 3.0 V to 3.6 V		1.0	2.5	4.9	1.0	6.5	ns
t _{dis}	disable time	OE to Qn; see Figure 7	[2]						
		V _{CC} = 1.2 V		-	11	-	-	-	ns
		V _{CC} = 1.65 V to 1.95 V		2.8	4.5	9.1	2.8	10.5	ns
		V _{CC} = 2.3 V to 2.7 V		1.0	2.5	5.1	1.0	6.0	ns
		V _{CC} = 2.7 V		1.5	3.3	6.3	1.5	8.0	ns
		V _{CC} = 3.0 V to 3.6 V		1.5	3.1	5.4	1.5	7.0	ns
t _w	pulse width	LE HIGH; see Figure 5							
		V _{CC} = 1.65 V to 1.95 V		5.0	-	-	5.0	-	ns
		V _{CC} = 2.3 V to 2.7 V		4.0	-	-	4.0	-	ns
		V _{CC} = 2.7 V		3.0	-	-	3.0	-	ns
		V _{CC} = 3.0 V to 3.6 V		3.0	2.0	-	3.0	-	ns
t _{su}	set-up time	Dn to LE; see Figure 6							
		V _{CC} = 1.65 V to 1.95 V		3.0	-	-	3.0	-	ns
		V _{CC} = 2.3 V to 2.7 V		2.5	-	-	2.5	-	ns
		V _{CC} = 2.7 V		2.0	-	-	2.0	-	ns
		V _{CC} = 3.0 V to 3.6 V		2.0	1.0	-	2.0	-	ns

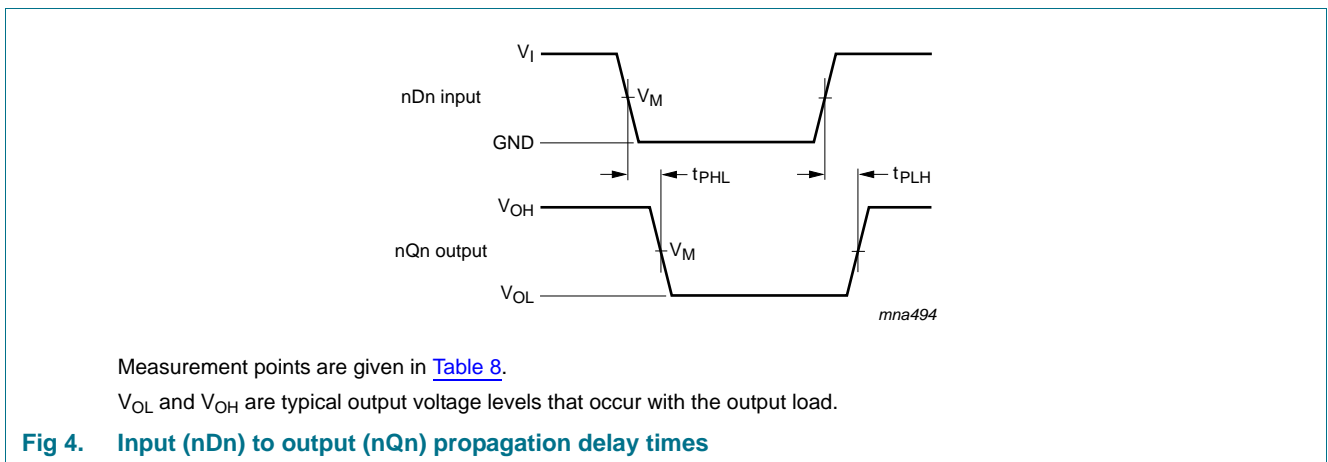
Table 7. Dynamic characteristics ...continued

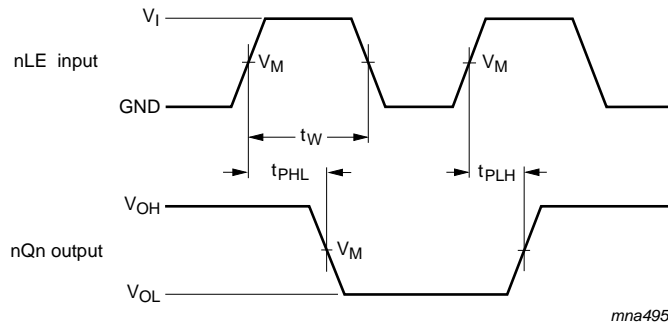
Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 8](#).

Symbol	Parameter	Conditions	T _{amb} = -40 °C to +85 °C			-40 °C to +125 °C		Unit	
			Min	Typ ^[1]	Max	Min	Max		
t _h	hold time	Dn to LE; see Figure 6							
		V _{CC} = 1.65 V to 1.95 V	2.5	-	-	2.5	-	ns	
		V _{CC} = 2.3 V to 2.7 V	2.0	-	-	2.0	-	ns	
		V _{CC} = 2.7 V	0.9	-	-	0.9	-	ns	
		V _{CC} = 3.0 V to 3.6 V	+0.9	-1.0	-	0.9	-	ns	
t _{sk(o)}	output skew time	V _{CC} = 3.0 V to 3.6 V	[3]	-	-	1.0	-	1.5	ns
C _{PD}	power dissipation capacitance	per input; V _I = GND to V _{CC}	[4]						
		V _{CC} = 1.65 V to 1.95 V	-	10.8	-	-	-	pF	
		V _{CC} = 2.3 V to 2.7 V	-	13.0	-	-	-	pF	
		V _{CC} = 3.0 V to 3.6 V	-	15.0	-	-	-	pF	

- [1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.2 V, 1.8 V, 2.5 V 2.7 V and 3.3 V respectively.
- [2] t_{pd} is the same as t_{PLH} and t_{PHL}.
t_{en} is the same as t_{PZL} and t_{PZH}.
t_{dis} is the same as t_{PLZ} and t_{PHZ}.
- [3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
- [4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
P_D = C_{PD} × V_{CC}² × f_i × N + Σ(C_L × V_{CC}² × f_o) where:
f_i = input frequency in MHz; f_o = output frequency in MHz
C_L = output load capacitance in pF
V_{CC} = supply voltage in Volts
N = number of inputs switching
Σ(C_L × V_{CC}² × f_o) = sum of the outputs

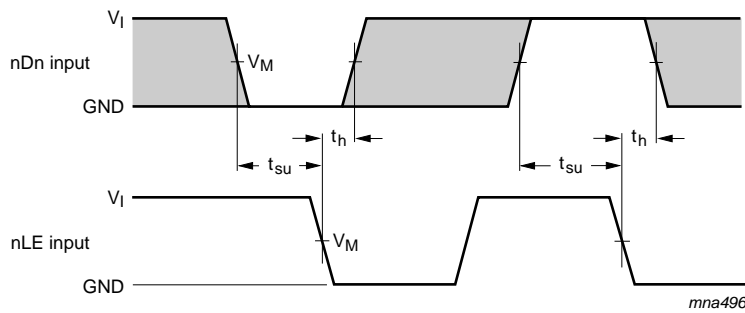
11. Waveforms





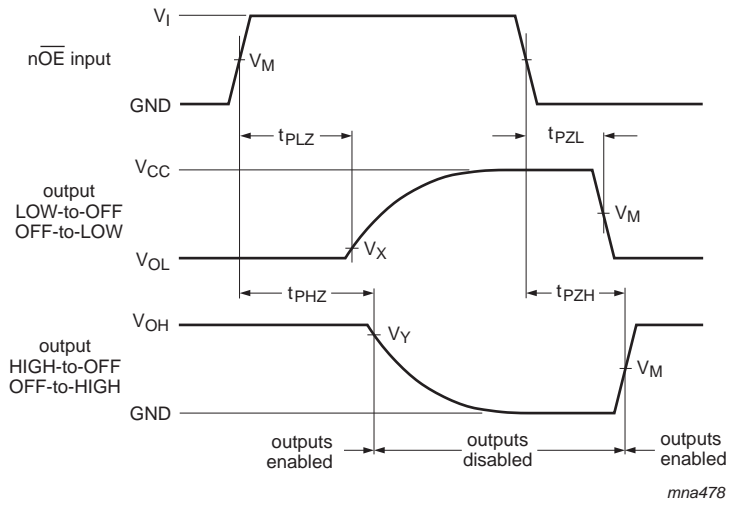
Measurement points are given in [Table 8](#).
 V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 5. Latch enable input (nLE) pulse width, the latch enable input to outputs (nQn) propagation delay times



Measurement points are given in [Table 8](#).
 V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.
 The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig 6. Set-up and hold times for inputs (nDn) to inputs (nLE)

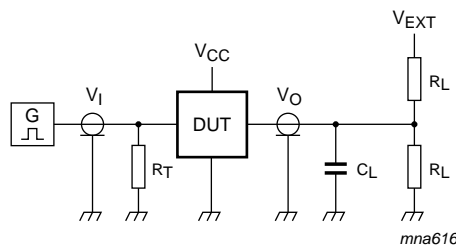


Measurement points are given in [Table 8](#).
 V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 7. 3-state output enable and disable times

Table 8. Measurement points

Supply voltage	Input		Output		
V_{CC}	V_I	V_M	V_M	V_X	V_Y
1.2 V	V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
1.65 V to 1.95 V	V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
2.3 V to 2.7 V	V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
2.7 V	2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$



Test data is given in [Table 9](#). Definitions for test circuit:
 R_L = Load resistance.
 C_L = Load capacitance including jig and probe capacitance
 R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig 8. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V _{EXT}		
	V _I	t _r , t _f	C _L	R _L	t _{PLH} , t _{PHL}	t _{PLZ} , t _{PZL}	t _{PHZ} , t _{PZH}
1.2 V	V _{CC}	≤ 2 ns	30 pF	1 kΩ	open	2 × V _{CC}	GND
1.65 V to 1.95 V	V _{CC}	≤ 2 ns	30 pF	1 kΩ	open	2 × V _{CC}	GND
2.3 V to 2.7 V	V _{CC}	≤ 2 ns	30 pF	500 Ω	open	2 × V _{CC}	GND
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	2 × V _{CC}	GND
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	2 × V _{CC}	GND

12. Package outline

LFBGA96: plastic low profile fine-pitch ball grid array package; 96 balls; body 13.5 x 5.5 x 1.05 mm SOT536-1

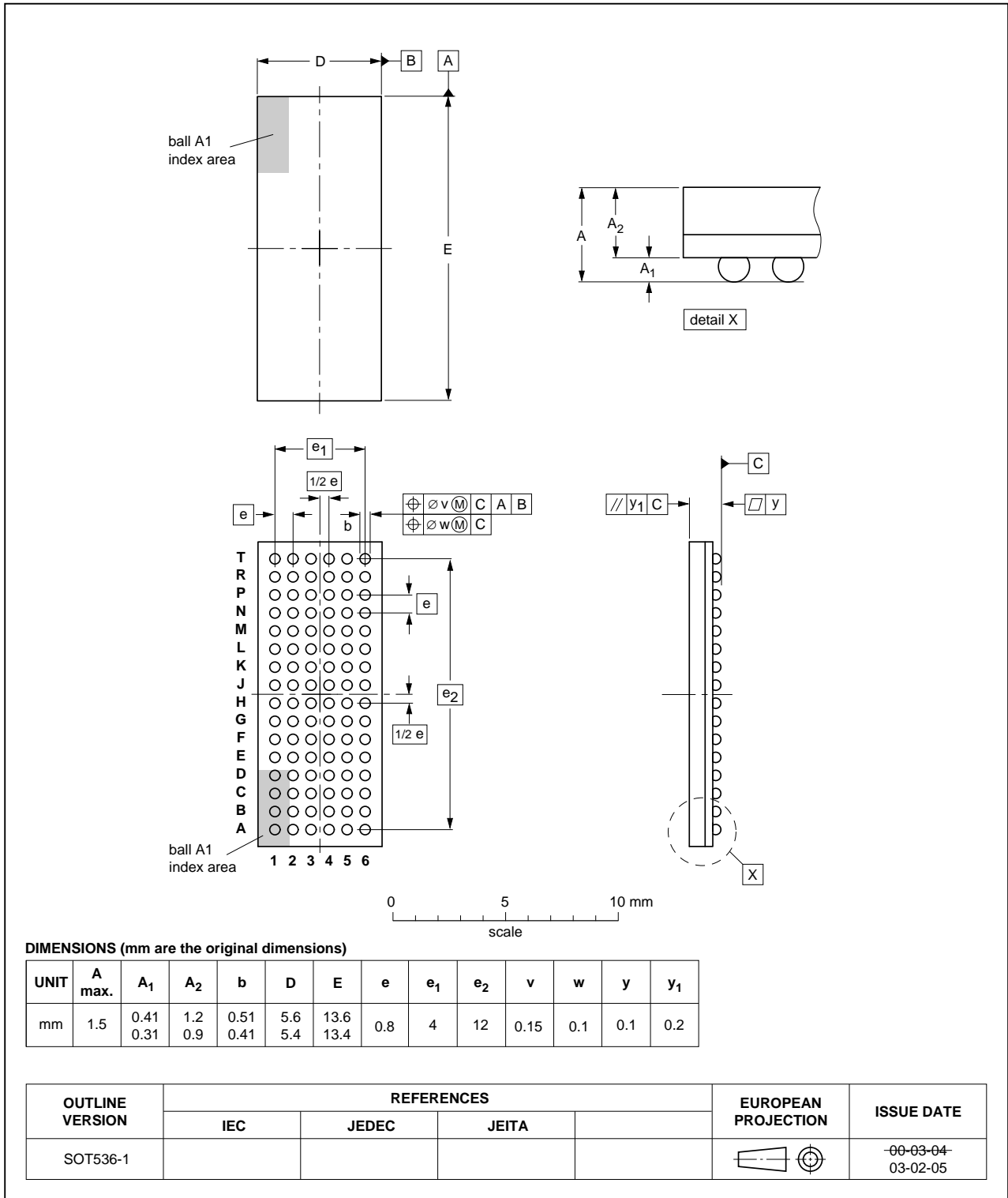


Fig 9. Package outline SOT536-1 (LFBGA96)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVCH32373A v.5	20151217	Product data sheet	-	74LVCH32373A v.4
Modifications:	<ul style="list-style-type: none"> • Table 1: Ordering info corrected (errata). 			
74LVCH32373A v.4	20130128	Product data sheet	-	74LVCH32373A v.3
Modifications:	<ul style="list-style-type: none"> • Features list corrected (errata). 			
74LVCH32373A v.3	20130122	Product data sheet	-	74LVCH32373A v.2
Modifications:	<ul style="list-style-type: none"> • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Table 4, Table 5, Table 6, Table 7, Table 8 and Table 9: values added for lower voltage ranges. 			
74LVCH32373A v.2	20040519	Product specification	-	74LVCH32373A v.1
74LVCH32373A v.1	19991124	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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