

DATA SHEET

BT134W series Triacs

Product specification

September 1997



Triacs

BT134W series

GENERAL DESCRIPTION

Glass passivated triacs in a plastic envelope suitable for surface mounting, intended for use in applications requiring high bidirectional transient and blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

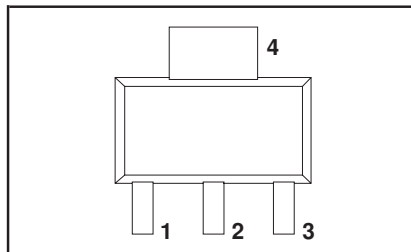
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	UNIT
V_{DRM}	Repetitive peak off-state voltages	500 500F 500G 500	600 600F 600G 600	800 800F 800G 800	V
$I_{T(RMS)}$	RMS on-state current	1	1	1	A
I_{TSM}	Non-repetitive peak on-state current	10	10	10	A

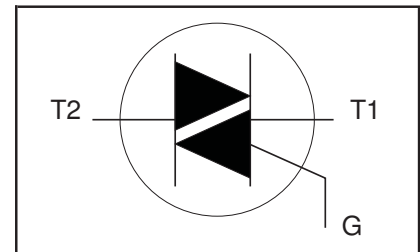
PINNING - SOT223

PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
tab	main terminal 2

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.			UNIT
				-500 500 ¹	-600 600 ¹	-800 800	
V_{DRM}	Repetitive peak off-state voltages		-				V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{sp} \leq 108\text{ }^\circ\text{C}$	-	1			A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_j = 25\text{ }^\circ\text{C}$ prior to surge $t = 20\text{ ms}$	-	10			A
I^2t	I^2t for fusing	$t = 16.7\text{ ms}$	-	11			A
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$t = 10\text{ ms}$ $I_{TM} = 1.5\text{ A}; I_G = 0.2\text{ A};$ $dI_G/dt = 0.2\text{ A}/\mu\text{s}$	-	0.5			A ² s
		T2+ G+	-	50			A/ μs
		T2+ G-	-	50			A/ μs
		T2- G-	-	50			A/ μs
		T2- G+	-	10			A/ μs
I_{GM}	Peak gate current		-	2			A
V_{GM}	Peak gate voltage		-	5			V
P_{GM}	Peak gate power		-	5			W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5			W
T_{stg}	Storage temperature		-40	150			$^\circ\text{C}$
T_j	Operating junction temperature		-	125			$^\circ\text{C}$

¹ Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 3 A/ μs .

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BT134W series

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-sp}$	Thermal resistance junction to solder point	full or half cycle	-	-	15	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	pcb mounted; minimum footprint pcb mounted; pad area as in fig:14	-	156 70	-	K/W K/W

STATIC CHARACTERISTICS

$T_j = 25\text{ °C}$ unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.			UNIT
I_{GT}	Gate trigger current	BT134W- $V_D = 12\text{ V}; I_T = 0.1\text{ A}$	-	-F	...G	
		T2+ G+	-	5	35	25	50	mA
		T2+ G-	-	8	35	25	50	mA
		T2- G-	-	11	35	25	50	mA
I_L	Latching current	$V_D = 12\text{ V}; I_{GT} = 0.1\text{ A}$	-	-	70	70	100	mA
		T2- G+	-	30	70	70	100	mA
		T2+ G+	-	7	20	20	30	mA
		T2+ G-	-	16	30	30	45	mA
I_H	Holding current	$V_D = 12\text{ V}; I_{GT} = 0.1\text{ A}$	-	-	5	15	30	mA
		T2- G+	-	7	30	30	45	mA
		T2- G-	-	5	20	20	30	mA
		T2+ G+	-	7	30	30	45	mA
V_T	On-state voltage	$I_T = 2\text{ A}$	-	1.2	1.50			V
V_{GT}	Gate trigger voltage	$V_D = 12\text{ V}; I_T = 0.1\text{ A}$	-	0.7	1.5			V
		$V_D = 400\text{ V}; I_T = 0.1\text{ A};$ $T_j = 125\text{ °C}$	0.25	0.4	-			V
I_D	Off-state leakage current	$V_D = V_{DRM(max)};$ $T_j = 125\text{ °C}$	-	0.1	0.5			mA

DYNAMIC CHARACTERISTICS

$T_j = 25\text{ °C}$ unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.			TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	BT134W- $V_{DM} = 67\% V_{DRM(max)};$ $T_j = 125\text{ °C};$ exponential waveform; gate open circuit	100	50	200	250	-	V/ μ s
dV_{com}/dt	Critical rate of change of commutating voltage	$V_{DM} = 400\text{ V}; T_j = 95\text{ °C};$ $I_{T(RMS)} = 1\text{ A};$ $dI_{com}/dt = 1.8\text{ A/ms};$ gate open circuit	-	-	10	50	-	V/ μ s
t_{gt}	Gate controlled turn-on time	$I_{TM} = 1.5\text{ A};$ $V_D = V_{DRM(max)};$ $I_G = 0.1\text{ A};$ $dI_G/dt = 5\text{ A}/\mu\text{s};$	-	-	-	2	-	μ s

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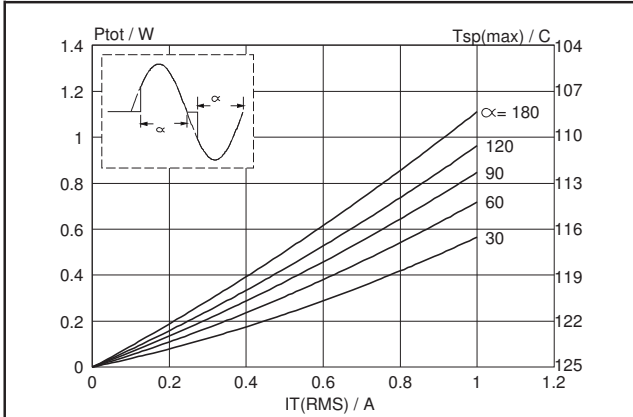


Fig.1. Maximum on-state dissipation, P_{tot} , versus rms on-state current, $I_{T(RMS)}$, where $\alpha =$ conduction angle.

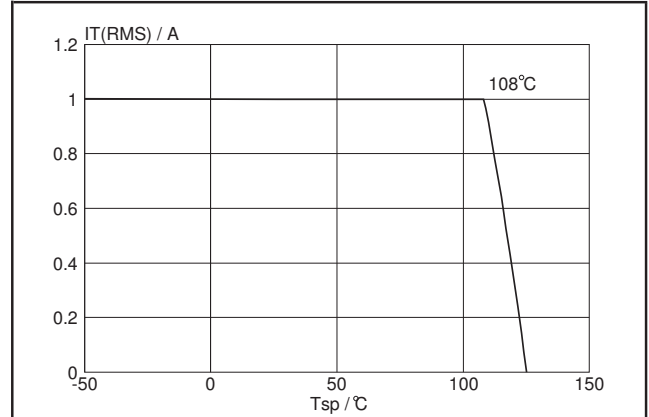


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus solder point temperature T_{sp} .

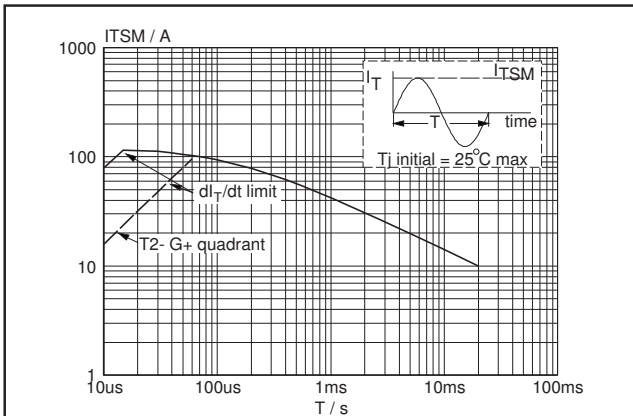


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM} , versus pulse width t_p , for sinusoidal currents, $t_p \leq 20ms$.

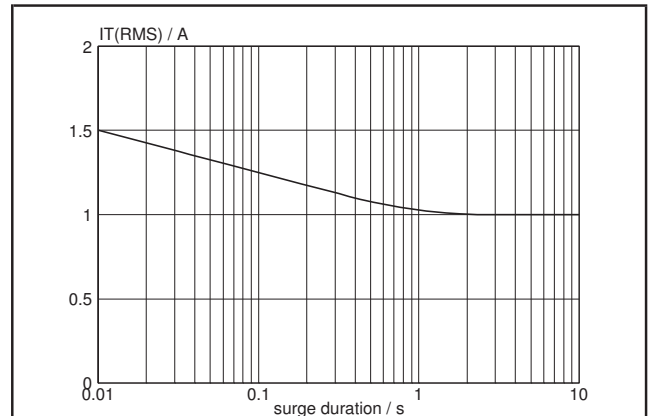


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, $f = 50 Hz$; $T_{sp} \leq 108^\circ C$.

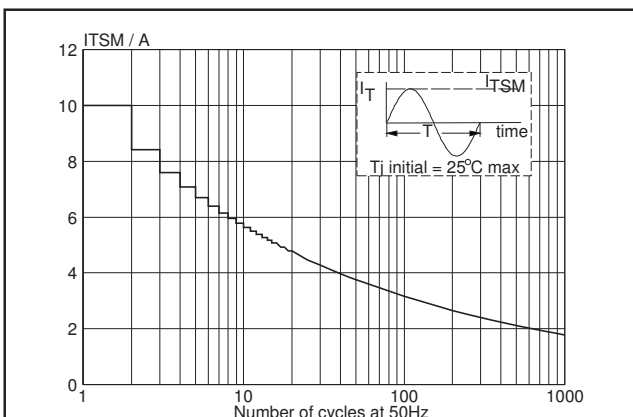


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM} , versus number of cycles, for sinusoidal currents, $f = 50 Hz$.

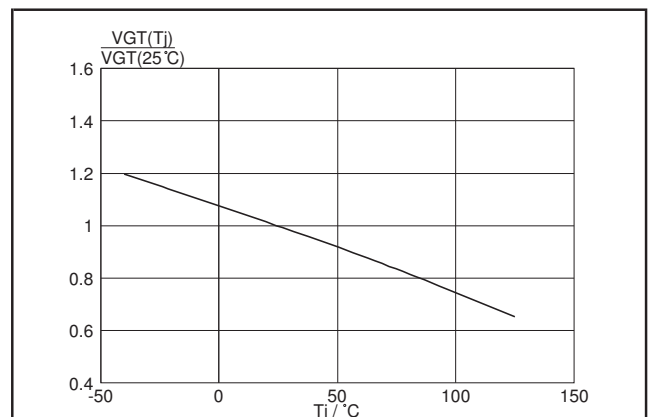
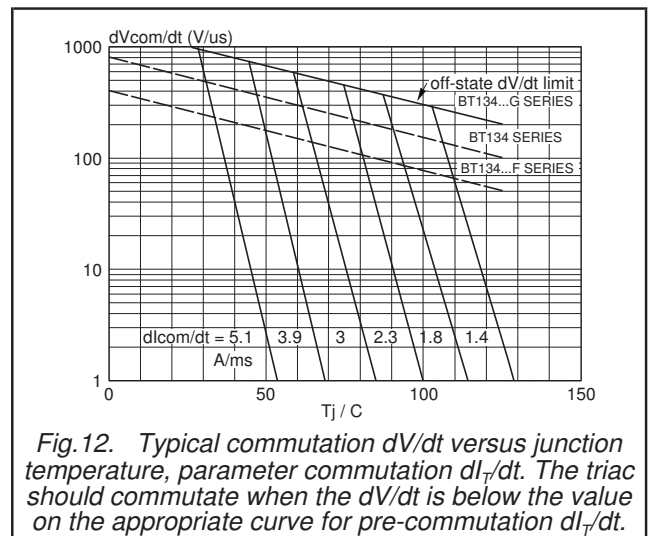
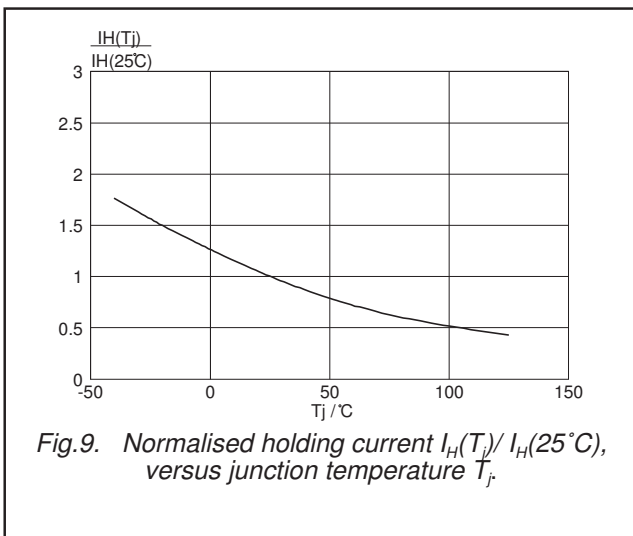
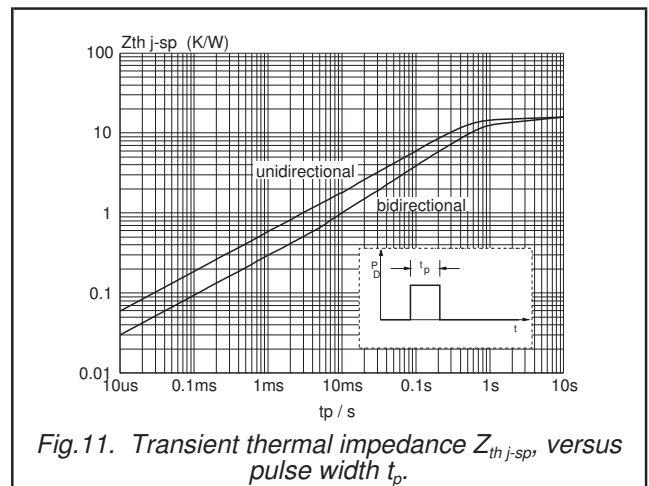
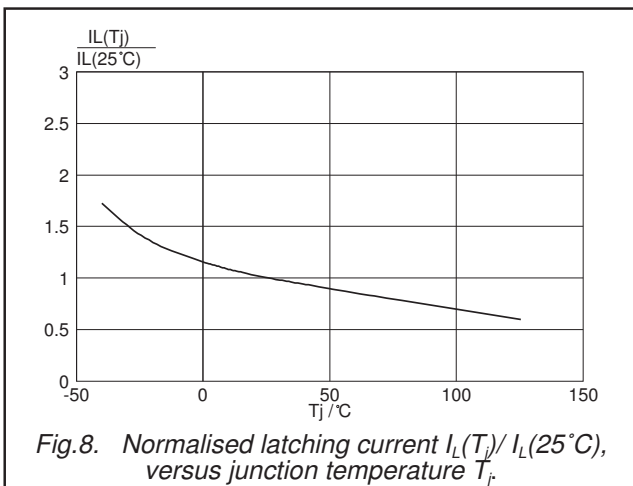
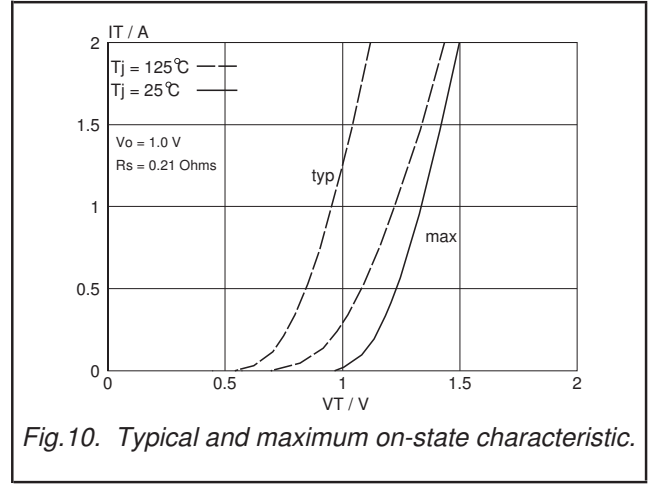
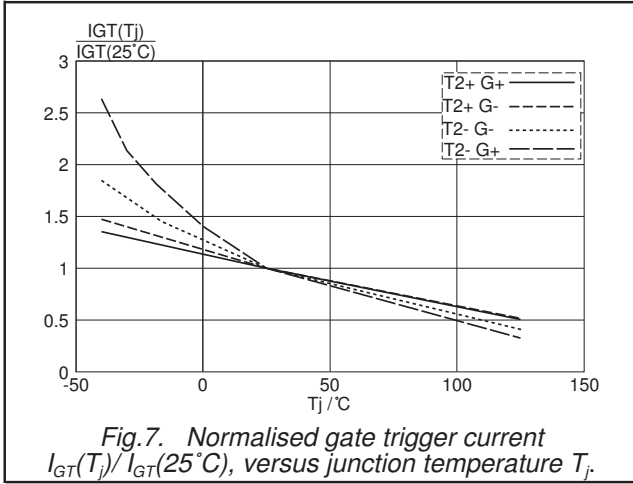


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j) / V_{GT}(25^\circ C)$, versus junction temperature T_j .

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BT134W series



MOUNTING INSTRUCTIONS

Dimensions in mm.

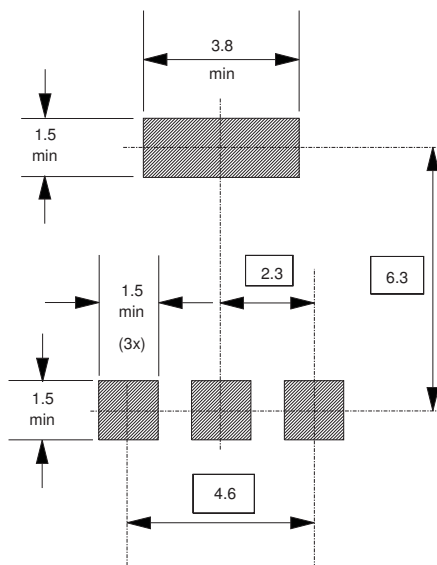


Fig.13. soldering pattern for surface mounting SOT223.

PRINTED CIRCUIT BOARD

Dimensions in mm.

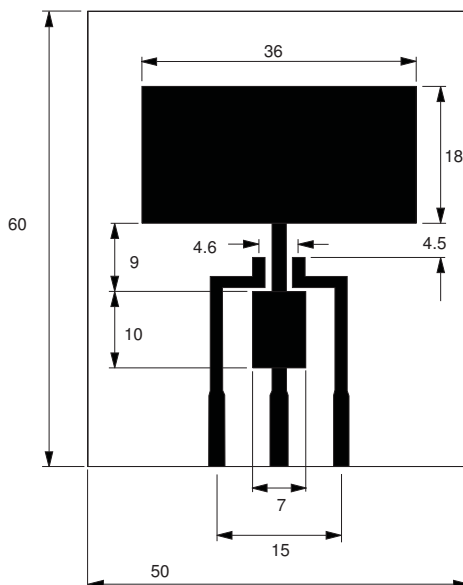


Fig.14. PCB for thermal resistance and power rating for SOT223.
PCB: FR4 epoxy glass (1.6 mm thick), copper laminate (35 μm thick).

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DATA SHEET STATUS

DOCUMENT STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾	DEFINITION
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Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

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