# HEF4046B

**Phase-locked loop**

**Rev. 5 — 18 November 2011**        **Product data sheet**

## 1. General description

The HEF4046B is a phase-locked loop circuit that consists of a linear Voltage Controlled Oscillator (VCO) and two different phase comparators with a common signal input amplifier and a common comparator input. A 7 V regulator (Zener) diode is provided for supply voltage regulation if necessary. For a functional description see Section 6.

It operates over a recommended $V_{DD}$ power supply range of 3 V to 15 V referenced to $V_{SS}$ (usually ground). Unused inputs must be connected to $V_{DD}$, $V_{SS}$, or another input.

## 2. Features and benefits

- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Specified from −40 °C to +85 °C
- Complies with JEDEC standard JESD 13-B

## 3. Ordering information

**Table 1.  Ordering information**
*All types operate from −40 ℃ to +85 ℃.*

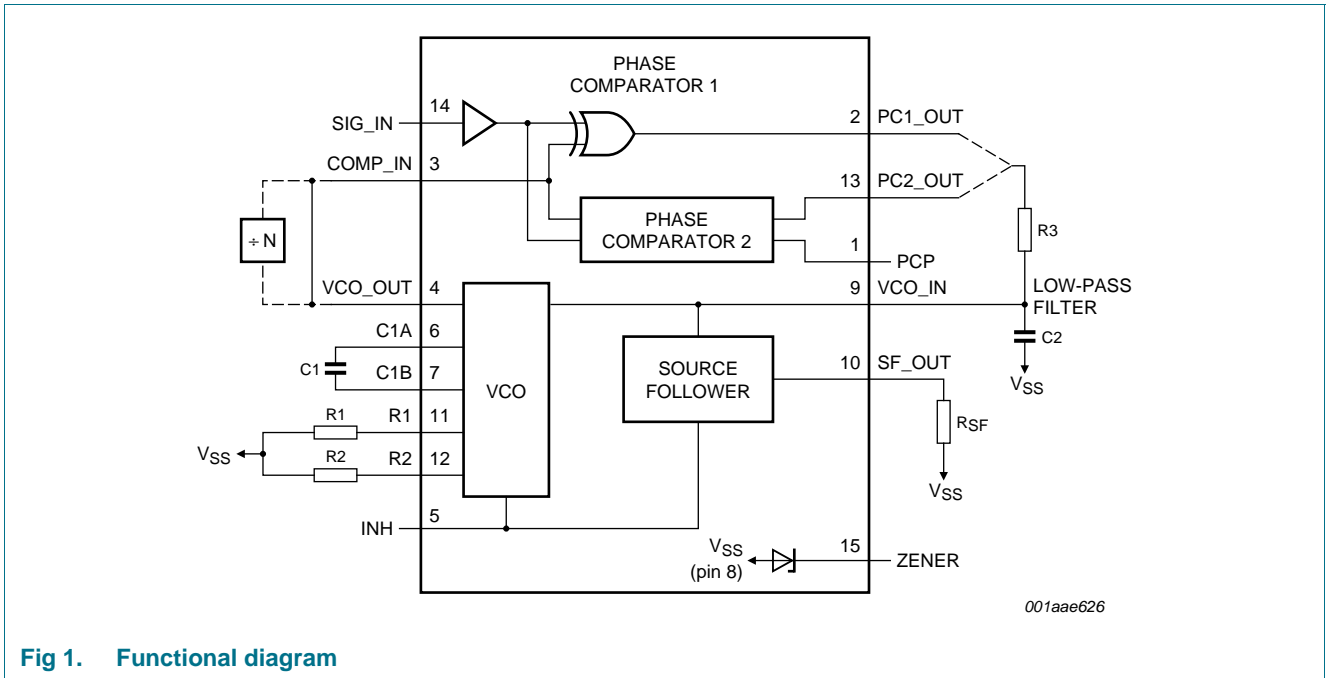| Type number | Package | | |
| --- | --- | --- | --- |
| | **Name** | **Description** | **Version** |
| HEF4046BP | DIP16 | plastic dual in-line package; 16 leads (300 mil) | SOT38-4 |
| HEF4046BT | SO16 | plastic small outline package; 16 leads; body width 3.9 mm | SOT109-1 |

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## 4. Functional diagram



**Fig 1.   Functional diagram**

## 5. Pinning information

### 5.1 Pinning



**Fig 2.   Pin configuration**

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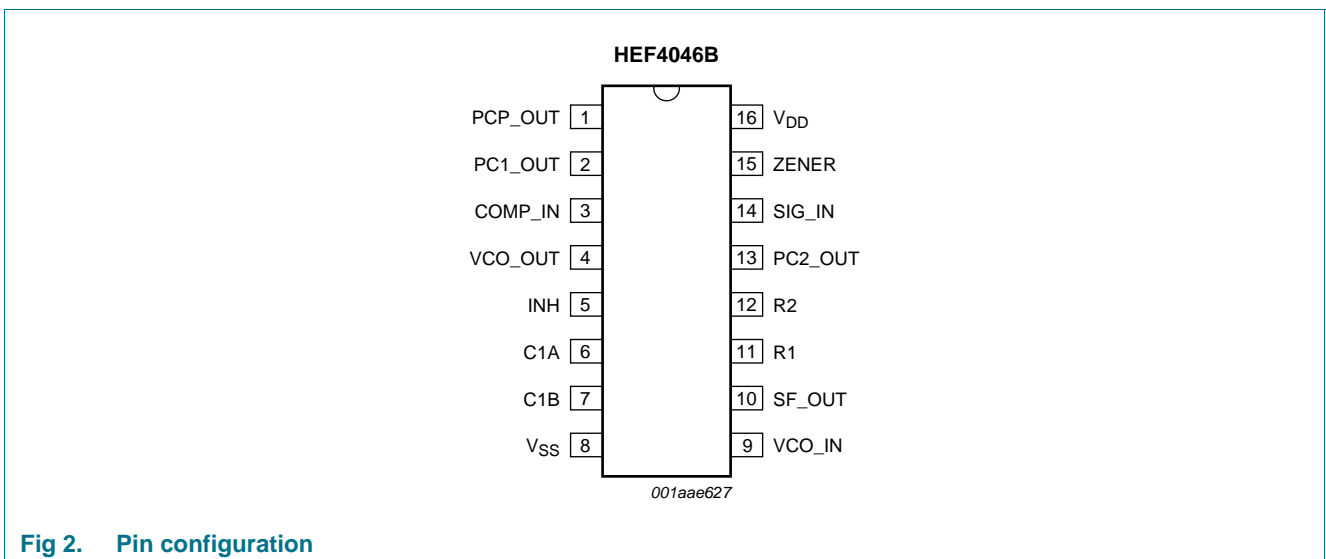
### 5.2 Pin description

**Table 2.    Pin description**

| Symbol | Pin | Description |
|--------|-----|-------------|
| PCP_OUT | 1 | phase comparator pulse output |
| PC1_OUT | 2 | phase comparator 1 output |
| COMP_IN | 3 | comparator input |
| VCO_OUT | 4 | VCO output |
| INH | 5 | inhibit input |
| C1A | 6 | capacitor C1 connection A |
| C1B | 7 | capacitor C1 connection B |
| $V_{SS}$ | 8 | ground supply voltage |
| VCO_IN | 9 | VCO input |
| SF_OUT | 10 | source-follower output |
| R1 | 11 | resistor R1 connection |
| R2 | 12 | resistor R2 connection |
| PC2_OUT | 13 | phase comparator 2 output |
| SIG_IN | 14 | signal input |
| ZENER | 15 | Zener diode input for regulated supply |
| $V_{DD}$ | 16 | supply voltage |

## 6.  Functional description

### 6.1  VCO control

The VCO requires an external capacitor (C1) and resistor (R1) with an optional resistor (R2). Resistor R1 and capacitor C1 determine the frequency range of the VCO, while resistor R2 enables the VCO to have a frequency off-set if required. The high input impedance of the VCO simplifies the design of low-pass filters; it permits the designer a wide choice of resistor/capacitor ranges. In order not to load the low-pass filter, a source-follower output of the VCO input voltage is provided at SF_OUT (pin 10). If this is used, a load resistor ($R_L$) should be connected from SF_OUT to $V_{SS}$; if unused, SF_OUT should be left open. The VCO output (pin 4) can either be connected directly to the comparator input COMP_IN (pin 3) or via a frequency divider. A LOW-level at the inhibit input INH_IN (pin 5) enables the VCO and the source follower, while a HIGH-level turns both off to minimize standby power consumption.
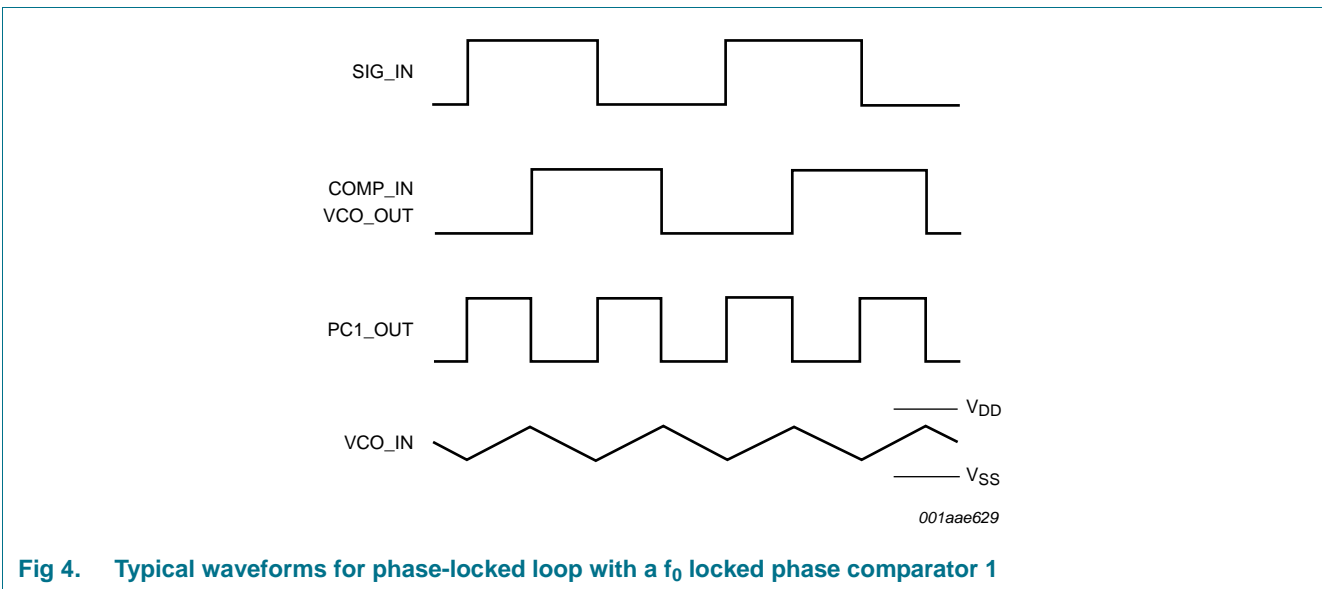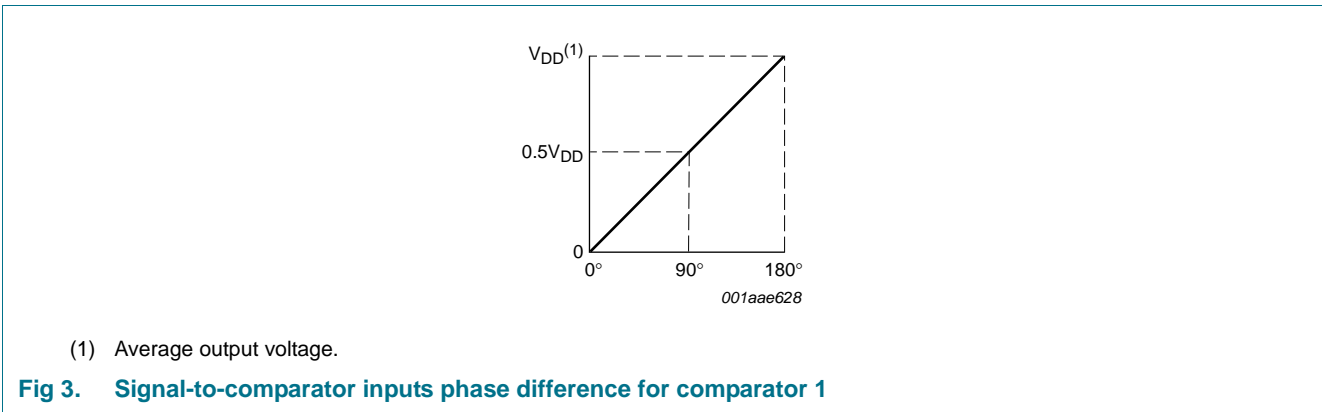
### 6.2  Phase comparators

The phase-comparator signal input SIG_IN (pin 14) can be direct-coupled, provided the signal swing is between the standard HE4000B family input logic levels. The signal must be capacitively coupled to the self-biasing amplifier at the signal input with smaller swings. Phase comparator 1 is an EXCLUSIVE-OR network. The signal and comparator input frequencies must have a 50 % duty factor to obtain the maximum lock range. The average output voltage of the phase comparator is equal to $0.5V_{DD}$ when there is no signal or noise at the signal input. The average voltage to the VCO input VCO_IN is supplied by the low-pass filter connected to the output of phase comparator 1. This also causes the VCO to oscillate at the center frequency ($f_0$). The frequency capture range ($2f_C$) is defined as

the frequency range of input signals on which the PLL will lock if it was initially out of lock. The frequency lock range ($2f_L$) is defined as the frequency range of input signals on which the loop will stay locked if it was initially in lock. The capture range is smaller or equal to the lock range.

With phase comparator 1, the range of frequencies over which the PLL can acquire lock (capture range) depends on the low-pass filter characteristics and this range can be made as large as the lock range. Phase comparator 1 enables the PLL system to remain in lock in spite of high amounts of noise in the input signal. A typical behavior of this type of phase comparator is that it may lock onto input frequencies that are close to harmonics of the VCO center frequency. Another typical behavior is that the phase angle between the signal and comparator input varies between 0° and 180°, and is 90° at the center frequency. Figure 3 shows the typical phase-to-output response characteristic.

Figure 4 shows the typical waveforms for a PLL with a $f_0$ locked phase comparator 1.



(1)  Average output voltage.

**Fig 3.  Signal-to-comparator inputs phase difference for comparator 1**



**Fig 4.  Typical waveforms for phase-locked loop with a $f_0$ locked phase comparator 1**

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Phase comparator 2 is an edge-controlled digital memory network. It consists of four flip-flops, control gating and a 3-state output circuit comprising p and n-type drivers with a common output node. When the p-type or n-type drivers are ON, they pull the output up to $V_{DD}$ or down to $V_{SS}$ respectively. This type of phase comparator only acts on the positive-going edges of the signals at SIG_IN and COMP_IN. Therefore, the duty factors of these signals are not of importance.

If the signal input frequency is higher than the comparator input frequency, the p-type output driver is maintained ON most of the time, and both the n and p-type drivers are OFF (3-state) the remainder of the time. If the signal input frequency is lower than the comparator input frequency, the n-type output driver is maintained ON most of the time, and both the n and p-type drivers are OFF the remainder of the time. If the signal input and comparator input frequencies are equal, but the signal input lags the comparator input in phase, the n-type output driver is maintained ON for a time corresponding to the phase difference. If the comparator input lags the signal input in phase, the p-type output driver is maintained ON for a time corresponding to the phase difference. Subsequently, the voltage at the capacitor of the low-pass filter connected to this phase comparator is adjusted until the signal and comparator inputs are equal in both phase and frequency. At this stable point, both p and n-type drivers remain OFF and thus the phase comparator output becomes an open circuit and keeps the voltage at the capacitor of the low-pass filter constant.

Moreover, the signal at the phase comparator pulse output (PCP_OUT) is a HIGH level, which can be used for indicating a locked condition. Thus, for phase comparator 2, no phase difference exists between the signal and comparator inputs over the full VCO frequency range. Moreover, the power dissipation due to the low-pass filter is reduced when this type of phase comparator is used, because both p and n-type output drivers are OFF for most of the signal input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range, independent of the low-pass filter. With no signal present at the signal input, the VCO is adjusted to its lowest frequency for phase comparator 2. Figure 5 shows typical waveforms for a PLL employing this type of locked phase comparator.
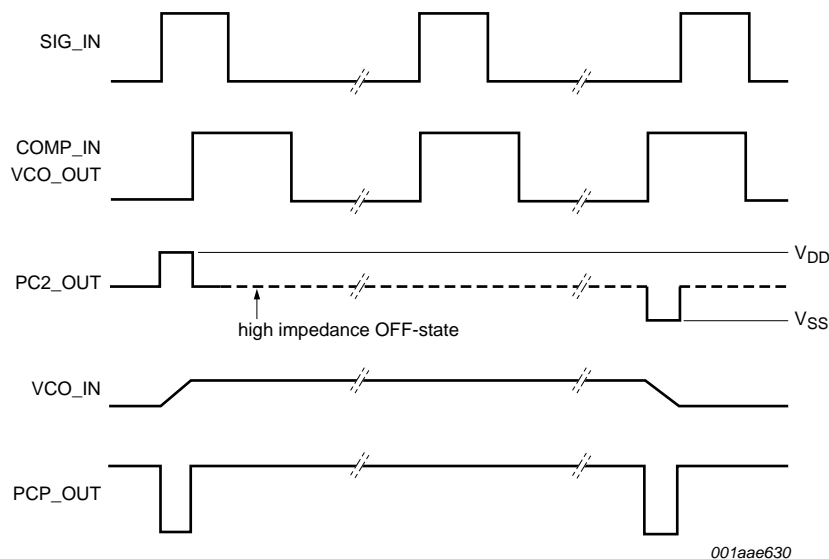


**Fig 5.  Typical waveforms for phase-locked loop with a locked phase comparator 2**

Figure 6 shows the state diagram for phase comparator 2. Each circle represents a state of the comparator. The number at the top, inside each circle, represents the state of the comparator, while the logic state of the signal and comparator inputs are represented by a '0' for a logic LOW or a '1' for a logic HIGH, and they are shown in the left and right bottom of each circle.

The transitions from one to another result from either a logic change at the signal input (S representing SIG_IN) or the comparator input (C representing COMP_IN). A positive-going and a negative-going transition are shown by an arrow pointing up or down respectively.

The state diagram assumes, that only one transition on either the signal input or comparator input occurs at any instant.

- States 3, 5, 9 and 11 represent the output condition when the p-type driver is ON.
- States 2, 4, 10 and 12 determine the condition when the n-type driver is ON.
- States 1, 6, 7 and 8 represent the condition when the output is in its high-impedance OFF state; i.e. both p and n-type drivers are OFF, and the PCP_OUT output is HIGH. The condition at output PCP_OUT for all other states is LOW.



S ↑: 0 to 1 transition at the signal input SIG_IN.

C ↓: 1 to 0 transition at the comparator input COMP_IN.

**Fig 6.**    **State diagram for comparator 2**

# 7. Limiting values

**Table 3.    Limiting values**
*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|--------|-----------|------------|---|-----|-----|------|
| $V_{DD}$ | supply voltage | | | −0.5 | +18 | V |
| $I_{IK}$ | input clamping current | $V_I < −0.5$ V or $V_I > V_{DD} + 0.5$ V | | - | ±10 | mA |
| $V_I$ | input voltage | | | −0.5 | $V_{DD} + 0.5$ | V |
| $I_{OK}$ | output clamping current | $V_O < −0.5$ V or $V_O > V_{DD} + 0.5$ V | | - | ±10 | mA |
| $I_{I/O}$ | input/output current | | | - | ±10 | mA |
| $I_{DD}$ | supply current | | | - | 50 | mA |
| $T_{stg}$ | storage temperature | | | −65 | +150 | °C |
| $T_{amb}$ | ambient temperature | | | −40 | +85 | °C |
| $P_{tot}$ | total power dissipation | DIP16 package | [1] | - | 750 | mW |
| | | SO16 package | [2] | - | 500 | mW |
| P | power dissipation | per output | | - | 100 | mW |

[1]    For DIP16 package: $P_{tot}$ derates linearly with 12 mW/K above 70 °C.

[2]    For SO16 package: $P_{tot}$ derates linearly with 8 mW/K above 70 °C.

# 8. Recommended operating conditions

**Table 4.    Recommended operating conditions**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|-----------|------------|-----|-----|-----|------|
| $V_{DD}$ | supply voltage | | 3 | - | 15 | V |
| | | as fixed oscillator only | 3 | - | 15 | V |
| | | phase-locked loop operation | 5 | - | 15 | V |
| $V_I$ | input voltage | | 0 | - | $V_{DD}$ | V |
| $T_{amb}$ | ambient temperature | in free air | −40 | - | +85 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | for INH input | | | | |
| | | $V_{DD} = 5$ V | - | - | 3.75 | μs/V |
| | | $V_{DD} = 10$ V | - | - | 0.5 | μs/V |
| | | $V_{DD} = 15$ V | - | - | 0.08 | μs/V |

## 9. Static characteristics

**Table 5.    Static characteristics**

*$V_{SS}$ = 0 V; $V_I$ = $V_{SS}$ or $V_{DD}$ unless otherwise specified.*

| Symbol | Parameter | Conditions | $V_{DD}$ | $T_{amb}$ = −40 °C | | $T_{amb}$ = 25 °C | | $T_{amb}$ = 85 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | Min | Max | |
| $V_{IH}$ | HIGH-level input voltage | $\|I_O\|$ < 1 µA | 5 V | 3.5 | - | 3.5 | - | 3.5 | - | V |
| | | | 10 V | 7.0 | - | 7.0 | - | 7.0 | - | V |
| | | | 15 V | 11.0 | - | 11.0 | - | 11.0 | - | V |
| $V_{IL}$ | LOW-level input voltage | $\|I_O\|$ < 1 µA | 5 V | - | 1.5 | - | 1.5 | - | 1.5 | V |
| | | | 10 V | - | 3.0 | - | 3.0 | - | 3.0 | V |
| | | | 15 V | - | 4.0 | - | 4.0 | - | 4.0 | V |
| $V_{OH}$ | HIGH-level output voltage | $\|I_O\|$ < 1 µA | 5 V | 4.95 | - | 4.95 | - | 4.95 | - | V |
| | | | 10 V | 9.95 | - | 9.95 | - | 9.95 | - | V |
| | | | 15 V | 14.95 | - | 14.95 | - | 14.95 | - | V |
| $V_{OL}$ | LOW-level output voltage | $\|I_O\|$ < 1 µA | 5 V | - | 0.05 | - | 0.05 | - | 0.05 | V |
| | | | 10 V | - | 0.05 | - | 0.05 | - | 0.05 | V |
| | | | 15 V | - | 0.05 | - | 0.05 | - | 0.05 | V |
| $I_{OH}$ | HIGH-level output current | $V_O$ = 2.5 V | 5 V | - | −1.7 | - | −1.4 | - | −1.1 | mA |
| | | $V_O$ = 4.6 V | 5 V | - | −0.52 | - | −0.44 | - | −0.36 | mA |
| | | $V_O$ = 9.5 V | 10 V | - | −1.3 | - | −1.1 | - | −0.9 | mA |
| | | $V_O$ = 13.5 V | 15 V | - | −3.6 | - | −3.0 | - | −2.4 | mA |
| $I_{OL}$ | LOW-level output current | $V_O$ = 0.4 V | 5 V | 0.52 | - | 0.44 | - | 0.36 | - | mA |
| | | $V_O$ = 0.5 V | 10 V | 1.3 | - | 1.1 | - | 0.9 | - | mA |
| | | $V_O$ = 1.5 V | 15 V | 3.6 | - | 3.0 | - | 2.4 | - | mA |
| $I_I$ | input leakage current | | 15 V | - | ±0.3 | - | ±0.3 | - | ±1.0 | µA |
| $I_{OZ}$ | OFF-state output current | output HIGH and returned to $V_{DD}$ | 15 V | - | 1.6 | - | 1.6 | - | 12.0 | µA |
| | | output LOW and returned to $V_{SS}$ | 15 V | - | 1.6 | - | 1.6 | - | 12.0 | µA |
| $I_{DD}$ | supply current | | 5 V [1] | - | - | 20 | - | - | - | µA |
| | | | 10 V [1] | - | - | 300 | - | - | - | µA |
| | | | 15 V [1] | - | - | 750 | - | - | - | µA |
| | | $I_O$ = 0 A | 5 V [2] | - | 20 | - | 20 | - | 150 | µA |
| | | | 10 V [2] | - | 40 | - | 40 | - | 300 | µA |
| | | | 15 V [2] | - | 80 | - | 80 | - | 600 | µA |
| $C_I$ | input capacitance | for INH input | | - | - | - | 7.5 | - | - | pF |

[1]    Pin 15 open; pin 5 at $V_{DD}$; pins 3 and 9 at $V_{SS}$; pin 14 open.

[2]    Pin 15 open; pin 5 at $V_{DD}$; pins 3 and 9 at $V_{SS}$; pin 14 at $V_{DD}$; input current pin 14 not included.

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## 10. Dynamic characteristics

**Table 6.    Dynamic characteristics**

*$V_{SS} = 0$ V; $T_{amb} = 25$ °C; $C_L = 50$ pF; input transition times $\leqslant$20 ns.*

| Symbol | Parameter | Conditions | $V_{DD}$ | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Phase comparators** | | | | | | | |
| $R_I$ | input resistance | SIG_IN input; at self-bias operating point | 5 V | - | 750 | - | kΩ |
| | | | 10 V | - | 220 | - | kΩ |
| | | | 15 V | - | 140 | - | kΩ |
| $V_{i(sens)}$ | input voltage sensitivity | SIG_IN input A.C. coupled; peak-to-peak values; R1 = 10 kΩ; R2 = ∞; C1 = 100 pF; independent of the lock range | 5 V | - | 150 | - | mV |
| | | | 10 V | - | 150 | - | mV |
| | | | 15 V | - | 200 | - | mV |
| $V_{IL}$ | LOW-level input voltage | SIG_IN and COMP_IN inputs, DC coupled LOW; full temperature range | 5 V | - | - | 1.5 | V |
| | | | 10 V | - | - | 3.0 | V |
| | | | 15 V | - | - | 4.0 | V |
| $V_{IH}$ | HIGH-level input voltage | SIG_IN and COMP_IN inputs, D.C. coupled HIGH; full temperature range | 5 V | 3.5 | - | - | V |
| | | | 10 V | 7.0 | - | - | V |
| | | | 15 V | 11.0 | - | - | V |
| $I_{IH}$ | HIGH-level input current | SIG_IN input; at $V_{DD}$ | 5 V | - | 7 | - | μA |
| | | | 10 V | - | 30 | - | μA |
| | | | 15 V | - | 70 | - | μA |
| $I_{IL}$ | LOW-level input current | SIG_IN input; at $V_{SS}$ | 5 V | - | −3 | - | μA |
| | | | 10 V | - | −18 | - | μA |
| | | | 15 V | - | −45 | - | μA |
| **VCO** | | | | | | | |
| P | power dissipation | $f_0 = 10$ kHz; R1 = 1 MΩ; R2 = ∞; VCO_IN at 0.5 $V_{DD}$; see Figure 10 to 12 | 5 V | - | 150 | - | μW |
| | | | 10 V | - | 2500 | - | μW |
| | | | 15 V | - | 9000 | - | μW |
| $f_{max}$ | maximum frequency | VCO_IN at $V_{DD}$; R1 = 10 kΩ; R2 = ∞; C1 = 50 pF | 5 V | 0.5 | 1.0 | - | MHz |
| | | | 10 V | 1.0 | 2.0 | - | MHz |
| | | | 15 V | 1.3 | 2.7 | - | MHz |
| $\Delta f/\Delta T$ | frequency variation with temperature | no frequency offset ($f_{min} = 0$ Hz) | 5 V [1] | - | 0.22 to 0.30 | - | % Hz/°C |
| | | | 10 V [1] | - | 0.04 to 0.05 | - | % Hz/°C |
| | | | 15 V [1] | - | 0.01 to 0.05 | - | % Hz/°C |
| | | with frequency offset ($f_{min} > 0$ Hz) | 5 V [1] | - | 0 to 0.22 | - | % Hz/°C |
| | | | 10 V [1] | - | 0 to 0.04 | - | % Hz/°C |
| | | | 15 V [1] | - | 0 to 0.01 | - | % Hz/°C |

**Table 6.** **Dynamic characteristics** *…continued*

$V_{SS} = 0$ V; $T_{amb} = 25$ °C; $C_L = 50$ pF; input transition times $\leq 20$ ns.

| Symbol | Parameter | Conditions | $V_{DD}$ | Min | Typ | Max | Unit |
|--------|-----------|------------|----------|-----|-----|-----|------|
| $\Delta f/f$ | relative frequency variation | for VCO see Figure 13 and 14 | | | | | |
| | | R1 > 10 kΩ | 5 V | - | 0.50 | - | % Hz |
| | | R1 > 400 kΩ | 10 V | - | 0.25 | - | % Hz |
| | | R1 = MΩ | 15 V | - | 0.25 | - | % Hz |
| $\delta$ | duty factor | VCO _OUT output | 5 V | - | 50 | - | % |
| | | | 10 V | - | 50 | - | % |
| | | | 15 V | - | 50 | - | % |
| $R_{in}$ | input resistance | for pin VCO_IN | | | 10 | | MΩ |
| **Source follower** | | | | | | | |
| $V_{offset}$ | offset voltage | $R_L = 10$ kΩ; VCO_IN at $0.5V_{DD}$ | 5 V | [2] - | 1.7 | - | V |
| | | | 10 V | - | 2.0 | - | V |
| | | | 15 V | - | 2.1 | - | V |
| | | $R_L = 50$ kΩ; VCO_IN at $0.5V_{DD}$ | 5 V | - | 1.5 | - | V |
| | | | 10 V | - | 1.7 | - | V |
| | | | 15 V | - | 1.8 | - | V |
| $\Delta f/f$ | relative frequency variation | VCO output; $R_L > 50$ kΩ; see Figure 13 | 5 V | - | 0.3 | - | % |
| | | | 10 V | - | 1.0 | - | % |
| | | | 15 V | - | 1.3 | - | % |
| **Zener diode** | | | | | | | |
| $V_Z$ | working voltage | $I_Z = 50$ µA | - | - | 7.3 | - | V |
| $R_{dyn}$ | dynamic resistance | For internal Zener diode; $I_Z = 1$ mA | - | - | 25 | - | Ω |

[1]    Over the recommended component range.

[2]    The offset voltage is equal to the input voltage on pin VCO_IN minus the output voltage on pin SF_OUT.

# 11. Design information

**Table 7.** **Design information**

| Test | Using phase comparator 1 | Using phase comparator 2 |
|------|--------------------------|--------------------------|
| VCO adjusts with no signal on SIG_IN | VCO in PLL system adjusts to center frequency ($f_0$) | VCO in PLL system adjusts to minimum frequency ($f_{min}$) |
| Phase angle between SIG_IN and COMP_IN | 90° at center frequency ($f_0$), approaching 0° and 180° at the ends of the lock range ($2f_L$) | always 0° in lock (positive-going edges) |
| Locks on harmonics of center frequency | yes | no |
| Signal input noise rejection | high | low |
| Lock frequency range ($2f_L$) | the frequency range of the input signal on which the loop will stay locked if it was initially in lock; $2f_L$ = full VCO frequency range = $f_{max} - f_{min}$ | |
| Capture frequency range ($2f_c$) | the frequency range of the input signal on which the loop will lock if it was initially out of lock | |
| | depends on low-pass filter characteristics; $2f_c < 2f_L$ | $2f_c = 2f_L$ |
| Center frequency ($f_0$) | the frequency of the VCO when VCO_IN at $0.5V_{DD}$ | |

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## 11.1 VCO component selection

Recommended range for R1 and R2: 10 kΩ to 1 MΩ; for C1: 50 pF to any practical value.

1. VCO without frequency offset (R2 = ∞). 0

   a. Given $f_0$: use $f_0$ with Figure 7 to determine R1 and C1.

   b. Given $f_{max}$: calculate $f_0$ from $f_0 = 0.5f_{max}$; use $f_0$ with Figure 7 to determine R1 and C1.

2. VCO with frequency offset.

   a. Given $f_0$ and $2f_L$ : calculate $f_{min}$ from the equation $f_{min} = f_0 - 2f_L$; use $f_{min}$ with

   Figure 8 to determine R2 and C1; calculate $\dfrac{f_{max}}{f_{min}}$ from the equation

   $\dfrac{f_{max}}{f_{min}} = \dfrac{f_0 + 2f_L}{f_0 - 2f_L}$ ; use $\dfrac{f_{max}}{f_{min}}$ with Figure 9 to determine the ratio R2/R1 to obtain R1.

   b. Given $f_{min}$ and $f_{max}$: use $f_{min}$ with Figure 8 to determine R2 and C1; calculate $\dfrac{f_{max}}{f_{min}}$ ;

   use $\dfrac{f_{max}}{f_{min}}$ with Figure 9 to determine R2/R1 to obtain R1.
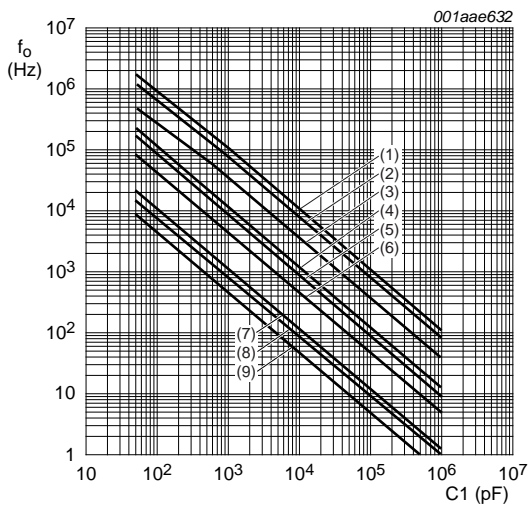


$T_{amb}$ = 25 °C; VCO_IN at $0.5V_{DD}$;
INH_IN at $V_{SS}$; R2 = ∞.
Lines (1), (4), and (7): $V_{DD}$ = 15 V;
Lines (2), (5), and (8): $V_{DD}$ = 10 V;
Lines (3), (6), and (9): $V_{DD}$ = 5 V;
Lines (1), (2), and (3): R1 = 10 kΩ;
Lines (4), (5), and (6): R1 = 100 kΩ;
Lines (7), (8), and (9): R1 = 1 MΩ.

**Fig 7. Typical center frequency as a function of capacitor C1**
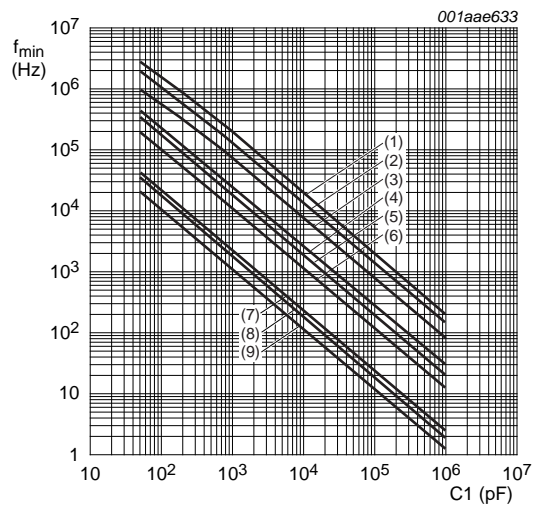
$T_{amb}$ = 25 °C; VCO_IN at $V_{SS}$; INH_IN at $V_{SS}$; R1 = ∞.
Lines (1), (4), and (7): $V_{DD}$ = 15 V;
Lines (2), (5), and (8): $V_{DD}$ = 10 V;
Lines (3), (6), and (9): $V_{DD}$ = 5 V;
Lines (1), (2), and (3): R2 = 10 kΩ;
Lines (4), (5), and (6): R2 = 100 kΩ;
Lines (7), (8), and (9): R2 = 1 MΩ.

**Fig 8. Typical frequency offset as a function of capacitor C1**

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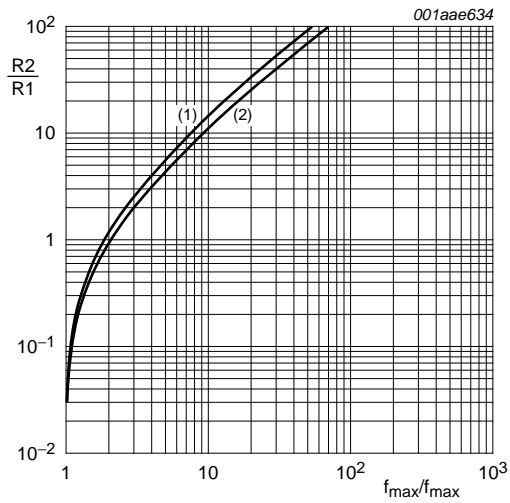
Line (1): $V_{DD}$ = 5 V;
Line (2): $V_{DD}$ = 10 V, 15 V.

**Fig 9. Typical ratio of R2/R1 as a function of the ratio $f_{max}/f_{min}$**
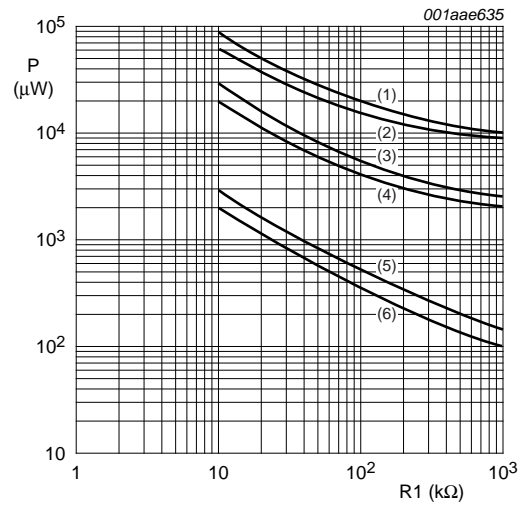


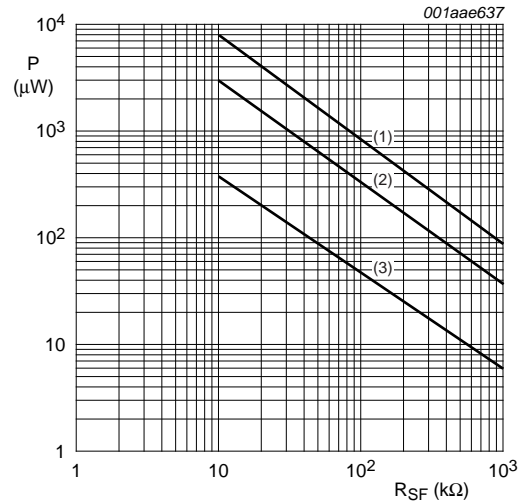$R2 = \infty$; VCO_IN at $0.5V_{DD}$; $C_L$ = 50 pF.
Lines (1) and (2): $V_{DD}$ = 15 V;
Lines (3) and (4): $V_{DD}$ = 10 V;
Lines (5) and (6): $V_{DD}$ = 5 V;
Lines (1), (3), and (5): C1 = 50 pF;
Lines (2), (4), and (6): C1 = 1 μF.
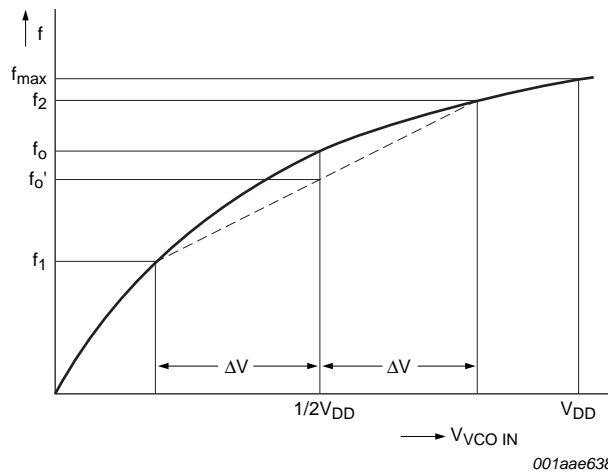
**Fig 10. Power dissipation as a function of R1**
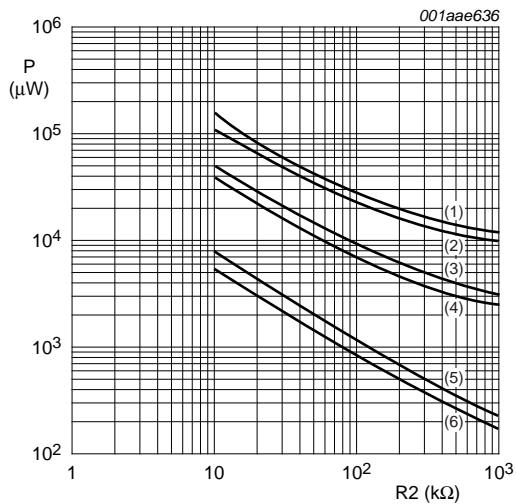


$R1 = \infty$; VCO_IN at $V_{SS}$ (0 V); $C_L$ = 50 pF.
Lines (1) and (2): $V_{DD}$ = 15 V;
Lines (3) and (4): $V_{DD}$ = 10 V;
Lines (5) and (6): $V_{DD}$ = 5 V;
Lines (1), (3), and (5): C1 = 50 pF;
Lines (2), (4), and (6): C1 = 1 μF.

**Fig 11. Power dissipation as a function of R2**



VCO_IN at $0.5V_{DD}$; $R1 = \infty$; $R2 = \infty$.
Line (1): $V_{DD}$ = 15 V;
Line (2): $V_{DD}$ = 10 V;
Line (3): $V_{DD}$ = 5 V.

**Fig 12. Power dissipation of source follower as a function of $R_L$**

See Section 10.

For VCO linearity:

$$f'_0 = \frac{f_1 + f_2}{2}$$
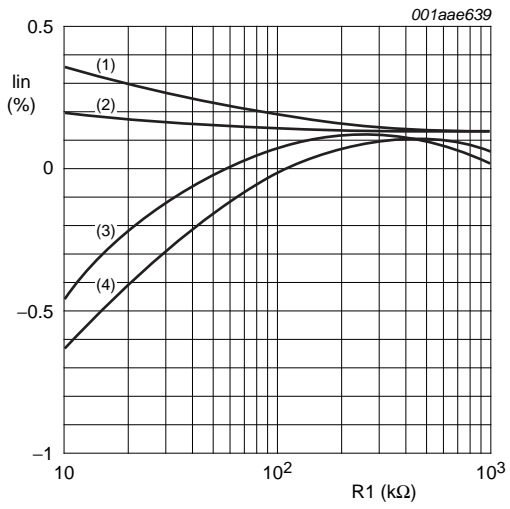
$$linearity = \frac{f'_0 - f_0}{f'_0} \times 100 \text{ %}$$

This figure and the above formula also apply to source follower linearity: substitute $V_O$ at SF_OUT for f.

$\Delta V = 0.3$ V at $V_{DD} = 5$ V;

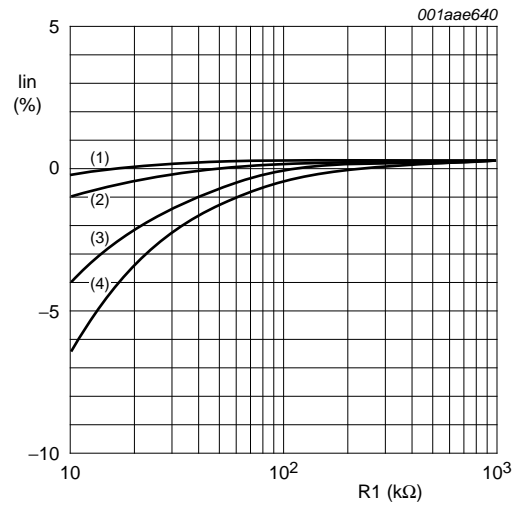$\Delta V = 2.5$ V at $V_{DD} = 10$ V;

$\Delta V = 5.0$ V at $V_{DD} = 15$ V.

**Fig 13. Definition of linearity**

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a. $V_{DD} = 5$ V

b. $V_{DD} = 10$ V
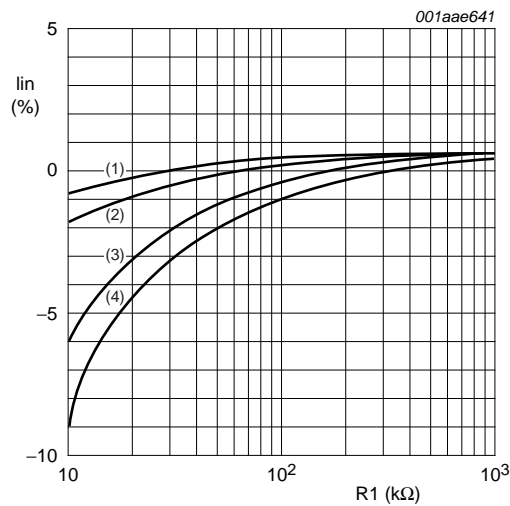
c. $V_{DD} = 15$ V

R2 = ∞;

Line (1): C1 = 1 μF;

Line (2): C1 = 1 nF;

Line (3): C1 = 100 pF;

Line (4): C1 = 50 pF.

**Fig 14. VCO frequency linearity as a function of R1**

## 12. Package outline

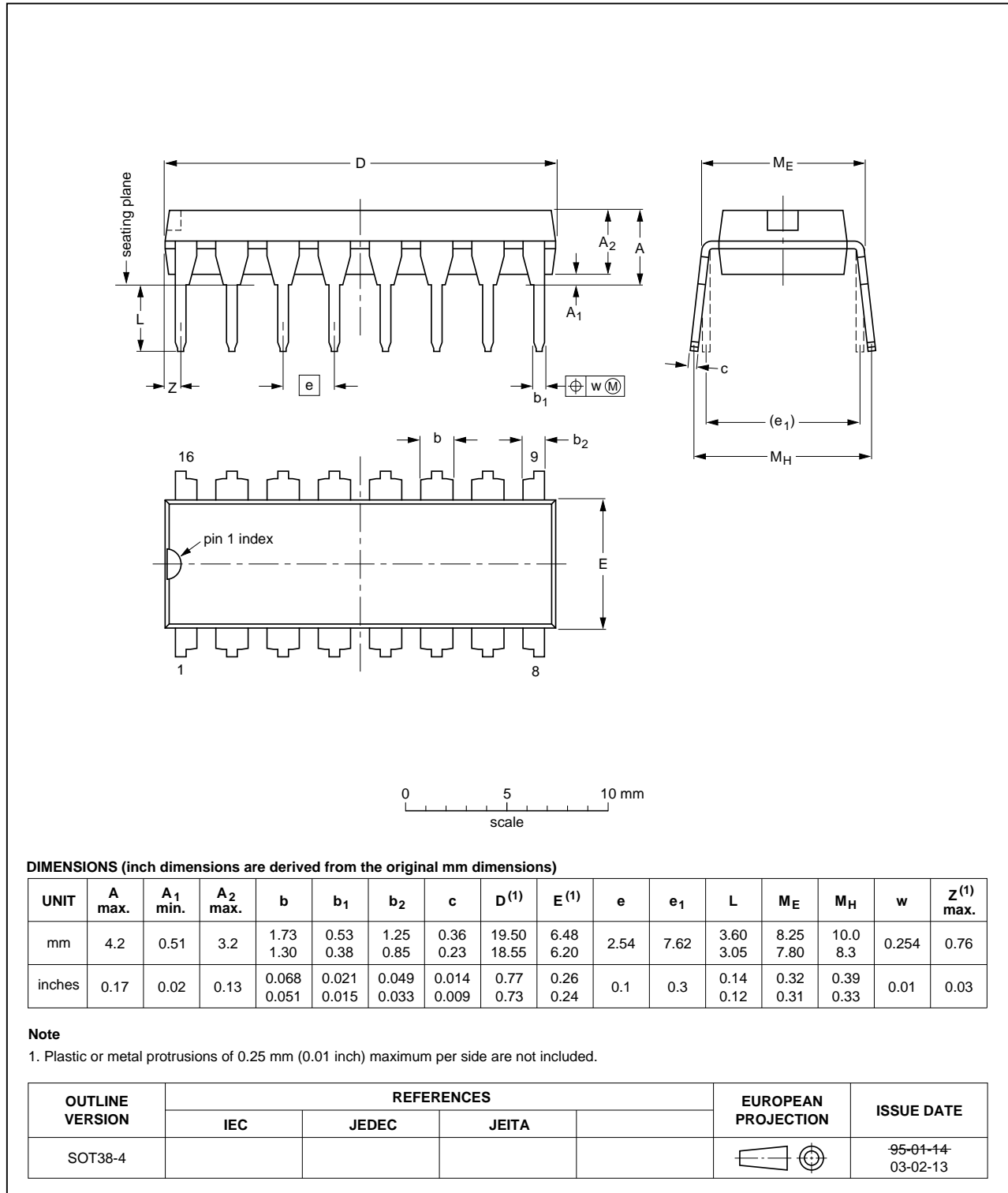**DIP16: plastic dual in-line package; 16 leads (300 mil)**　　　　　　　　**SOT38-4**



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | A₁ min. | A₂ max. | b | b₁ | b₂ | c | D [1] | E [1] | e | e₁ | L | M_E | M_H | w | Z [1] max. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 4.2 | 0.51 | 3.2 | 1.73 1.30 | 0.53 0.38 | 1.25 0.85 | 0.36 0.23 | 19.50 18.55 | 6.48 6.20 | 2.54 | 7.62 | 3.60 3.05 | 8.25 7.80 | 10.0 8.3 | 0.254 | 0.76 |
| inches | 0.17 | 0.02 | 0.13 | 0.068 0.051 | 0.021 0.015 | 0.049 0.033 | 0.014 0.009 | 0.77 0.73 | 0.26 0.24 | 0.1 | 0.3 | 0.14 0.12 | 0.32 0.31 | 0.39 0.33 | 0.01 | 0.03 |

**Note**

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT38-4 | | | | | | ~~95-01-14~~ 03-02-13 |

**Fig 15.　Package outline SOT38-4 (DIP16)**

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**SO16: plastic small outline package; 16 leads; body width 3.9 mm**

**SOT109-1**



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | A₁ | A₂ | A₃ | bₚ | c | D[1] | E[1] | e | H_E | L | Lₚ | Q | v | w | y | Z[1] | θ |
|------|--------|-----|------|------|------|--------|------|------|------|------|------|------|------|------|------|-------|------|-------|
| mm | 1.75 | 0.25 0.10 | 1.45 1.25 | 0.25 | 0.49 0.36 | 0.25 0.19 | 10.0 9.8 | 4.0 3.8 | 1.27 | 6.2 5.8 | 1.05 | 1.0 0.4 | 0.7 0.6 | 0.25 | 0.25 | 0.1 | 0.7 0.3 | 8° 0° |
| inches | 0.069 | 0.010 0.004 | 0.057 0.049 | 0.01 | 0.019 0.014 | 0.0100 0.0075 | 0.39 0.38 | 0.16 0.15 | 0.05 | 0.244 0.228 | 0.041 | 0.039 0.016 | 0.028 0.020 | 0.01 | 0.01 | 0.004 | 0.028 0.012 | |

**Note**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|-------|-------|---|---------------------|------------|
| | IEC | JEDEC | JEITA | | | |
| SOT109-1 | 076E07 | MS-012 | | | | ~~99-12-27~~ 03-02-19 |

**Fig 16. Package outline SOT109-1 (SO16)**

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## 13. Revision history

**Table 8.    Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| HEF4046B v.5 | 20111118 | Product data sheet | - | HEF4046B v.4 |
| Modifications: | • Section Applications removed<br>• Table 5: $I_{OH}$ minimum values changed to maximum<br>• Table 6: $R_{in}$ typical value changed from $10^6$ MΩ to 10 MΩ | | | |
| HEF4046B v.4 | 20100105 | Product data sheet | - | HEF4046B_CNV v.3 |
| HEF4046B_CNV v.3 | 19950101 | Product specification | - | HEF4046B_CNV v.2 |
| HEF4046B_CNV v.2 | 19950101 | Product specification | - | - |

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# 14. Legal information

## 14.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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