

# 1. General description

The 74ALVC32 is a quad 2-input OR gate.

Schmitt trigger action on all inputs makes the device tolerant of slow rise and fall times.

## 2. Features and benefits

- Wide supply voltage range from 1.65 V to 3.6 V
- 3.6 V tolerant inputs/outputs
- CMOS low power consumption
- Direct interface with TTL levels (2.7 V to 3.6 V)
- Power-down mode
- Latch-up performance exceeds 250 mA
- Complies with JEDEC standards:
  - JESD8-7 (1.65 V to 1.95 V)
  - ◆ JESD8-5 (2.3 V to 2.7 V)
  - ◆ JESD8B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - ◆ HBM JESD22-A114E exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V

# 3. Ordering information

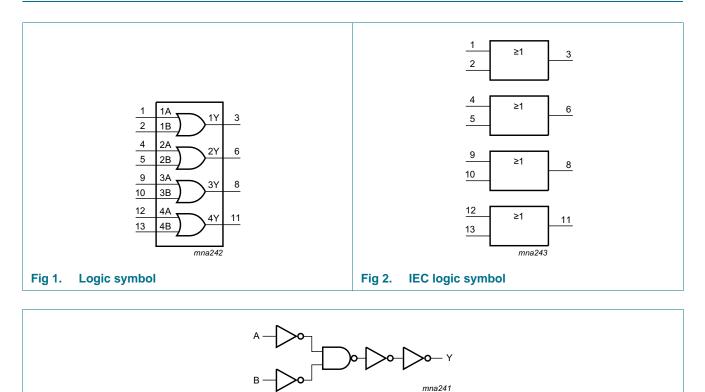
#### Table 1. Ordering information

Type number	Package							
	Temperature range	Name	Description	Version				
74ALVC32D	–40 °C to +85 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1				
74ALVC32PW	–40 °C to +85 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1				
74ALVC32BQ	–40 °C to +85 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body $2.5 \times 3 \times 0.85$ mm	SOT762-1				



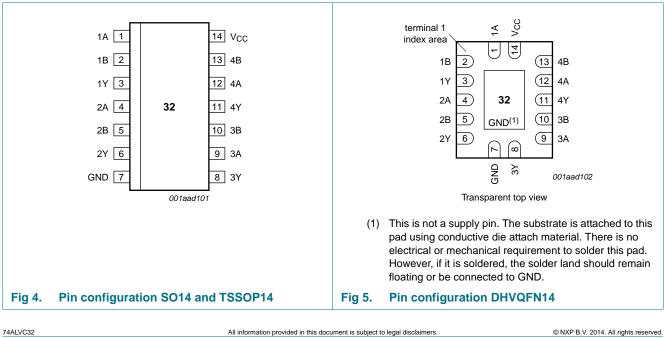
74ALVC32 **Quad 2-input OR gate** 

**Functional diagram** 4.



Logic diagram (one gate) Fig 3.

#### **Pinning information** 5.



## 5.1 Pinning

# 5.2 Pin description

Table 2.	Pin description	
Symbol	Pin	Description
nA	1, 4, 9, 12	data input
nB	2, 5, 10, 13	data input
nY	3, 6, 8, 11	data output
V <sub>CC</sub>	14	supply voltage
GND	7	ground (0 V)

# 6. Functional description

#### Table 3. Function table<sup>[1]</sup>

Input nA	Input nB	Output nY
L	L	L
L	Н	Н
Н	L	Н
Н	Н	Н

[1] H = HIGH voltage level

L = LOW voltage level

# 7. Limiting values

#### Table 4.Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

						-
Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>CC</sub>	supply voltage			-0.5	+4.6	V
I <sub>IK</sub>	input clamping current	V <sub>1</sub> < 0 V		-50	-	mA
VI	input voltage			-0.5	+4.6	V
I <sub>OK</sub>	output clamping current	$V_{O} > V_{CC}$ or $V_{O} < 0 V$		-	±50	mA
Vo	output voltage	output HIGH or LOW state	<u>[1] [2]</u>	-0.5	V <sub>CC</sub> + 0.5	V
		output 3-state		-0.5	+4.6	V
		power-down mode, $V_{CC} = 0 V$	[2]	-0.5	+4.6	V
lo	output current	$V_{O} = 0 V \text{ to } V_{CC}$		-	±50	mA
I <sub>CC</sub>	supply current			-	100	mA
I <sub>GND</sub>	ground current			-100	-	mA
T <sub>stg</sub>	storage temperature			-65	+150	°C
P <sub>tot</sub>	total power dissipation	$T_{amb} = -40 \ ^{\circ}C \ to \ +85 \ ^{\circ}C$	[3]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] When  $V_{CC} = 0 V$  (power-down mode), the output voltage can be 3.6 V in normal operation.

[3] For SO14 packages: above 70 °C derate linearly with 8 mW/K.

For TSSOP14 packages: above 60 °C derate linearly with 5.5 mW/K.

For DHVQFN14 packages: above 60 °C derate linearly with 4.5 mW/K.

Quad 2-input OR gate

# 8. Recommended operating conditions

Table 5.	Recommended operating condit	ions			
Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		1.65	3.6	V
VI	input voltage		0	3.6	V
Vo	output voltage	output HIGH or LOW state	0	V <sub>CC</sub>	V
		output 3-state	0	3.6	V
		power-down mode; $V_{CC} = 0 V$	0	3.6	V
T <sub>amb</sub>	ambient temperature	in free air	-40	+85	°C
$\Delta t / \Delta V$	input transition rise and fall rate	$V_{CC}$ = 1.65 V to 2.7 V	0	20	ns/V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	0	10	ns/V

# 9. Static characteristics

#### Table 6.Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T <sub>amb</sub> =	T <sub>amb</sub> = −40 °C to +85 °C				
			Min	Typ <mark>[1]</mark>	Max			
VIH	HIGH-level input voltage	$V_{CC} = 1.65 \text{ V}$ to 1.95 V	$0.65  imes V_{CC}$	-	-	V		
		$V_{CC}$ = 2.3 V to 2.7 V	1.7	-	-	V		
		$V_{CC}$ = 2.7 V to 3.6 V	2.0	-	-	V		
V <sub>IL</sub>	LOW-level input voltage	$V_{CC} = 1.65 \text{ V}$ to 1.95 V	-	-	$0.35 \times V_{CC}$	V		
		$V_{CC}$ = 2.3 V to 2.7 V	-	-	0.7	V		
		$V_{CC}$ = 2.7 V to 3.6 V	-	-	0.8	V		
V <sub>он</sub>	HIGH-level output voltage	$V_{I} = V_{IH} \text{ or } V_{IL}$						
		$I_{O}$ = $-100~\mu\text{A};~V_{CC}$ = 1.65 V to 3.6 V	$V_{CC}-0.2$	-	-	V		
		$I_0 = -6 \text{ mA}; V_{CC} = 1.65 \text{ V}$	1.25	1.51	-	V		
		$I_{O} = -12 \text{ mA}; V_{CC} = 2.3 \text{ V}$	1.8	2.10	-	V		
		$I_{O} = -18 \text{ mA}; V_{CC} = 2.3 \text{ V}$	1.7	2.01	-	V		
		$I_{O} = -12 \text{ mA}; V_{CC} = 2.7 \text{ V}$	2.2	2.53	-	V		
		$I_{O} = -18 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.4	2.76	-	V		
		$I_{O} = -24$ mA; $V_{CC} = 3.0$ V	2.2	2.68	-	V		
V <sub>OL</sub>	LOW-level output voltage	$V_{I} = V_{IH} \text{ or } V_{IL}$						
		$I_{O}$ = 100 $\mu\text{A};V_{CC}$ = 1.65 V to 3.6 V	-	-	0.2	V		
		$I_0 = 6 \text{ mA}; V_{CC} = 1.65 \text{ V}$	-	0.11	0.3	V		
		$I_0 = 12 \text{ mA}; V_{CC} = 2.3 \text{ V}$	-	0.17	0.4	V		
		$I_0$ = 18 mA; $V_{CC}$ = 2.3 V	-	0.25	0.6	V		
		$I_0 = 12 \text{ mA}; V_{CC} = 2.7 \text{ V}$	-	0.16	0.4	V		
		$I_0 = 18 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	0.23	0.4	V		
		$I_{O} = 24 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	0.30	0.55	V		
<sub> </sub>	input leakage current	$V_{CC} = 3.6 \text{ V}; \text{ V}_{I} = 3.6 \text{ V} \text{ or GND}$	-	±0.1	±5	μΑ		
OFF	power-off leakage current	$V_{CC} = 0 \text{ V}; \text{ V}_{I} \text{ or } \text{ V}_{O} = 0 \text{ V to } 3.6 \text{ V}$	-	±0.1	±10	μA		

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**Quad 2-input OR gate** 

At recom	At recommended operating conditions. Voltages are referenced to GND (ground = $0$ V).							
Symbol	Parameter	Conditions	T <sub>amb</sub> =	Unit				
			Min	Typ <mark>[1]</mark>	Мах			
I <sub>CC</sub>	supply current	$V_{CC} = 3.6 \text{ V}; V_I = V_{CC} \text{ or GND};$ $I_O = 0 \text{ A}$	-	0.2	10	μA		
$\Delta I_{CC}$	additional supply current	per input pin; V <sub>CC</sub> = 3.0 V to 3.6 V; V <sub>I</sub> = V <sub>CC</sub> – 0.6 V; I <sub>O</sub> = 0 A	-	5	750	μA		
CI	input capacitance		-	3.5	-	pF		

#### Table 6. Static characteristics ... continued

[1] All typical values are measured at V<sub>CC</sub> = 3.3 V (unless stated otherwise) and T<sub>amb</sub> = 25 °C.

## **10. Dynamic characteristics**

#### Table 7. **Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 7.

Symbol	Parameter	Conditions		T <sub>amb</sub> =	Unit		
				Min	Typ <mark>[1]</mark>	Max	
t <sub>pd</sub>	propagation delay	CP to Qn; see Figure 6	[2]				
		$V_{CC} = 1.65 \text{ V} \text{ to } 1.95 \text{ V}$		1.0	2.8	4.7	ns
		$V_{CC}$ = 2.3 V to 2.7 V		1.0	2.0	3.1	ns
		$V_{CC} = 2.7 V$		1.0	2.2	2.9	ns
		$V_{CC} = 3.0 \text{ V} \text{ to } 3.6 \text{ V}$		1.0	2.0	2.8	ns
C <sub>PD</sub>	power dissipation capacitance	per gate; V <sub>I</sub> = GND to V <sub>CC</sub> ; V <sub>CC</sub> = 3.3 V	<u>[3]</u>	-	25	-	pF

[1] Typical values are measured at  $T_{amb} = 25 \ ^{\circ}C$ 

[2]  $t_{pd}$  is the same as  $t_{PHL}$  and  $t_{PLH}$ .

[3]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu W$ ).

 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$  where:

 $f_i$  = input frequency in MHz;  $f_o$  = output frequency in MHz

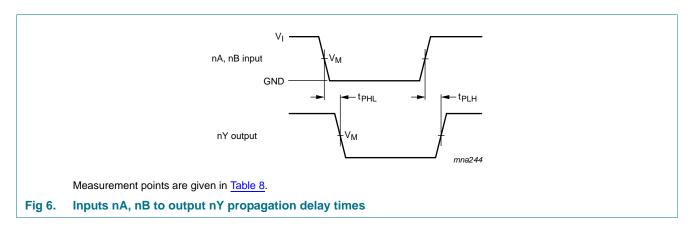
C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in Volts

N = number of inputs switching

 $\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs

# 11. Waveforms



#### Table 8.Measurement points

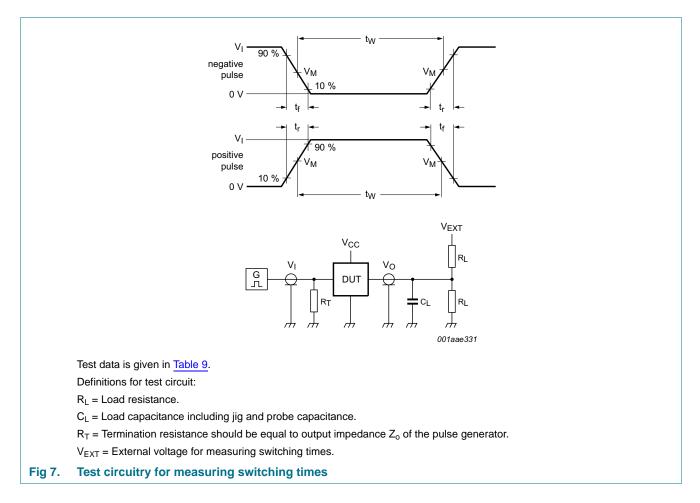
Supply voltage V <sub>CC</sub>	Input V <sub>I</sub>	V <sub>M</sub>
1.65 V to 1.95 V	V <sub>CC</sub>	0.5V <sub>CC</sub>
2.3 V to 2.7 V	V <sub>CC</sub>	0.5V <sub>CC</sub>
2.7 V	2.7 V	1.5 V
3.0 V to 3.6 V	2.7 V	1.5 V

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## **NXP Semiconductors**

# 74ALVC32

#### Quad 2-input OR gate

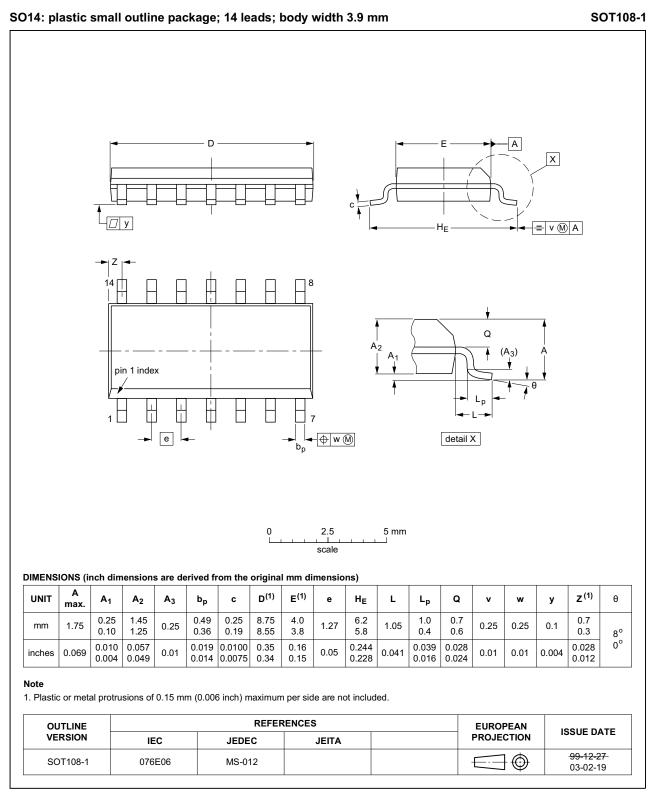


#### Table 9. Test data

Supply voltage V <sub>CC</sub>	Input		Load	Load		V <sub>EXT</sub>		
	VI	t <sub>r</sub> , t <sub>f</sub>	CL	RL	t <sub>PLH</sub> , t <sub>PHL</sub>	t <sub>PLZ</sub> , t <sub>PZL</sub>	t <sub>PHZ</sub> , t <sub>PZH</sub>	
1.65 V to 1.95 V	V <sub>CC</sub>	$\leq$ 2.0 ns	30 pF	1 kΩ	open	$2 \times V_{CC}$	GND	
2.3 V to 2.7 V	V <sub>CC</sub>	$\leq$ 2.0 ns	30 pF	500 Ω	open	$2 \times V_{CC}$	GND	
2.7 V	2.7 V	$\leq$ 2.5 ns	50 pF	500 Ω	open	6 V	GND	
3.0 V to 3.6 V	2.7 V	$\leq$ 2.5 ns	50 pF	500 Ω	open	6 V	GND	

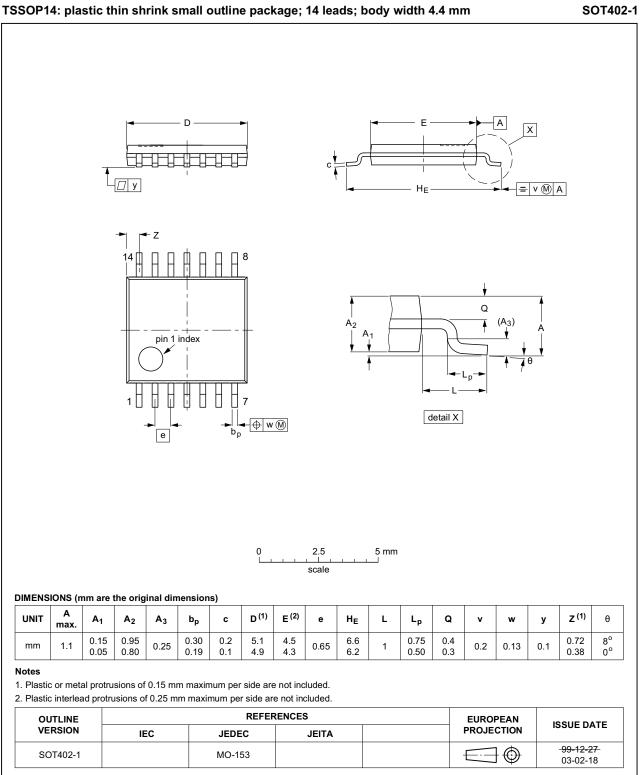
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# 12. Package outline



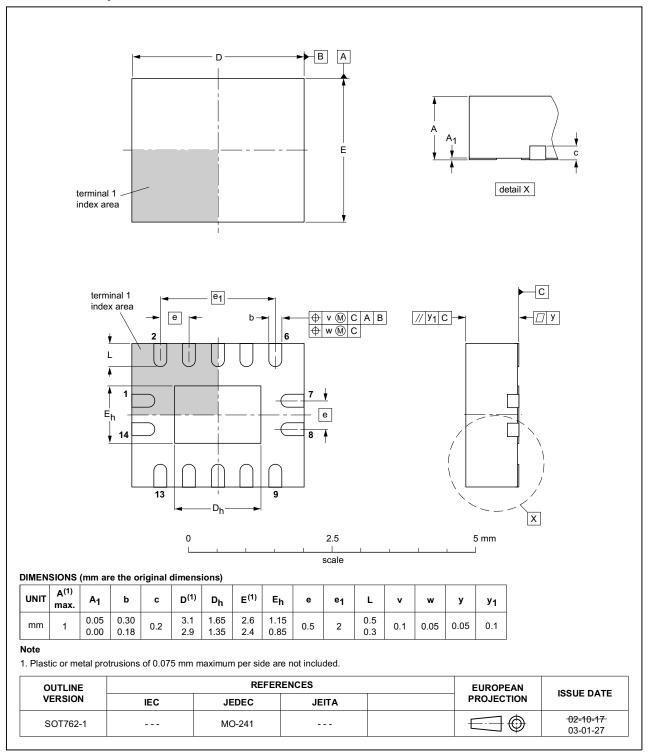
#### Fig 8. Package outline SOT108-1 (SO14)

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Package outline SOT402-1 (TSSOP14) Fig 9.

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#### DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm SOT762-1

#### Fig 10. Package outline SOT762-1 (DHVQFN14)



# **13. Abbreviations**

Table 10.	Abbreviations
Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

# 14. Revision history

Table 11. Revi	sion history					
Document ID	Release date	Data sheet status	Change notice	Supersedes		
74ALVC32 v.3	20140120	Product data sheet	-	74ALVC32 v.2		
<ul> <li>The format of this data sheet has been redesigned to comply with the new identity guideline of NXP Semiconductors.</li> </ul>						
	<ul> <li>Legal texts hat</li> </ul>	ve been adapted to the new	company name where	e appropriate.		
74ALVC32 v.2	20071210	Product data sheet	-	74ALVC32 v.1		
74ALVC32 v.1	20021115	Product specification	-	-		

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Document status[1][2]	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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# 74ALVC32

#### Quad 2-input OR gate

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