

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## **74HC/HCT03** Quad 2-input NAND gate

Product specification  
File under Integrated Circuits, IC06

December 1990

## Quad 2-input NAND gate

## 74HC/HCT03

## FEATURES

- Level shift capability
- Output capability: standard (open drain)
- $I_{CC}$  category: SSI

## GENERAL DESCRIPTION

The 74HC/HCT03 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT03 provide the 2-input NAND function.

The 74HC/HCT03 have open-drain N-transistor outputs, which are not clamped by a diode connected to  $V_{CC}$ . In the OFF-state, i.e. when one input is LOW, the output may be pulled to any voltage between GND and  $V_{Omax}$ . This allows the device to be used as a LOW-to-HIGH or HIGH-to-LOW level shifter. For digital operation and OR-tied output applications, these devices must have a pull-up resistor to establish a logic HIGH level.

## QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $t_r = t_f = 6\text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
$t_{PZL}/t_{PLZ}$	propagation delay	$C_L = 15\text{ pF}$ ; $R_L = 1\text{ k}\Omega$ ; $V_{CC} = 5\text{ V}$	8	10	ns
$C_I$	input capacitance		3.5	3.5	pF
$C_{PD}$	power dissipation capacitance per gate	notes 1, 2 and 3	4.0	4.0	pF

## Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) + \sum (V_O^2/R_L) \times \text{duty factor LOW, where:}$$

$f_i$  = input frequency in MHz

$f_o$  = output frequency in MHz

$V_O$  = output voltage in V

$C_L$  = output load capacitance in pF

$V_{CC}$  = supply voltage in V

$R_L$  = pull-up resistor in  $M\Omega$

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

$\sum (V_O^2/R_L)$  = sum of outputs

2. For HC the condition is  $V_I = \text{GND to } V_{CC}$   
For HCT the condition is  $V_I = \text{GND to } V_{CC} - 1.5\text{ V}$
3. The given value of  $C_{PD}$  is obtained with:  
 $C_L = 0\text{ pF}$  and  $R_L = \infty$

## ORDERING INFORMATION

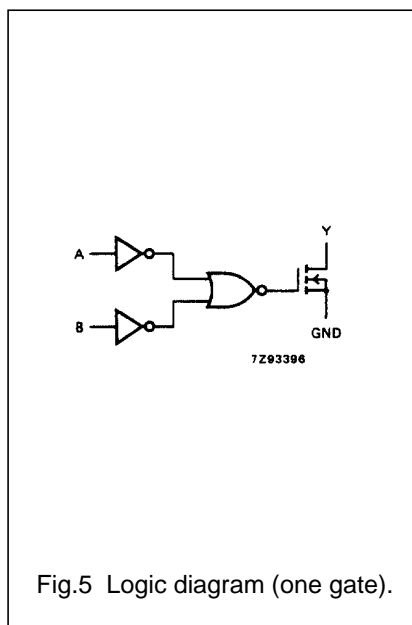
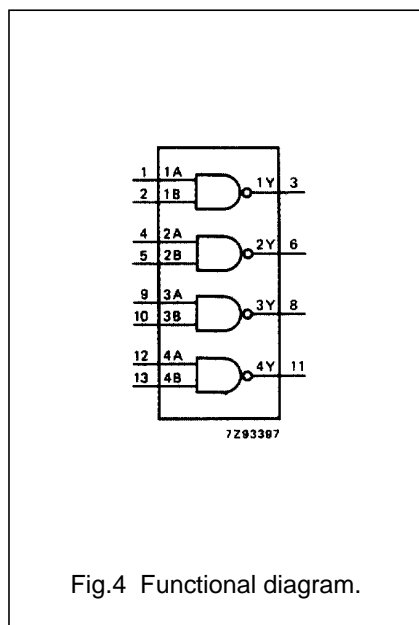
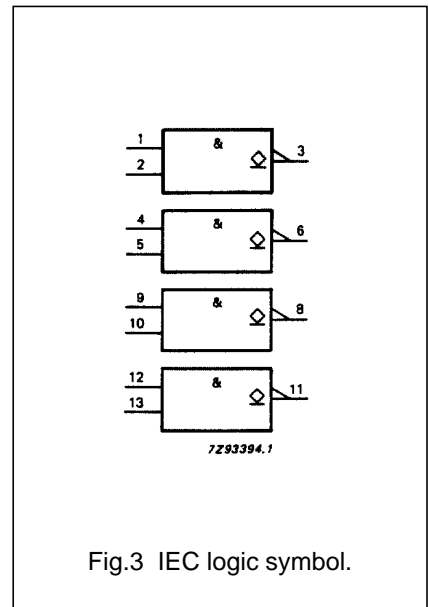
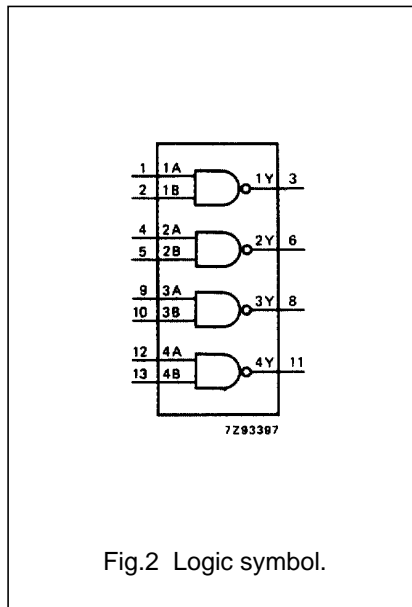
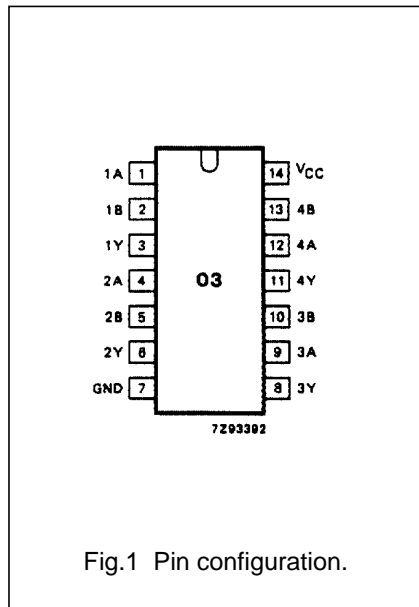
See "74HC/HCT/HCU/HCMOS Logic Package Information".

# Quad 2-input NAND gate

# 74HC/HCT03

## PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	data inputs
2, 5, 10, 13	1B to 4B	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V <sub>CC</sub>	positive supply voltage



## FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	Z
L	H	Z
H	L	Z
H	H	L

### Note

1. H = HIGH voltage level  
L = LOW voltage level  
Z = high impedance OFF-state

## Quad 2-input NAND gate

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**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
$V_{CC}$	DC supply voltage	-0.5	+7	V	
$V_O$	DC output voltage	-0.5	+7	V	
$I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$-I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V
$-I_O$	DC output sink current		25	mA	for $-0.5$ V $< V_O$
$\pm I_{CC};$ $\pm I_{GND}$	DC VCC or GND current		50	mA	
$T_{stg}$	storage temperature range	-65	+150	°C	
$P_{tot}$	power dissipation per package				for temperature range; -40 to +125 °C 74HC/HCT
	plastic DIL		750	mW	above +70 °C: derate linearly with 12 mW/K
	plastic mini-pack (SO)		500	mW	above +70 °C: derate linearly with 8 mW/K

## Quad 2-input NAND gate

## 74HC/HCT03

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*, except that the  $V_{OH}$  values are not valid for open drain. They are replaced by  $I_{OZ}$  as given below.

Output capability: standard (open drain), excepting  $V_{OH}$

$I_{CC}$  category: SSI

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	$T_{amb}$ (°C)							UNIT	TEST CONDITIONS		
		74HC								$V_{CC}$ (V)	$V_I$	OTHER
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
$I_{OZ}$	HIGH level output leakage current			0.5		5.0		10.0	$\mu A$	2.0 to 6.0	$V_{IL}$	$V_O = V_{O(max)}^{(1)}$ or GND

**Note**

- The maximum operating output voltage ( $V_{O(max)}$ ) is 6.0 V.

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)							UNIT	TEST CONDITIONS	
		74HC								$V_{CC}$ (V)	WAVEFORMS
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
$t_{PZL}/$ $t_{PLZ}$	propagation delay nA, nB to nY		28 10 8	95 19 16		120 24 20		145 29 25	ns	2.0 4.5 6.0	Fig.6
$t_{THL}$	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.6

## Quad 2-input NAND gate

## 74HC/HCT03

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*, except that the  $V_{OH}$  values are not valid for open drain. They are replaced by  $I_{OZ}$  as given below.

Output capability: standard (open drain), excepting  $V_{OH}$

$I_{CC}$  category: SSI

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	$T_{amb}$ (°C)								UNIT	TEST CONDITIONS		
		74HCT									$V_{CC}$ (V)	$V_I$	OTHER
		+25			-40 to +85		-40 to +125						
		min.	typ.	max.	min.	max.	min.	max.					
$I_{OZ}$	HIGH level output leakage current			0.5		5.0		10.0	$\mu A$	4.5 to 5.5	$V_{IL}$	$V_O = V_{O(max)}^{(1)}$ or GND	

**Note**

- The maximum operating output voltage ( $V_{O(max)}$ ) is 6.0 V.

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nA, nB	1.0

**AC CHARACTERISTICS FOR 74HCT**

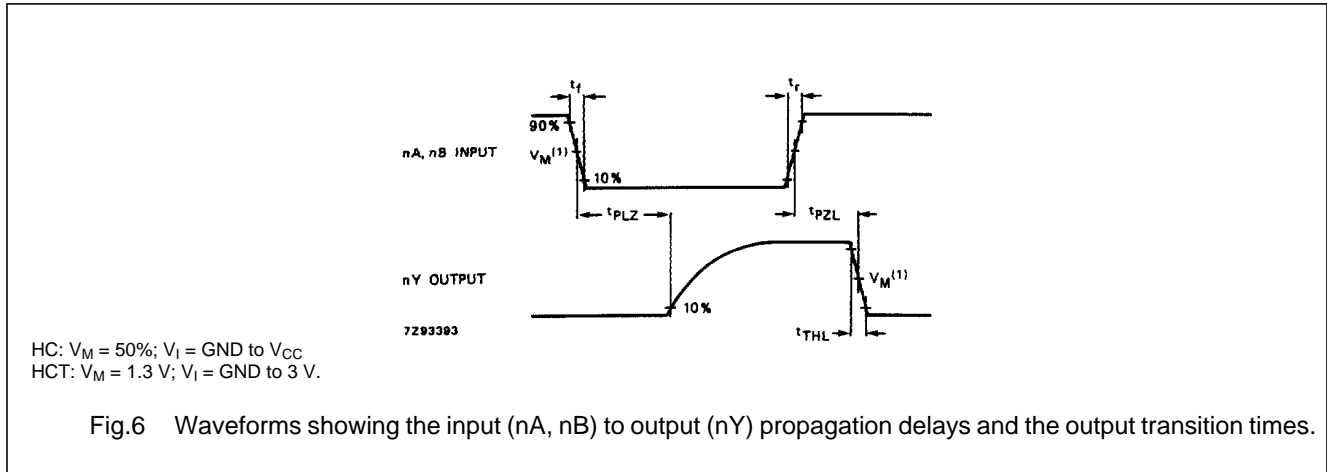
GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)								UNIT	TEST CONDITIONS	
		74HCT									$V_{CC}$ (V)	WAVEFORMS
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
$t_{PZL} / t_{PLZ}$	propagation delay nA, nB, to nY		12	24		30		36	ns	4.5	Fig.6	
$t_{THL}$	output transition time		7	15		19		22	ns	4.5	Fig.6	

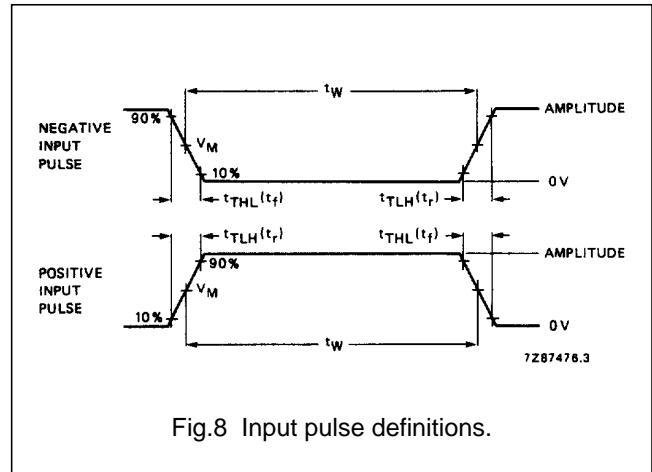
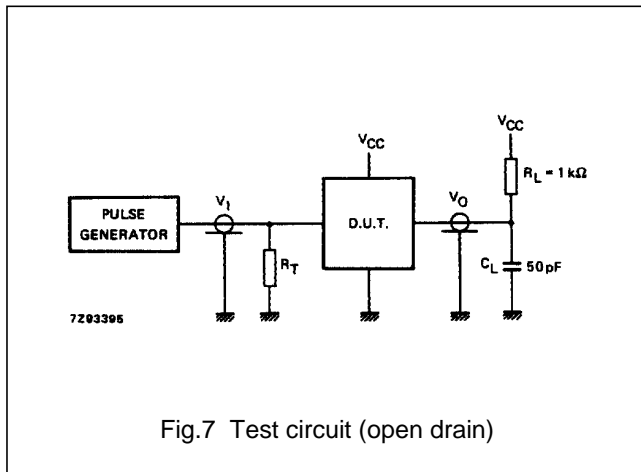
Quad 2-input NAND gate

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AC WAVEFORMS



TEST CIRCUIT AND WAVEFORMS



Definitions for Figs. 7, 8:

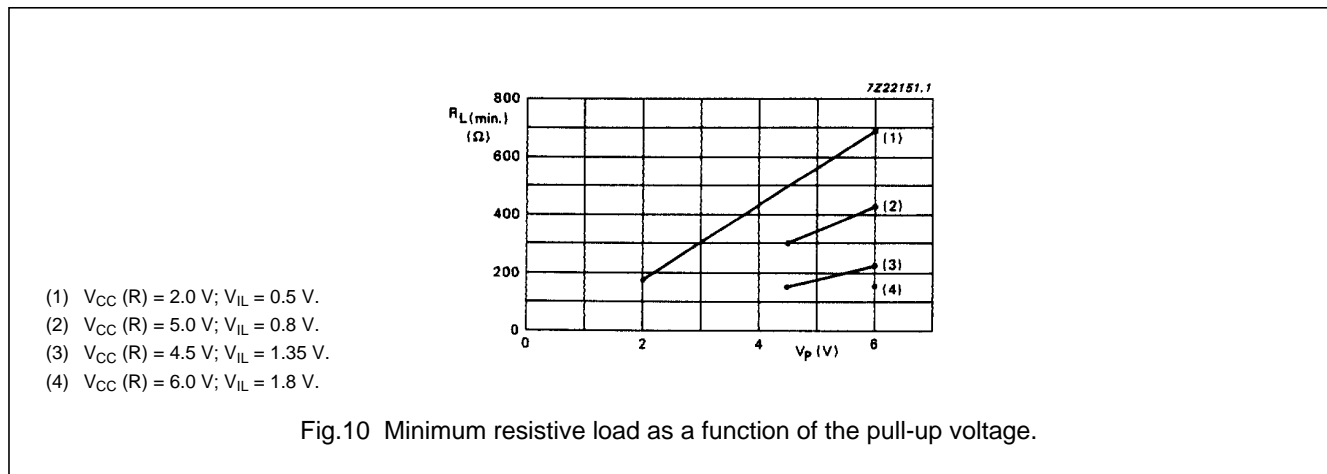
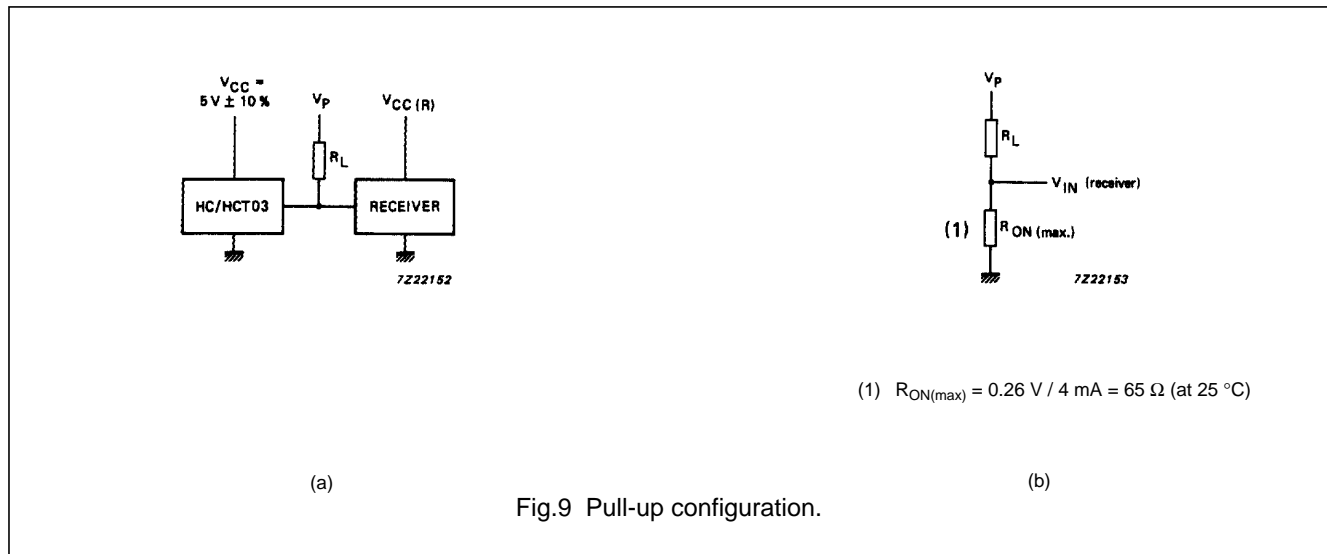
- $C_L$  = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).
- $R_T$  = termination resistance should be equal to the output impedance  $Z_O$  of the pulse generator.
- $t_f$  =  $t_f = 6 \text{ ns}$ ; when measuring  $f_{max}$ , there is no constraint on  $t_r$ ,  $t_f$  with 50% duty factor.

FAMILY	AMPLITUDE	$V_M$	$t_r$ ; $t_f$	
			$f_{max}$ ; PULSE WIDTH	OTHER
74HC	$V_{CC}$	50%	< 2 ns	6 ns
74HCT	3.0 V	1.3 V	< 2 ns	6 ns

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APPLICATION INFORMATION



Notes to Figs 9 and 10

If  $V_P - V_{CC} (R) > 0.5 \text{ V}$  a positive current will flow into the receiver (as described in the "USER GUIDE"; input/output protection), this will not affect the receiver provided the current does not exceed 20 mA. At  $V_{CC} < 4.5 \text{ V}$ ,  $R_{ON(max)}$  is not guaranteed;  $R_{ON(max)}$  can be estimated using Figs 33 and 34 in the "USER GUIDE".

Note to Application information

All values given are typical unless otherwise specified.

PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".