

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## **74HC/HCT251** 8-input multiplexer; 3-state

Product specification  
File under Integrated Circuits, IC06

December 1990

## 8-input multiplexer; 3-state

## 74HC/HCT251

## FEATURES

- True and complement outputs
- Both outputs are 3-state for further multiplexer expansion
- Multifunction capability
- Permits multiplexing from n-lines to one line
- Output capability: standard
- I<sub>CC</sub> category: MSI

## GENERAL DESCRIPTION

The 74HC/HCT251 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT251 are the logic implementations of single-pole 8-position switches with the state of three select inputs (S<sub>0</sub>, S<sub>1</sub>, S<sub>2</sub>) controlling the switch positions. Assertion (Y) and negation ( $\bar{Y}$ ) outputs are both provided. The output enable input ( $\bar{OE}$ ) is active LOW. The logic function provided at the output, when activated, is:

$$Y = \bar{OE} \cdot (I_0 \cdot \bar{S}_0 \cdot \bar{S}_1 \cdot \bar{S}_2 + I_1 \cdot S_0 \cdot \bar{S}_1 \cdot \bar{S}_2 + I_2 \cdot \bar{S}_0 \cdot S_1 \cdot \bar{S}_2 + I_3 \cdot S_0 \cdot S_1 \cdot \bar{S}_2 + I_4 \cdot \bar{S}_0 \cdot \bar{S}_1 \cdot S_2 + I_5 \cdot S_0 \cdot \bar{S}_1 \cdot S_2 + I_6 \cdot \bar{S}_0 \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2)$$

Both outputs are in the high impedance OFF-state (Z) when the output enable input is HIGH, allowing multiplexer expansion by tying the outputs.

## QUICK REFERENCE DATA

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

| SYMBOL                              | PARAMETER                                 | CONDITIONS                                    | TYPICAL |     | UNIT |
|-------------------------------------|---|---|---------|-----|------|
|                                     |   |   | HC      | HCT |      |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay                         | C <sub>L</sub> = 15 pF; V <sub>CC</sub> = 5 V |         |     |      |
|                                     | I <sub>n</sub> to Y                       |   | 15      | 19  | ns   |
|                                     | I <sub>n</sub> to $\bar{Y}$               |   | 17      | 19  | ns   |
|                                     | S <sub>n</sub> to Y                       |   | 20      | 20  | ns   |
|                                     | S <sub>n</sub> to $\bar{Y}$               |   | 21      | 21  | ns   |
| C <sub>I</sub>                      | input capacitance                         |   | 3.5     | 3.5 | pF   |
| C <sub>PD</sub>                     | power dissipation capacitance per package | notes 1 and 2                                 | 44      | 46  | pF   |

## Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz

f<sub>o</sub> = output frequency in MHz

∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in V

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> – 1.5 V

## ORDERING INFORMATION

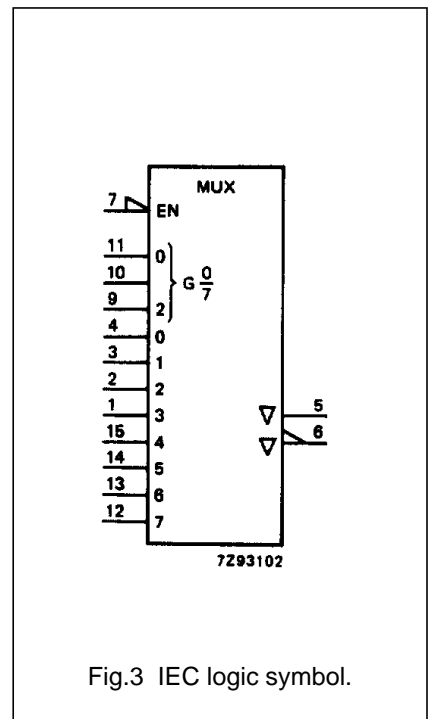
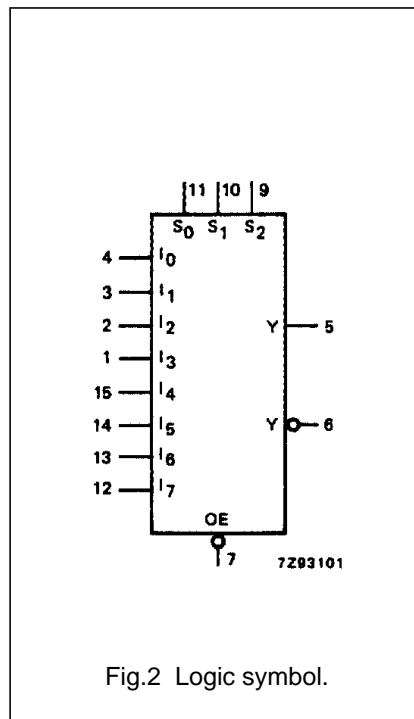
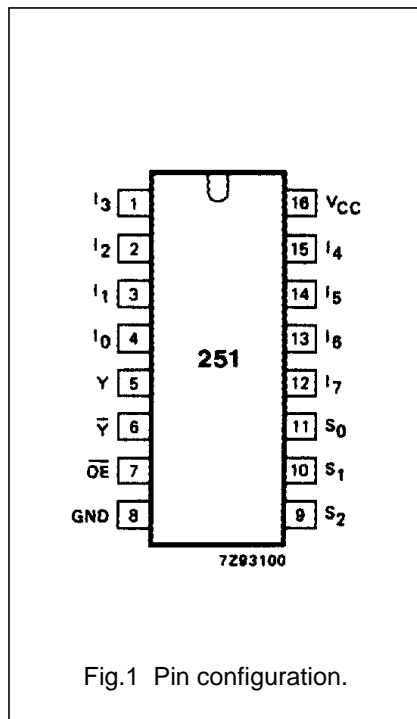
See "74HC/HCT/HCU/HCMOS Logic Package Information".

8-input multiplexer; 3-state

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PIN DESCRIPTION

| PIN NO.                    | SYMBOL          | NAME AND FUNCTION                        |
|----------------------------|-----------------|--|
| 4, 3, 2, 1, 15, 14, 13, 12 | $I_0$ to $I_7$  | multiplexer inputs                       |
| 5                          | Y               | multiplexer output                       |
| 6                          | $\bar{Y}$       | complementary multiplexer output         |
| 7                          | $\overline{OE}$ | 3-state output enable input (active LOW) |
| 8                          | GND             | ground (0 V)                             |
| 11, 10, 9                  | $S_0, S_1, S_2$ | select inputs                            |
| 16                         | $V_{CC}$        | positive supply voltage                  |



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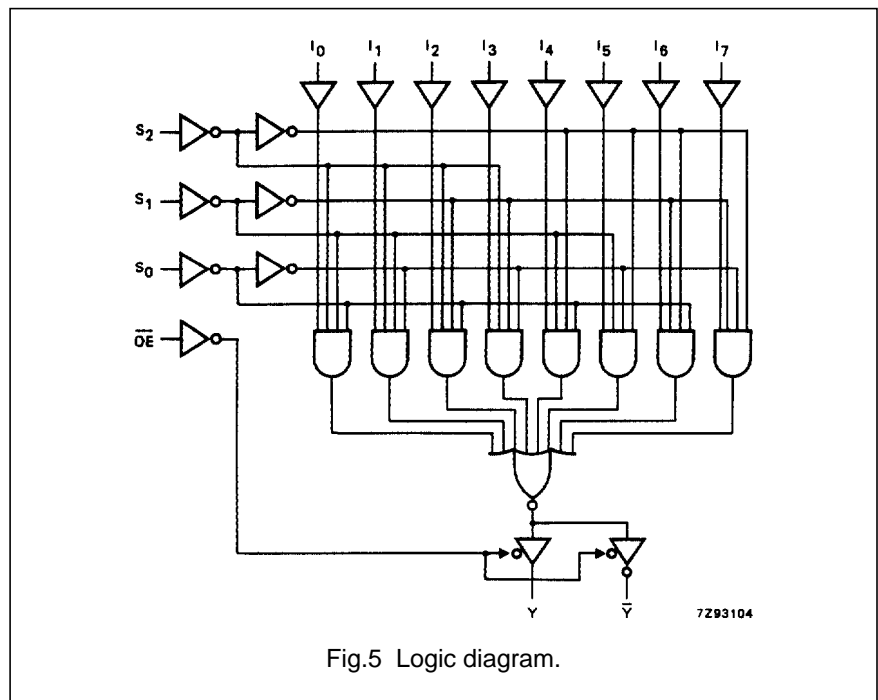
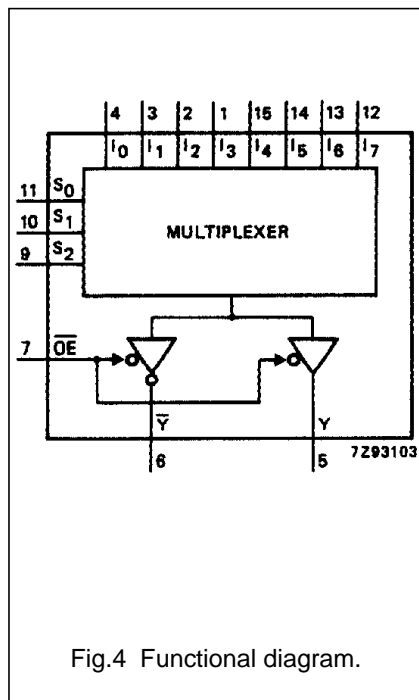
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FUNCTION TABLE

| INPUTS          |       |       |       |       |       |       |       |       |       |       |       | OUTPUTS        |   |
|-----------------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|----------------|---|
| $\overline{OE}$ | $S_2$ | $S_1$ | $S_0$ | $I_0$ | $I_1$ | $I_2$ | $I_3$ | $I_4$ | $I_5$ | $I_6$ | $I_7$ | $\overline{Y}$ | Y |
| H               | X     | X     | X     | X     | X     | X     | X     | X     | X     | X     | X     | Z              | Z |
| L               | L     | L     | L     | L     | X     | X     | X     | X     | X     | X     | X     | H              | L |
| L               | L     | L     | L     | H     | X     | X     | X     | X     | X     | X     | X     | L              | H |
| L               | L     | L     | H     | X     | L     | X     | X     | X     | X     | X     | X     | H              | L |
| L               | L     | L     | H     | X     | H     | X     | X     | X     | X     | X     | X     | L              | H |
| L               | L     | H     | L     | X     | X     | L     | X     | X     | X     | X     | X     | H              | L |
| L               | L     | H     | L     | X     | X     | H     | X     | X     | X     | X     | X     | L              | H |
| L               | L     | H     | H     | X     | X     | X     | L     | X     | X     | X     | X     | H              | L |
| L               | L     | H     | H     | X     | X     | X     | H     | X     | X     | X     | X     | L              | H |
| L               | H     | L     | L     | X     | X     | X     | X     | L     | X     | X     | X     | H              | L |
| L               | H     | L     | L     | X     | X     | X     | X     | H     | X     | X     | X     | L              | H |
| L               | H     | L     | H     | X     | X     | X     | X     | X     | L     | X     | X     | H              | L |
| L               | H     | L     | H     | X     | X     | X     | X     | X     | H     | X     | X     | L              | H |
| L               | H     | H     | L     | X     | X     | X     | X     | X     | X     | L     | X     | H              | L |
| L               | H     | H     | L     | X     | X     | X     | X     | X     | X     | H     | X     | L              | H |
| L               | H     | H     | H     | X     | X     | X     | X     | X     | X     | X     | L     | H              | L |
| L               | H     | H     | H     | X     | X     | X     | X     | X     | X     | X     | H     | L              | H |

Note

- H = HIGH voltage level  
L = LOW voltage level  
X = don't care  
Z = high impedance OFF-state



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**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

| SYMBOL                              | PARAMETER  | T <sub>amb</sub> (°C) |                |                 |            |                 |             | UNIT            | TEST CONDITIONS        |                   |              |
|-------------------------------------|--|-----------------------|----------------|-----------------|------------|-----------------|-------------|-----------------|------------------------|-------------------|--------------|
|                                     |  | 74HC                  |                |                 |            |                 |             |                 | V <sub>CC</sub><br>(V) | WAVEFORMS         |              |
|                                     |  | +25                   |                |                 | -40 to +85 |                 | -40 to +125 |                 |                        |                   |              |
|                                     |  | min.                  | typ.           | max.            | min.       | max.            | min.        |                 |                        |                   | max.         |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>I <sub>n</sub> to Y                       |                       | 50<br>18<br>14 | 170<br>34<br>29 |            | 215<br>43<br>37 |             | 255<br>51<br>43 | ns                     | 2.0<br>4.5<br>6.0 | Fig.6        |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>I <sub>n</sub> to $\bar{Y}$               |                       | 55<br>20<br>16 | 175<br>35<br>30 |            | 220<br>44<br>37 |             | 265<br>53<br>45 | ns                     | 2.0<br>4.5<br>6.0 | Fig.7        |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>S <sub>n</sub> to Y                       |                       | 66<br>24<br>19 | 205<br>41<br>35 |            | 255<br>51<br>43 |             | 310<br>62<br>53 | ns                     | 2.0<br>4.5<br>6.0 | Fig.6        |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>S <sub>n</sub> to $\bar{Y}$               |                       | 69<br>25<br>20 | 205<br>41<br>35 |            | 255<br>51<br>43 |             | 310<br>62<br>53 | ns                     | 2.0<br>4.5<br>6.0 | Fig.7        |
| t <sub>PZH</sub> / t <sub>PZL</sub> | 3-state output enable time<br>$\overline{OE}$ to Y, $\bar{Y}$  |                       | 36<br>13<br>10 | 140<br>28<br>24 |            | 175<br>35<br>30 |             | 210<br>42<br>36 | ns                     | 2.0<br>4.5<br>6.0 | Fig.7        |
| t <sub>PHZ</sub> / t <sub>PLZ</sub> | 3-state output disable time<br>$\overline{OE}$ to Y, $\bar{Y}$ |                       | 39<br>14<br>11 | 140<br>28<br>24 |            | 170<br>35<br>30 |             | 210<br>42<br>36 | ns                     | 2.0<br>4.5<br>6.0 | Fig.7        |
| t <sub>THL</sub> / t <sub>TLH</sub> | output transition time   |                       | 19<br>7<br>6   | 75<br>15<br>13  |            | 95<br>19<br>16  |             | 110<br>22<br>19 | ns                     | 2.0<br>4.5<br>6.0 | Figs 6 and 7 |

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**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications.

To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

| INPUT                           | UNIT LOAD COEFFICIENT |
|---------------------------------|-----------------------|
| I <sub>n</sub>                  | 1.00                  |
| S <sub>0</sub>                  | 1.50                  |
| S <sub>1</sub> , S <sub>2</sub> | 1.50                  |
| $\overline{OE}$                 | 1.50                  |

**AC CHARACTERISTICS FOR HCT**

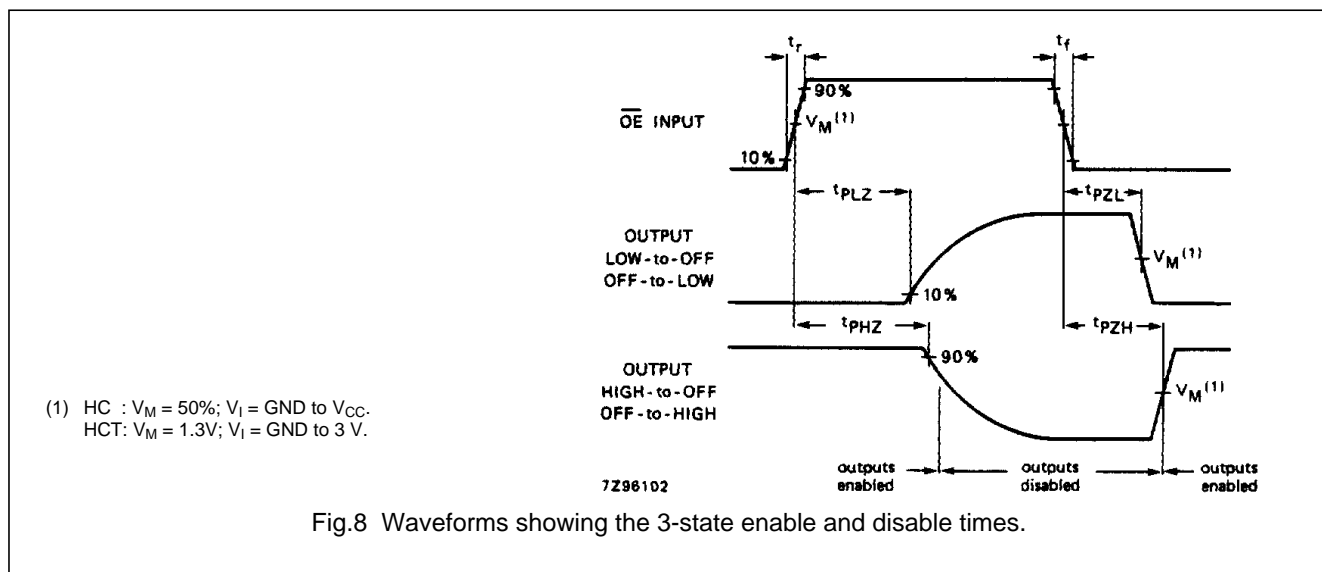
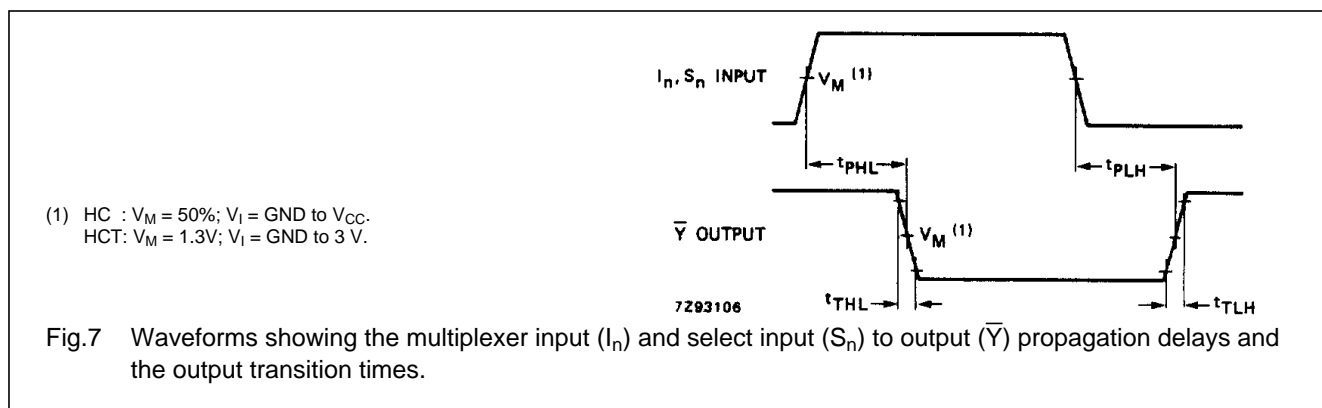
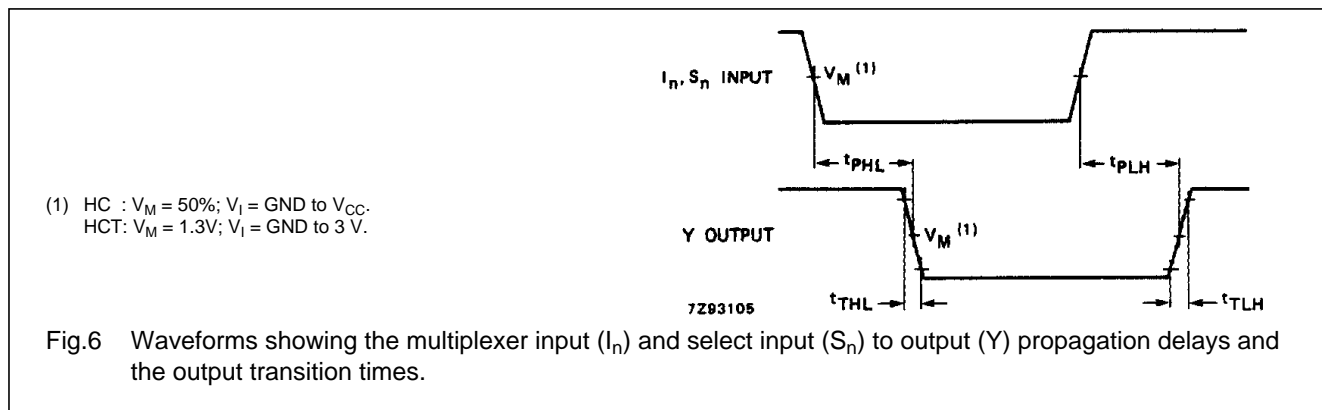
GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

| SYMBOL                              | PARAMETER   | T <sub>amb</sub> (°C) |      |      |            |      |             |      | UNIT | TEST CONDITIONS        |              |
|-------------------------------------|---|-----------------------|------|------|------------|------|-------------|------|------|------------------------|--------------|
|                                     |   | 74HCT                 |      |      |            |      |             |      |      | V <sub>CC</sub><br>(V) | WAVEFORMS    |
|                                     |   | +25                   |      |      | -40 to +85 |      | -40 to +125 |      |      |                        |              |
|                                     |   | min.                  | typ. | max. | min.       | max. | min.        | max. |      |                        |              |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>I <sub>n</sub> to Y                            |                       | 22   | 35   |            | 44   |             | 53   | ns   | 4.5                    | Fig.6        |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>I <sub>n</sub> to $\overline{Y}$               |                       | 22   | 35   |            | 44   |             | 53   | ns   | 4.5                    | Fig.7        |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>S <sub>n</sub> to Y                            |                       | 24   | 44   |            | 55   |             | 66   | ns   | 4.5                    | Fig.6        |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>S <sub>n</sub> to $\overline{Y}$               |                       | 25   | 44   |            | 55   |             | 66   | ns   | 4.5                    | Fig.7        |
| t <sub>PZH</sub> / t <sub>PZL</sub> | 3-state output enable time<br>$\overline{OE}$ to Y, $\overline{Y}$  |                       | 13   | 28   |            | 35   |             | 42   | ns   | 4.5                    | Fig.7        |
| t <sub>PHZ</sub> / t <sub>PLZ</sub> | 3-state output disable time<br>$\overline{OE}$ to Y, $\overline{Y}$ |                       | 14   | 28   |            | 35   |             | 42   | ns   | 4.5                    | Fig.7        |
| t <sub>THL</sub> / t <sub>TLH</sub> | output transition time  |                       | 7    | 15   |            | 19   |             | 22   | ns   | 4.5                    | Figs 6 and 7 |

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AC WAVEFORMS



PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".