

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT4316 Quad bilateral switches

Product specification
File under Integrated Circuits, IC06

September 1993

Quad bilateral switches

74HC/HCT4316

FEATURES

- Low “ON” resistance:
160 Ω (typ.) at $V_{CC} - V_{EE} = 4.5$ V
120 Ω (typ.) at $V_{CC} - V_{EE} = 6.0$ V
80 Ω (typ.) at $V_{CC} - V_{EE} = 9.0$ V
- Logic level translation:
to enable 5 V logic to communicate
with ± 5 V analog signals
- Typical “break before make” built in
- Output capability: non-standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4316 are high-speed Si-gate CMOS devices. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4316 have four independent analog switches. Each switch has two input/output terminals (nY, nZ) and an active HIGH select input (nS). When the enable input (\bar{E}) is HIGH, all four analog switches are turned off.

Current through a switch will not cause additional V_{CC} current provided the voltage at the terminals of the switch is maintained within the supply voltage range; $V_{CC} \gg (V_Y, V_Z) \gg V_{EE}$. Inputs nY and nZ are electrically equivalent terminals.

V_{CC} and GND are the supply voltage pins for the digital control inputs (\bar{E} and nS). The V_{CC} to GND ranges are 2.0 to 10.0 V for HC and 4.5 to 5.5 V for HCT.

The analog inputs/outputs (nY and nZ) can swing between V_{CC} as a positive limit and V_{EE} as a negative limit. $V_{CC} - V_{EE}$ may not exceed 10.0 V.

See the “4016” for the version without logic level translation.

QUICK REFERENCE DATA

$V_{EE} = \text{GND} = 0$ V; $T_{\text{amb}} = 25$ °C; $t_r = t_f = 6$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PZH}	turn “ON” time \bar{E} to V_{OS} nS to V_{OS}	$C_L = 15$ pF; $R_L = 1$ k Ω ; $V_{CC} = 5$ V	19	19	ns
			16	17	ns
t_{PZL}	turn “ON” time \bar{E} to V_{OS} nS to V_{OS}		19	24	ns
			16	21	ns
t_{PHZ}/t_{PLZ}	turn “OFF” time \bar{E} to V_{OS} nS to V_{OS}		20	21	ns
			16	19	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per switch	notes 1 and 2	13	14	pF
C_S	max. switch capacitance		5	5	pF

Notes

- C_{PD} is used to determine the dynamic power dissipation (P_D in μ W):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum \{ (C_L + C_S) \times V_{CC}^2 \times f_o \}$$
 where:
 f_i = input frequency in MHz
 f_o = output frequency in MHz
 $\sum \{ (C_L + C_S) \times V_{CC}^2 \times f_o \}$ = sum of outputs

C_L = output load capacitance in pF

C_S = max. switch capacitance in pF

V_{CC} = supply voltage in V

- For HC the condition is $V_I = \text{GND}$ to V_{CC}
For HCT the condition is $V_I = \text{GND}$ to $V_{CC} - 1.5$ V

Quad bilateral switches

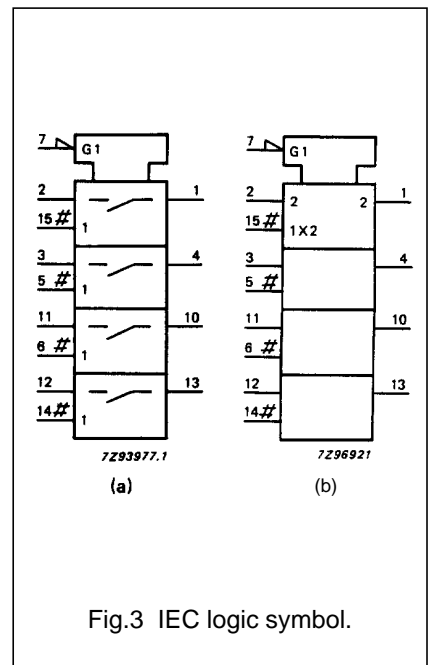
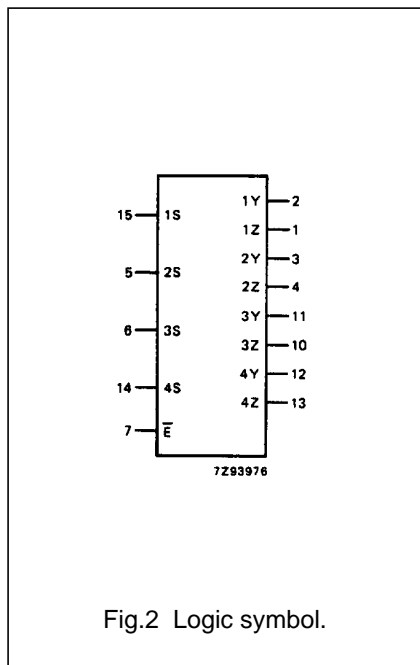
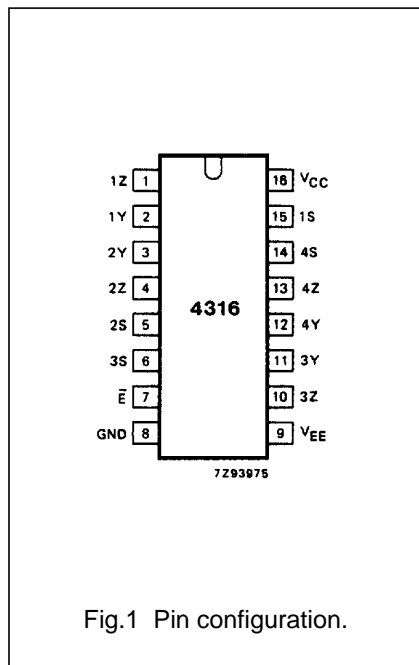
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ORDERING INFORMATION

See "74HC/HCT/HCU/HCMOS Logic Package Information".

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 10, 13	1Z to 4Z	independent inputs/outputs
2, 3, 11, 12	1Y to 4Y	independent inputs/outputs
7	\bar{E}	enable input (active LOW)
8	GND	ground (0 V)
9	V_{EE}	negative supply voltage
15, 5, 6, 14	1S to 4S	select inputs (active HIGH)
16	V_{CC}	positive supply voltage



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FUNCTION TABLE

INPUTS		SWITCH
\bar{E}	nS	
L	L	off
L	H	on
H	X	off

Note

- H = HIGH voltage level
L = LOW voltage level
X = don't care

APPLICATIONS

- Signal gating
- Modulation
- Demodulation
- Chopper

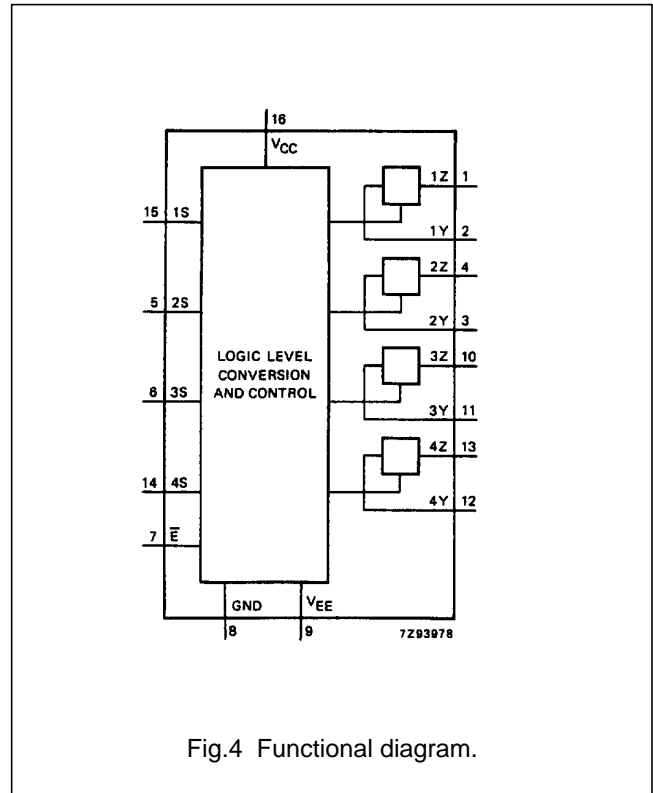


Fig.4 Functional diagram.

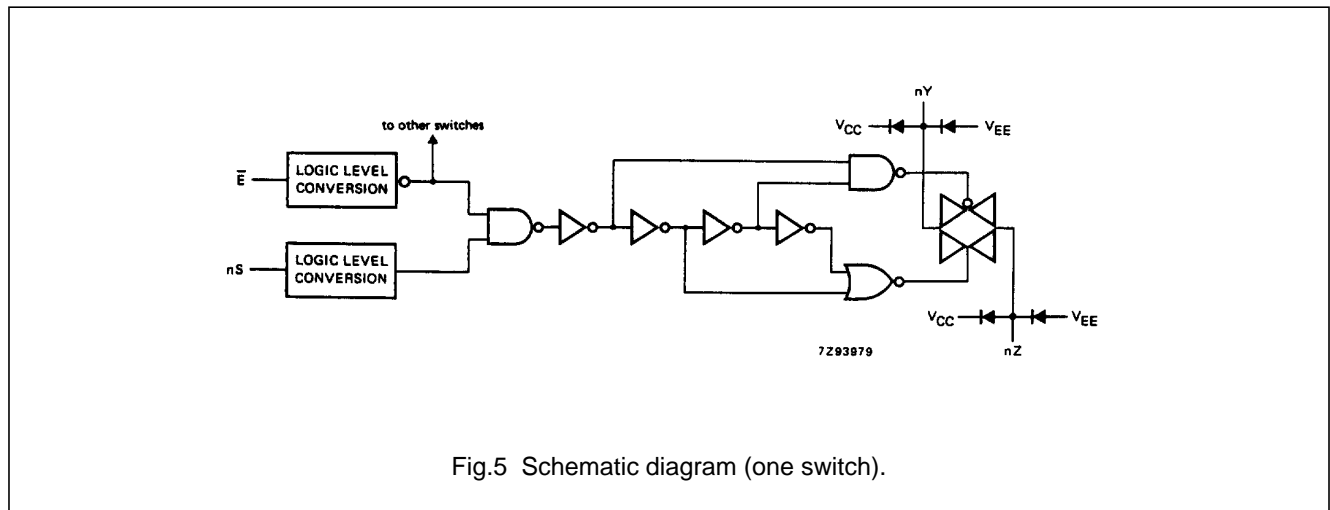


Fig.5 Schematic diagram (one switch).

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RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to $V_{EE} = \text{GND}$ (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	-0.5	+11.0	V	
$\pm I_{IK}$	DC digital input diode current		20	mA	for $V_I < -0.5 \text{ V}$ or $V_I > V_{CC} + 0.5 \text{ V}$
$\pm I_{SK}$	DC switch diode current		20	mA	for $V_S < -0.5 \text{ V}$ or $V_S > V_{CC} + 0.5 \text{ V}$
$\pm I_S$	DC switch current		25	mA	for $-0.5 \text{ V} < V_S < V_{CC} + 0.5 \text{ V}$
$\pm I_{EE}$	DC V_{EE} current		20	mA	
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	-65	+150	°C	
P_{tot}	power dissipation per package				for temperature range: -40 to +125 °C 74HC/HCT
	plastic DIL		750	mW	above +70 °C: derate linearly with 12 mW/K
	plastic mini-pack (SO)		500	mW	above +70 °C: derate linearly with 8 mW/K
P_S	power dissipation per switch		100	mW	

Note to ratings

To avoid drawing V_{CC} current out of terminal Z, when switch current flows in terminals Y_n , the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminals Z, no V_{CC} current will flow out of terminal Y_n . In this case there is no limit for the voltage drop across the switch, but the voltages at Y_n and Z may not exceed V_{CC} or V_{EE} .

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74HC			74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage $V_{CC}-\text{GND}$	2.0	5.0	10.0	4.5	5.0	5.5	V	see Figs 6 and 7
V_{CC}	DC supply voltage $V_{CC}-V_{EE}$	2.0	5.0	10.0	2.0	5.0	10.0	V	see Figs 6 and 7
V_I	DC input voltage range	GND		V_{CC}	GND		V_{CC}	V	
V_S	DC switch voltage range	V_{EE}		V_{CC}	V_{EE}		V_{CC}	V	
T_{amb}	operating ambient temperature range	-40		+85	-40		+85	°C	see DC and AC CHARACTERISTICS
T_{amb}	operating ambient temperature range	-40		+125	-40		+125	°C	
t_r, t_f	input rise and fall times		6.0	1000 500 400 250		6.0	500	ns	$V_{CC} = 2.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 6.0 \text{ V}$ $V_{CC} = 10.0 \text{ V}$

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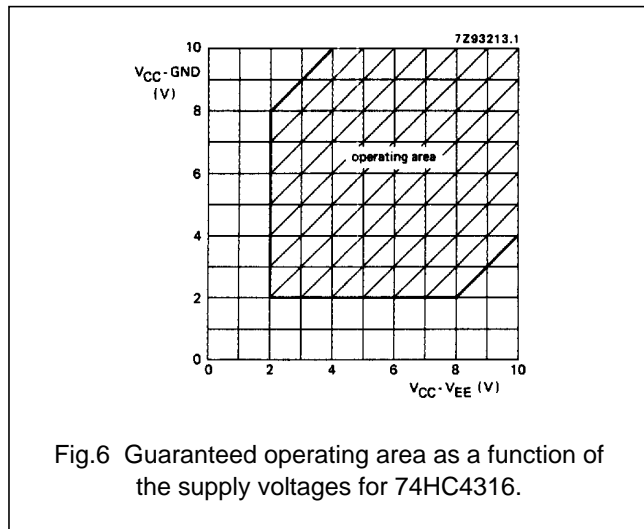


Fig.6 Guaranteed operating area as a function of the supply voltages for 74HC4316.

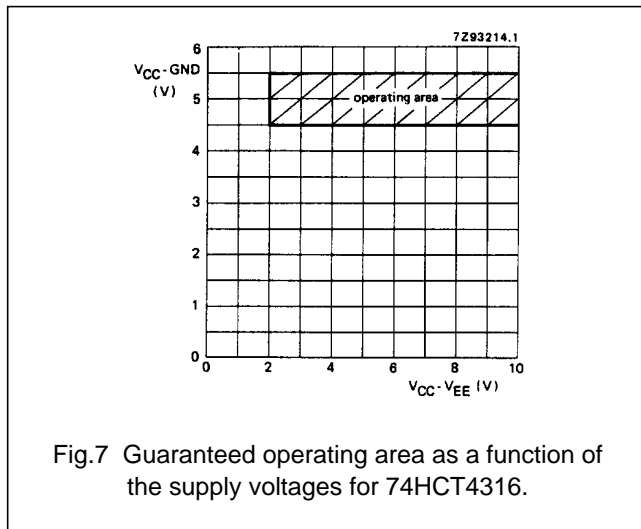


Fig.7 Guaranteed operating area as a function of the supply voltages for 74HCT4316.

DC CHARACTERISTICS FOR 74HC/HCT

For 74HC: $V_{CC} - GND$ or $V_{CC} - V_{EE} = 2.0, 4.5, 6.0$ and 9.0 V

For 74HCT: $V_{CC} - GND = 4.5$ and 5.5 V; $V_{CC} - V_{EE} = 2.0, 4.5, 6.0$ and 9.0 V

SYMBOL	PARAMETER	T_{amb} (°C)						UNIT	TEST CONDITIONS					
		74HC/HCT							V_{CC} (V)	V_{EE} (V)	I_S (μA)	V_{is}	V_I	
		+25			-40 to +85		-40 to +125							
		min.	typ.	max.	min.	max.	min.							max.
R_{ON}	ON resistance (peak)		—	—		—		—	Ω	2.0	0	100	V_{CC} to V_{EE}	V_{IH} or V_{IL}
			160	320		400		480	Ω	4.5	0	1000		
			120	240		300		360	Ω	6.0	0	1000		
			85	170		215		255	Ω	4.5	-4.5	1000		
R_{ON}	ON resistance (rail)		160	—		—		—	Ω	2.0	0	100	V_{EE}	V_{IH} or V_{IL}
			80	160		200		240	Ω	4.5	0	1000		
			70	140		175		210	Ω	6.0	0	1000		
			60	120		150		180	Ω	4.5	-4.5	1000		
R_{ON}	ON resistance (rail)		170	—		—		—	Ω	2.0	0	100	V_{CC}	V_{IH} or V_{IL}
			90	180		225		270	Ω	4.5	0	1000		
			80	160		200		240	Ω	6.0	0	1000		
			65	135		170		205	Ω	4.5	-4.5	1000		
ΔR_{ON}	maximum ΔON resistance between any two channels		—						Ω	2.0	0		V_{CC} to V_{EE}	V_H or V_{IL}
			16						Ω	4.5	0			
			9						Ω	6.0	0			
			6						Ω	4.5	-4.5			

Notes

- At supply voltages ($V_{CC} - V_{EE}$) approaching 2.0 V the analog switch ON-resistance becomes extremely non-linear. Therefore it is recommended that these devices are used to transmit digital signals only, when using these supply voltages.
- For test circuit measuring R_{ON} see Fig.8.

Quad bilateral switches

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DC CHARACTERISTICS FOR 74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS			
		74HC								V_{CC} (V)	V_{EE} (V)	V_I	OTHER
		+25			-40 to +85		-40 to +125						
		min.	typ.	max.	min.	max.	min.	max.					
V_{IH}	HIGH level input voltage	1.5 3.15 4.2 6.3	1.2 2.4 3.2 4.3		1.5 3.15 4.2 6.3		1.5 3.15 4.2 6.3		V	2.0 4.5 6.0 9.0			
V_{IL}	LOW level input voltage		0.8 2.1 2.8 4.3	0.5 1.35 1.8 2.7		0.5 1.35 1.8 2.7	0.5 1.35 1.8 2.7	V	2.0 4.5 6.0 9.0				
$\pm I_I$	input leakage current			0.1 0.2		1.0 2.0	1.0 2.0	μA	6.0 10.0	0 0	V_{CC} or GND		
$\pm I_S$	analog switch OFF-state current			0.1		1.0	1.0	μA	10.0	0	V_{IH} or V_{IL}	$ V_S = V_{CC} - V_{EE}$ (see Fig.10)	
$\pm I_S$	analog switch ON-state current			0.1		1.0	1.0	μA	10.0	0	V_{IH} or V_{IL}	$ V_S = V_{CC} - V_{EE}$ (see Fig.11)	
I_{CC}	quiescent supply current			8.0 16.0		80.0 160.0	160.0 320.0	μA	6.0 10.0	0 0	V_{CC} or GND	$V_{IS} = V_{EE}$ or V_{CC} ; $V_{OS} = V_{CC}$ or V_{EE}	

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AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)						UNIT	TEST CONDITIONS			
		74HC							V_{CC} (V)	V_{EE} (V)	OTHER	
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.		max.			
t_{PHL}/t_{PLH}	propagation delay V_{is} to V_{os}		17 6 5 4	60 12 10 8		75 15 13 10		90 18 15 12	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = \infty$; $C_L = 50$ pF (see Fig.18)
t_{PZH}/t_{PZL}	turn "ON" time \bar{E} to V_{os}		61 22 18 19	205 41 35 37		255 51 43 47		310 62 53 56	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1$ k Ω ; $C_L = 50$ pF (see Figs 19, 20 and 21)
t_{PZH}/t_{PZL}	turn "ON" time nS to V_{os}		52 19 15 17	175 35 30 34		220 44 37 43		265 53 45 51	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1$ k Ω ; $C_L = 50$ pF (see Figs 19, 20 and 21)
t_{PHZ}/t_{PLZ}	turn "OFF" time \bar{E} to V_{os}		63 23 18 21	220 44 37 39		275 55 47 49		330 66 56 59	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1$ k Ω ; $C_L = 50$ pF (see Figs 19, 20 and 21)
t_{PHZ}/t_{PLZ}	turn "OFF" time nS to V_{os}		55 20 16 18	175 35 30 36		220 44 37 45		265 53 45 54	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1$ k Ω ; $C_L = 50$ pF (see Figs 19, 20 and 21)

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DC CHARACTERISTICS FOR 74HCT

Voltages are referenced to GND (ground = 0)

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS			
		74HCT								V _{CC} (V)	V _{EE} (V)	V _I	OTHER
		+25			-40 to +85		-40 to +125						
		min.	typ.	max.	min.	max.	min.	max.					
V _{IH}	HIGH level input voltage	2.0	1.6		2.0		2.0		V	4.5 to 5.5			
V _{IL}	LOW level input voltage		1.2	0.8		0.8		0.8	V	4.5 to 5.5			
±I _I	input leakage current			0.1		1.0		1.0	µA	5.5	0	V _{CC} or GND	
±I _S	analog switch OFF-state current			0.1		1.0		1.0	µA	10.0	0	V _{IH} or V _{IL}	V _S = V _{CC} - V _{EE} (see Fig.10)
±I _S	analog switch ON-state current			0.1		1.0		1.0	µA	10.0	0	V _{IH} or V _{IL}	V _S = V _{CC} - V _{EE} (see Fig.11)
I _{CC}	quiescent supply current			8.0 16.0		80.0 160.0		160.0 320.0	µA	5.5 5.0	0 -5.0	V _{CC} or GND	V _{is} = V _{EE} or V _{CC} ; V _{OS} = V _{CC} or V _{EE}
ΔI _{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	µA	4.5 to 5.5	0	V _{CC} -2.1 V	other inputs at V _{CC} or GND

Note

- The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given here. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nS	0.50
\bar{E}	0.50

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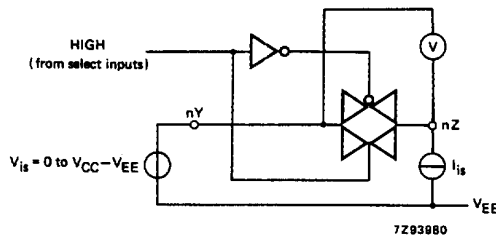


Fig.8 Test circuit for measuring R_{ON} .

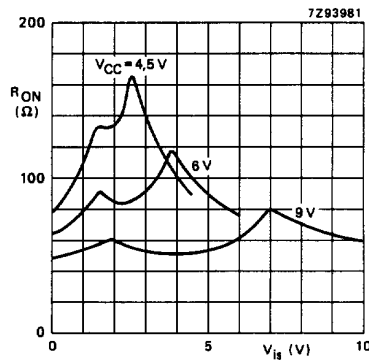


Fig.9 Typical R_{ON} as a function of input voltage V_{is} for $V_{is} = 0$ to $V_{CC} - V_{EE}$.

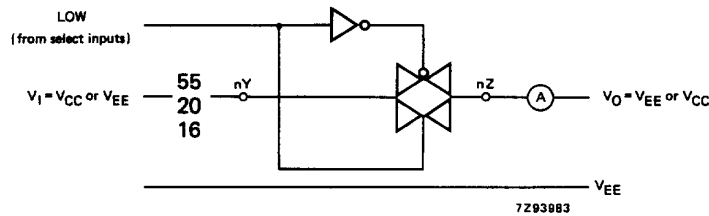


Fig.10 Test circuit for measuring OFF-state current.

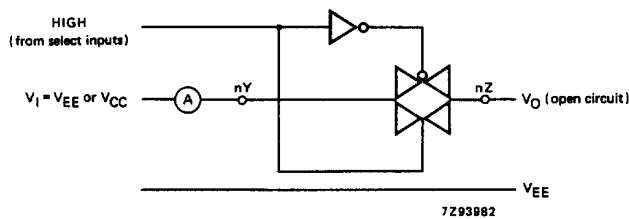


Fig.11 Test circuit for measuring ON-state current.

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AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)								UNIT	TEST CONDITIONS		
		74HCT									V_{CC} (V)	V_{EE} (V)	OTHER
		+25			-40 TO +85		-40 to +125						
		min.	typ.	max.	min.	max.	min.	max.					
t_{PHL}/t_{PLH}	propagation delay V_{is} to V_{os}		6 4	12 8		15 10		18 12	ns	4.5 4.5	0 -4.5	$R_L = \infty$; $C_L = 50$ pF (see Fig.18)	
t_{PZH}	turn "ON" time \bar{E} to V_{os}		22 21	44 42		55 53		66 63	ns	4.5 4.5	0 -4.5	$R_L = 1$ k Ω ; $C_L = 50$ pF (see Figs 19, 20 and 21)	
t_{PZL}	turn "ON" time \bar{E} to V_{os}		28 21	56 42		70 53		84 63	ns	4.5 4.5	0 -4.5	(see Figs 19, 20 and 21)	
t_{PZH}	turn "ON" time nS to V_{os}		20 17	40 34		53 43		60 51	ns	4.5 4.5	0 -4.5	$R_L = 1$ k Ω ; $C_L = 50$ pF (see Figs 19, 20 and 21)	
t_{PZL}	turn "ON" time nS to V_{os}		25 17	50 34		63 43		75 51	ns	4.5 4.5	0 -4.5	(see Figs 19, 20 and 21)	
t_{PHZ}/t_{PLZ}	turn "OFF" time \bar{E} to V_{os}		25 23	50 46		63 58		75 69	ns	4.5 4.5	0 -4.5	$R_L = 1$ k Ω ; $C_L = 50$ pF (see Figs 19, 20 and 21)	
t_{PHZ}/t_{PLZ}	turn "OFF" time nS to V_{os}		22 20	44 40		55 50		66 60	ns	4.5 4.5	0 -4.5	$R_L = 1$ k Ω ; $C_L = 50$ pF (see Figs 19, 20 and 21)	

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ADDITIONAL AC CHARACTERISTICS FOR 74HC/HCT

Recommended conditions and typical values

GND = 0 V; T_{amb} = 25 °C

SYMBOL	PARAMETER	typ.	UNIT	V _{CC} (V)	V _{EE} (V)	V _{is(p-p)} (V)	CONDITIONS
	sine-wave distortion f = 1 kHz	0.80 0.40	% %	2.25 4.5	-2.25 -4.5	4.0 8.0	R _L = 10 kΩ; C _L = 50 pF (see Fig.14)
	sine-wave distortion f = 10 kHz	2.40 1.20	% %	2.25 4.5	-2.25 -4.5	4.0 8.0	R _L = 10 kΩ; C _L = 50 pF (see Fig.14)
	switch "OFF" signal feed-through	-50 -50	dB dB	2.25 4.5	-2.25 -4.5	note 1	R _L = 600 Ω; C _L = 50 pF f = 1 MHz (see Figs 12 and 15)
	crosstalk between any two switches	-60 -60	dB dB	2.25 4.5	-2.25 -4.5	note 1	R _L = 600 Ω; C _L = 50 pF; f = 1 MHz; (see Fig.16)
V _(p-p)	crosstalk voltage between control and any switch (peak-to-peak value)	110 220	mV mV	4.5 4.5	0 -4.5		R _L = 600 kΩ; C _L = 50 pF; f = 1 MHz (\bar{E} or nS, square-wave between V _{CC} and GND, t _r = t _f = 6 ns) (see Fig.17)
f _{max}	minimum frequency response (-3 dB)	150 160	MHz MHz	2.25 4.5	-2.25 -4.5	note 2	R _L = 50 Ω; C _L = 10 pF (see Figs 13 and 14)
C _S	maximum switch capacitance	5	pF				

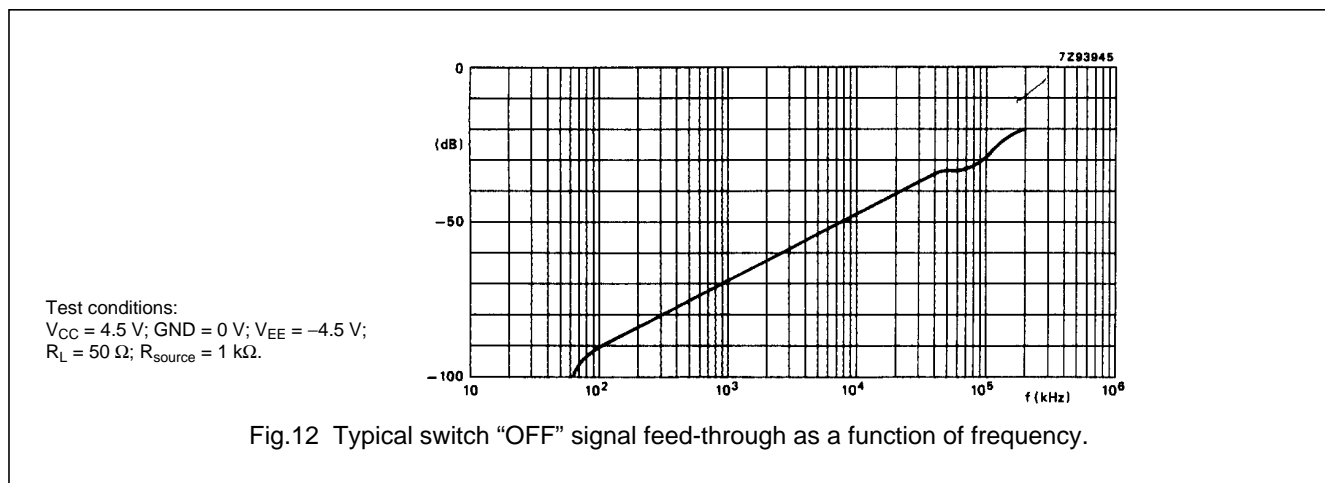
Notes

1. Adjust input voltage V_{is} to 0 dBm level (0 dBm = 1 mW into 600 Ω).
2. Adjust input voltage V_{is} to 0 dBm level at V_{OS} for 1 MHz (0 dBm = 1 mW into 50 Ω).

General note

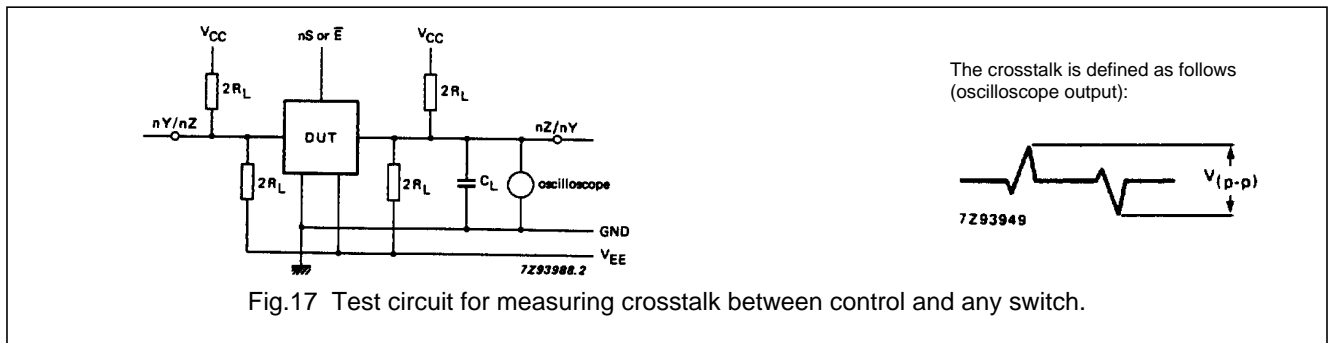
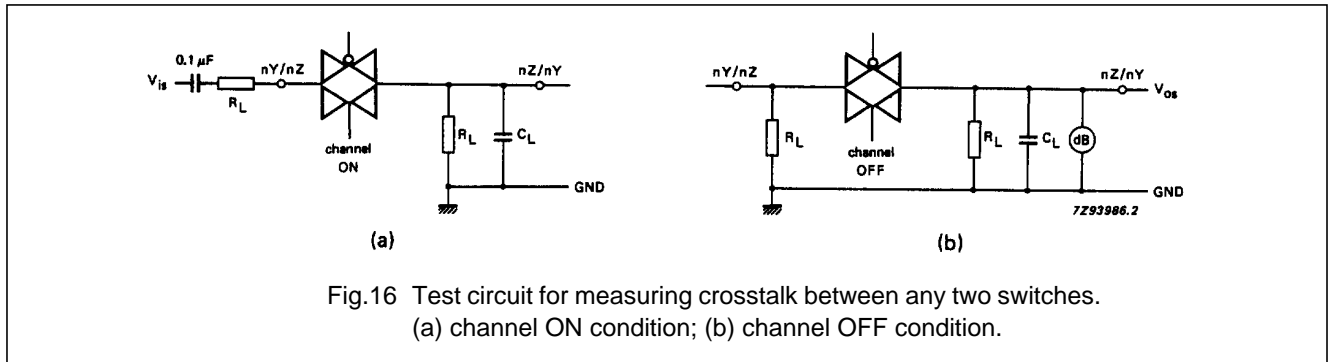
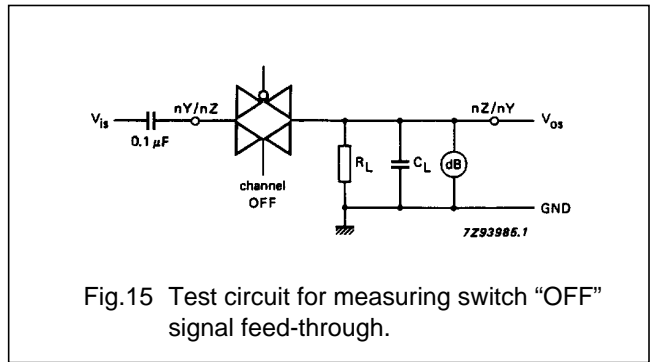
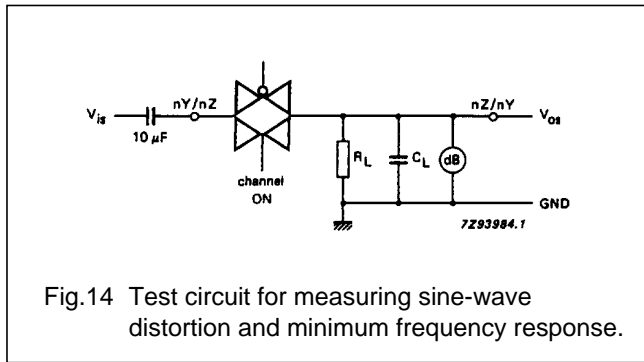
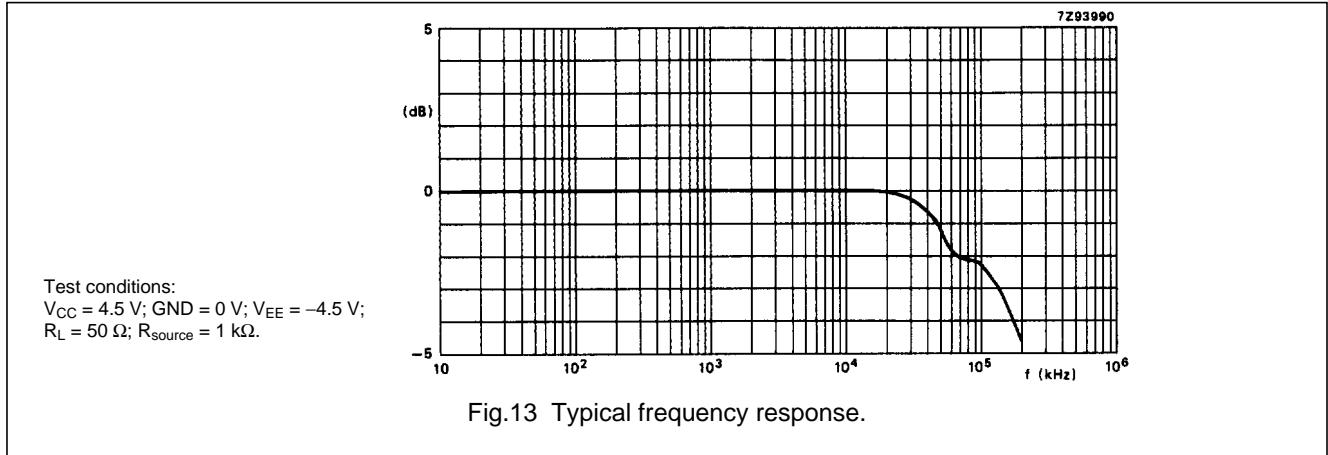
V_{is} is the input voltage at an nY or nZ terminal, whichever is assigned as an input.

V_{OS} is the output voltage at an nY or nZ terminal, whichever is assigned as an output.



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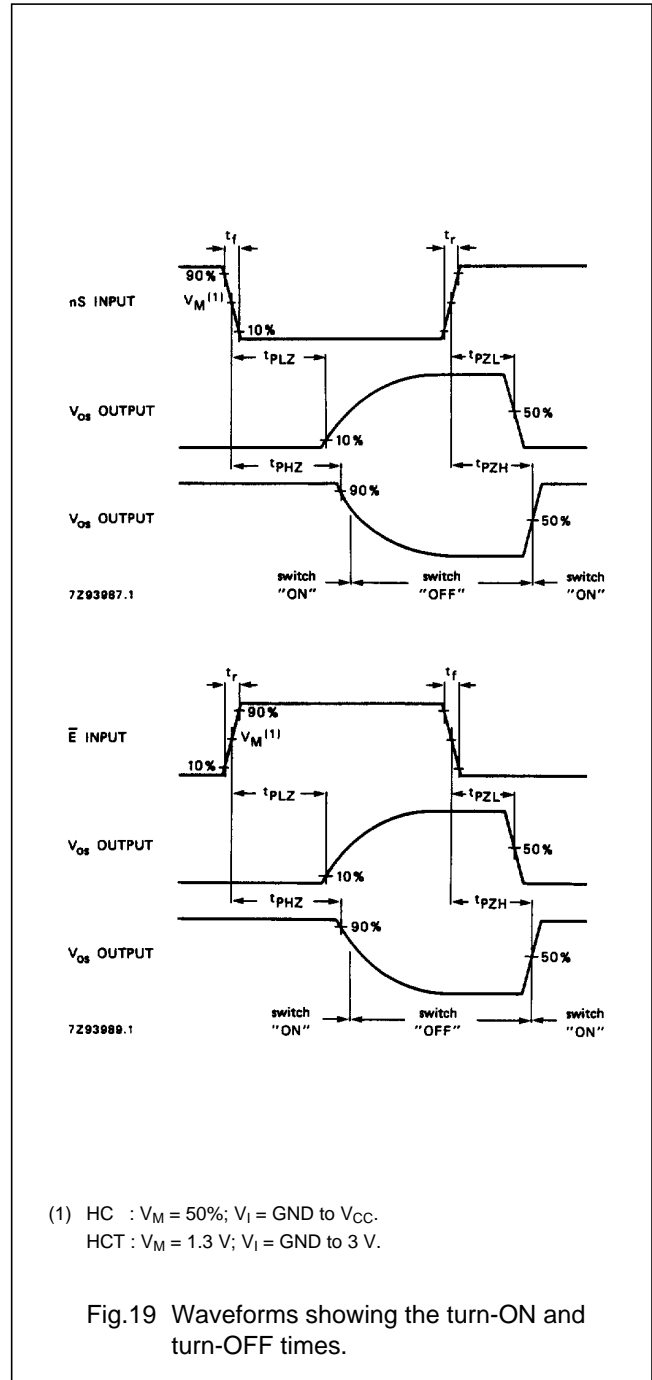
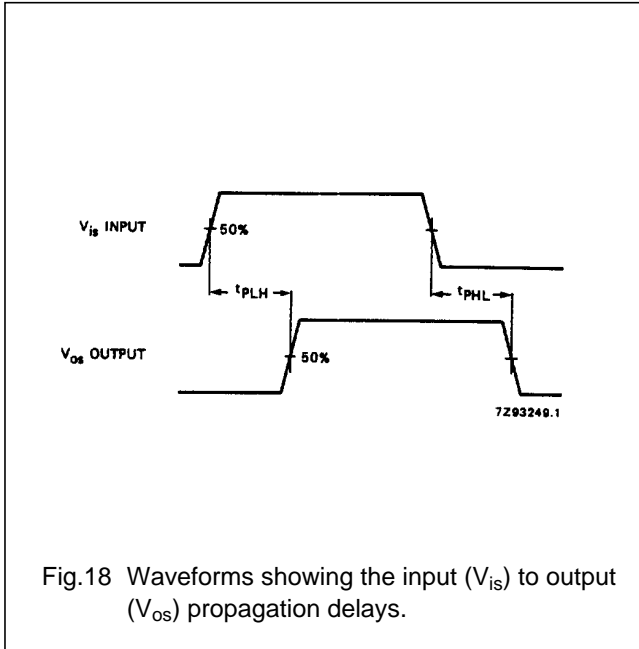
74HC/HCT4316



Quad bilateral switches

74HC/HCT4316

AC WAVEFORMS



Quad bilateral switches

74HC/HCT4316

TEST CIRCUIT AND WAVEFORMS

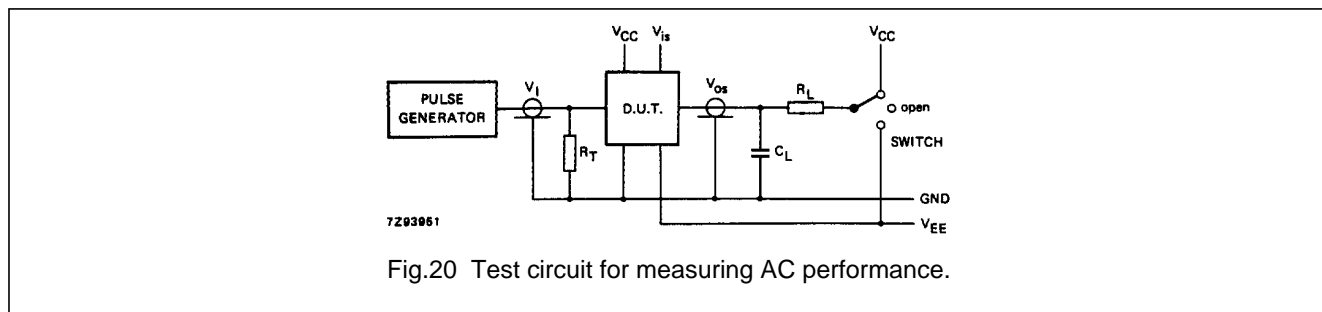


Fig.20 Test circuit for measuring AC performance.

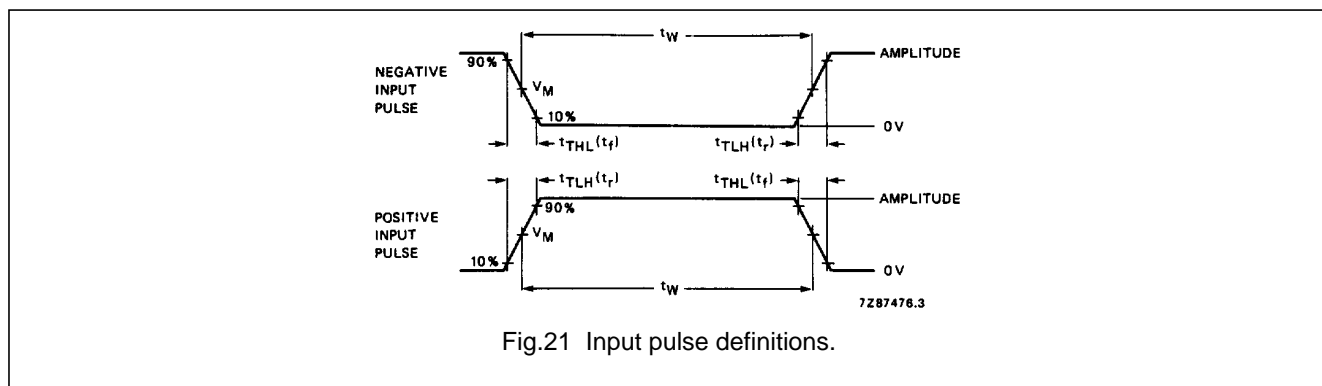


Fig.21 Input pulse definitions.

Conditions

TEST	SWITCH	V _{iss}
t _{PZH}	V _{EE}	V _{CC}
t _{PZL}	V _{CC}	V _{EE}
t _{PHZ}	V _{EE}	V _{CC}
t _{PLZ}	V _{CC}	V _{EE}
others	open	pulse

FAMILY	AMPLITUDE	V _M	t _r ; t _f	
			f _{max} ; PULSE WIDTH	OTHER
74HC	V _{CC}	50%	< 2 ns	6 ns
74HCT	3.0 V	1.3 V	< 2 ns	6 ns

Definitions for Figs 20 and 21:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint to t_r, t_f with 50% duty factor.

PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".