

74HC2G66; 74HCT2G66

Dual single-pole single-throw analog switch

Rev. 10 — 3 October 2013

Product data sheet

1. General description

The 74HC2G66; 74HCT2G66 is a dual single pole, single-throw analog switch. Each switch has two input/output terminals (nY and nZ) and a digital enable input (nE). When nE is LOW, the analog switch is turned off. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

2. Features and benefits

- Wide supply voltage range from 2.0 V to 10.0 V for 74HC2G66
- Very low ON resistance:
 - ◆ 41 Ω (typ.) at $V_{CC} = 4.5$ V
 - ◆ 30 Ω (typ.) at $V_{CC} = 6.0$ V
 - ◆ 21 Ω (typ.) at $V_{CC} = 9.0$ V
- High noise immunity
- Low power dissipation
- 25 mA continuous switch current
- Multiple package options
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to $+85$ °C and -40 °C to $+125$ °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC2G66DP 74HCT2G66DP	-40 °C to $+125$ °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
74HC2G66DC 74HCT2G66DC	-40 °C to $+125$ °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
74HC2G66GT 74HCT2G66GT	-40 °C to $+125$ °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body $1 \times 1.95 \times 0.5$ mm	SOT833-1
74HC2G66GD 74HCT2G66GD	-40 °C to $+125$ °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body $3 \times 2 \times 0.5$ mm	SOT996-2

4. Marking

Table 2. Marking codes

Type number	Marking ^[1]
74HC2G66DP	H66
74HCT2G66DP	T66
74HC2G66DC	H66
74HCT2G66DC	T66
74HC2G66GT	H66
74HCT2G66GT	T66
74HC2G66GD	H66
74HCT2G66GD	T66

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

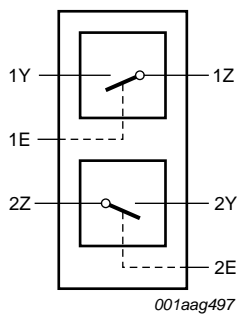


Fig 1. Logic symbol

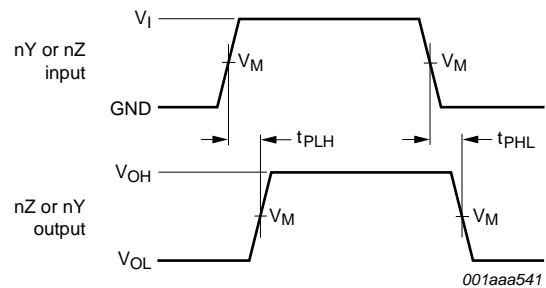
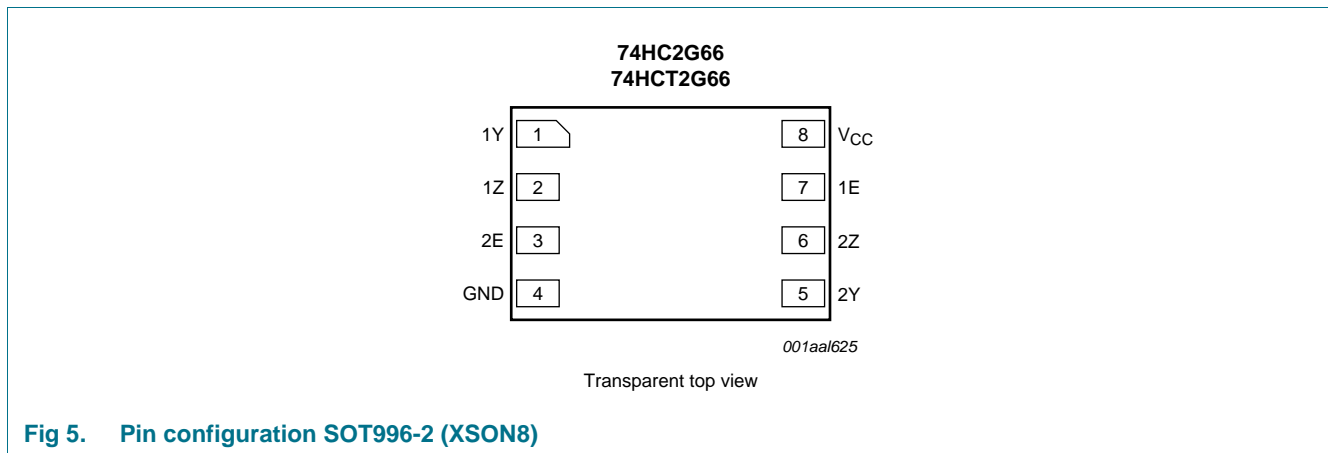
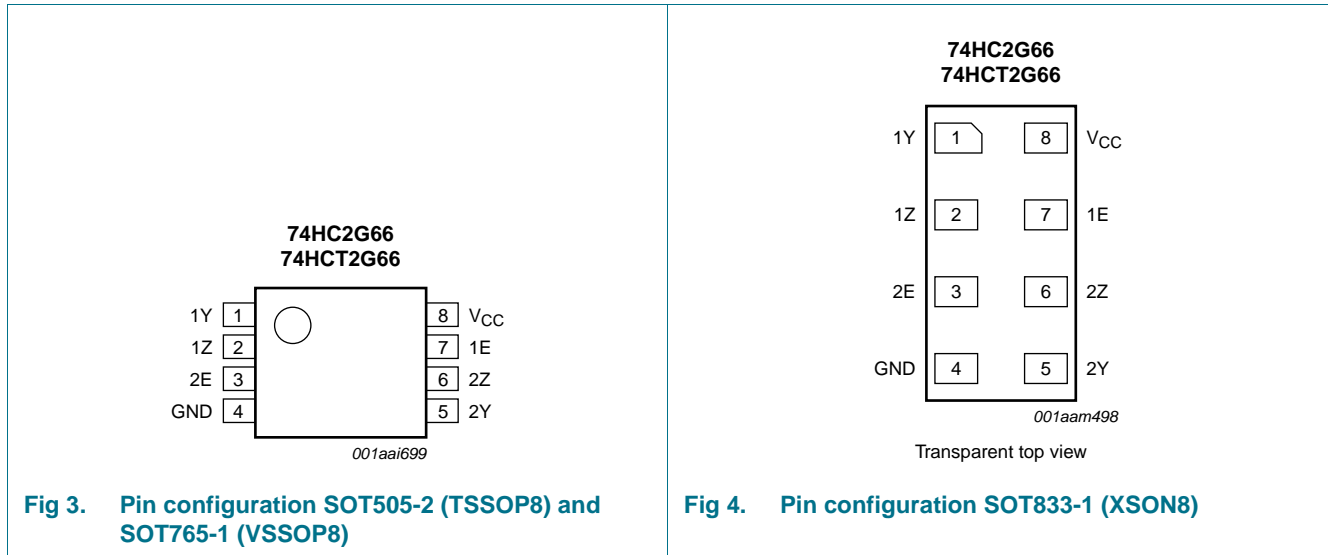


Fig 2. Logic diagram for 1 switch

6. Pinning information

6.1 Pinning



6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
1Y, 2Y	1, 5	independent input or output
1Z, 2Z	2, 6	independent input or output
GND	4	ground (0 V)
1E, 2E	7, 3	enable input (active HIGH)
V _{CC}	8	supply voltage

7. Functional description

Table 4. Function table^[1]

Input nE	Switch
L	OFF
H	ON

[1] H = HIGH voltage level; L = LOW voltage level.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+11.0	V
I_{IK}	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	[1] -	± 20	mA
I_{SK}	switch clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	[1] -	± 20	mA
I_{SW}	switch current	$V_{SW} > -0.5\text{ V}$ or $V_{SW} < V_{CC} + 0.5\text{ V}$	-	± 20	mA
I_{CC}	supply current		-	30	mA
I_{GND}	ground current		-30	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$			
		per package	[2] -	300	mW
		per switch	[2] -	100	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For TSSOP8 packages: above 55 °C the value of P_{tot} derates linearly with 2.5 mW/K.
 For VSSOP8 packages: above 110 °C the value of P_{tot} derates linearly with 8.0 mW/K.
 For XSON8 packages: above 118 °C the value of P_{tot} derates linearly with 7.8 mW/K.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).^[1]

Symbol	Parameter	Conditions	74HC2G66			74HCT2G66			Unit
			Min	Typ	Max	Min	Typ	Max	
V _{CC}	supply voltage		2.0	5.0	10.0	4.5	5.0	5.5	V
V _I	input voltage		0	-	V _{CC}	0	-	V _{CC}	V
V _O	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
V _{SW}	switch voltage		0	-	V _{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V _{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V _{CC} = 6.0 V	-	-	83	-	-	-	ns/V
		V _{CC} = 10.0 V	-	-	35	-	-	-	ns/V

[1] To avoid drawing V_{CC} current out of pin nZ, when switch current flows in pin nY, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into pin nZ, no V_{CC} current will flow out of terminal nY. In this case there is no limit for the voltage drop across the switch, but the voltage at pins nY and nZ may not exceed V_{CC} or GND.

10. Static characteristics

Table 7. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
74HC2G66								
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	V
		V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	V
		V _{CC} = 9.0 V	6.3	4.7	-	6.3	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	V
		V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	V
		V _{CC} = 9.0 V	-	4.3	2.7	-	2.7	V
I _I	input leakage current	nE; V _I = V _{CC} or GND						
		V _{CC} = 6.0 V	-	-	±0.1	-	±0.1	μA
		V _{CC} = 9.0 V	-	-	±0.2	-	±0.2	μA
I _{S(OFF)}	OFF-state leakage current	nY or nZ; V _{CC} = 9.0 V; see Figure 6	-	0.1	1.0	-	1.0	μA
I _{S(ON)}	ON-state leakage current	nY or nZ; V _{CC} = 9.0 V; see Figure 7	-	0.1	1.0	-	1.0	μA
I _{CC}	supply current	nE, nY and nZ = V _{CC} or GND						
		V _{CC} = 6.0 V	-	-	10	-	20	μA
		V _{CC} = 9.0 V	-	-	20	-	40	μA

Table 7. Static characteristics ...continued
 Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
C_I	input capacitance		-	3.5	-	-	-	pF
C_{PD}	power dissipation capacitance		-	9	-	-	-	pF
$C_{S(ON)}$	ON-state capacitance		-	8	-	-	-	pF
74HCT2G66								
V_{IH}	HIGH-level input voltage	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	2.0	1.6	-	2.0	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	1.2	0.8	-	0.8	V
I_I	input leakage current	nE; $V_I = V_{CC}$ or GND; $V_{CC} = 5.5\text{ V}$	-	-	± 1.0	-	± 1.0	μA
$I_{S(OFF)}$	OFF-state leakage current	nY or nZ; $V_{CC} = 5.5\text{ V}$; see Figure 6	-	0.1	1.0	-	1.0	μA
$I_{S(ON)}$	ON-state leakage current	nY or nZ; $V_{CC} = 5.5\text{ V}$; see Figure 7	-	0.1	1.0	-	1.0	μA
I_{CC}	supply current	nE, nY and nZ = V_{CC} or GND; $V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	-	10	-	20	μA
ΔI_{CC}	additional supply current	nE = $V_{CC} - 2.1\text{ V}$; $I_O = 0\text{ A}$; $V_{CC} = 4.5\text{ V to }5.5\text{ V}$;	-	-	375	-	410	μA
C_I	input capacitance		-	3.5	-	-	-	pF
C_{PD}	power dissipation capacitance		-	9	-	-	-	pF
$C_{S(ON)}$	ON-state capacitance		-	8	-	-	-	pF

[1] Typical values are measured at $T_{amb} = 25\text{ °C}$.

10.1 Test circuits

$V_I = V_{CC}$ or GND and $V_O = \text{GND}$ or V_{CC} .

Fig 6. Test circuit for measuring OFF-state leakage current

$V_I = V_{CC}$ or GND and $V_O = \text{open circuit}$.

Fig 7. Test circuit for measuring ON-state leakage current

10.2 ON resistance

Table 8. ON resistance for 74HC2G66 and 74HCT2G66

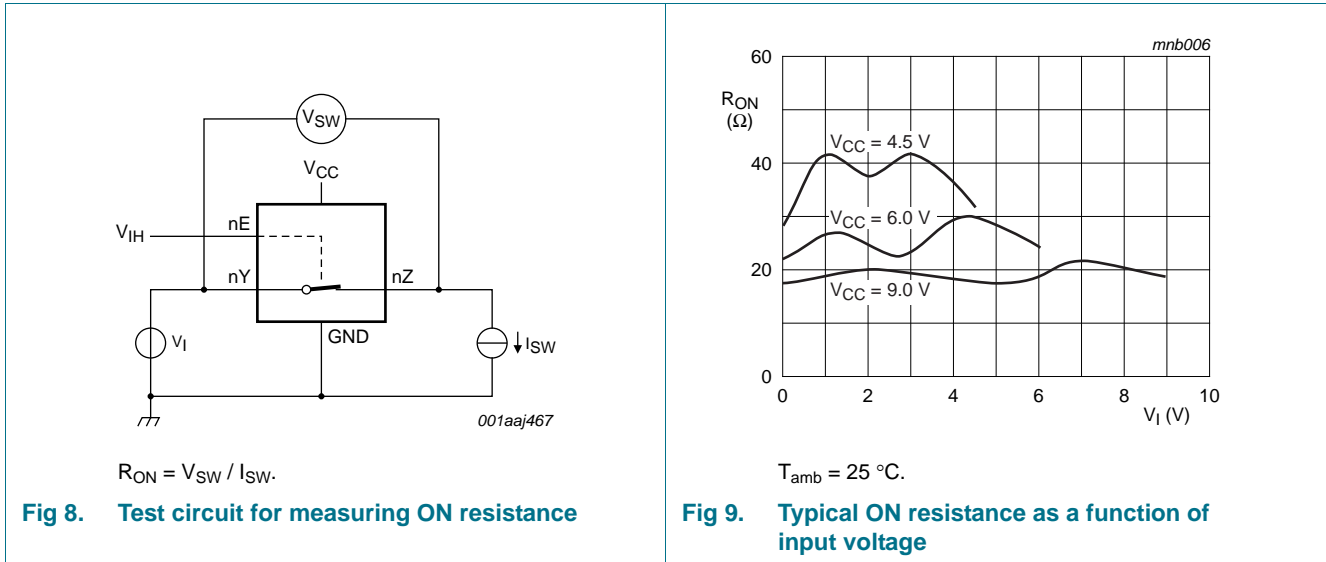
At recommended operating conditions; voltages are referenced to GND (ground 0 V); for graph see [Figure 9](#).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit	
			Min	Typ ^[2]	Max	Min	Max		
74HC2G66^[1]									
R _{ON(peak)}	ON resistance (peak)	V _I = GND to V _{CC} ; see Figure 8 and 9							
		I _{SW} = 0.1 mA; V _{CC} = 2.0 V	-	250	-	-	-	Ω	
		I _{SW} = 1.0 mA; V _{CC} = 4.5 V	-	41	118	-	142	Ω	
		I _{SW} = 1.0 mA; V _{CC} = 6.0 V	-	30	105	-	126	Ω	
		I _{SW} = 1.0 mA; V _{CC} = 9.0 V	-	21	88	-	105	Ω	
R _{ON(rail)}	ON resistance (rail)	V _I = GND; see Figure 8 and 9							
		I _{SW} = 0.1 mA; V _{CC} = 2.0 V	-	65	-	-	-	Ω	
		I _{SW} = 1.0 mA; V _{CC} = 4.5 V	-	28	95	-	115	Ω	
		I _{SW} = 1.0 mA; V _{CC} = 6.0 V	-	22	82	-	100	Ω	
		I _{SW} = 1.0 mA; V _{CC} = 9.0 V	-	18	70	-	80	Ω	
		V _I = V _{CC} ; see Figure 8 and 9							
		I _{SW} = 0.1 mA; V _{CC} = 2.0 V	-	65	-	-	-	Ω	
		I _{SW} = 1.0 mA; V _{CC} = 4.5 V	-	31	106	-	128	Ω	
		I _{SW} = 1.0 mA; V _{CC} = 6.0 V	-	23	94	-	113	Ω	
		I _{SW} = 1.0 mA; V _{CC} = 9.0 V	-	19	78	-	95	Ω	
ΔR _{ON}	ON resistance mismatch between channels	V _I = V _{CC} to GND; see Figure 8 and 9							
		V _{CC} = 4.5 V	-	5	-	-	-	Ω	
		V _{CC} = 6.0 V	-	4	-	-	-	Ω	
		V _{CC} = 9.0 V	-	3	-	-	-	Ω	
74HCT2G66									
R _{ON(peak)}	ON resistance (peak)	V _I = GND to V _{CC} ; see Figure 8 and 9							
		I _{SW} = 1.0 mA; V _{CC} = 4.5 V	-	41	118	-	142	Ω	
R _{ON(rail)}	ON resistance (rail)	V _I = GND; see Figure 8 and 9							
		I _{SW} = 1.0 mA; V _{CC} = 4.5 V	-	28	95	-	115	Ω	
		V _I = V _{CC} ; see Figure 8 and 9							
		I _{SW} = 1.0 mA; V _{CC} = 4.5 V	-	31	106	-	128	Ω	
ΔR _{ON}	ON resistance mismatch between channels	V _I = V _{CC} to GND; see Figure 8 and 9							
		V _{CC} = 4.5 V	-	5	-	-	-	Ω	

[1] At supply voltages approaching 2 V, the ON resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital signals only, when using this supply voltage.

[2] Typical values are measured at T_{amb} = 25 °C.

10.3 ON resistance test circuit and graphs



11. Dynamic characteristics

Table 9. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); For test circuit see Figure 12.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit	
			Min	Typ ^[1]	Max	Min	Max		
74HC2G66									
t_{pd}	propagation delay	nY to nZ or nZ to nY; $R_L = \infty\ \Omega$; see Figure 10		[2]					
		$V_{CC} = 2.0\text{ V}$	-	6.5	65	-	80	ns	
		$V_{CC} = 4.5\text{ V}$	-	2	13	-	15	ns	
		$V_{CC} = 6.0\text{ V}$	-	1.5	11	-	14	ns	
		$V_{CC} = 9.0\text{ V}$	-	1.2	10	-	12	ns	
t_{en}	enable time	nE to nY or nZ; see Figure 11		[2]					
		$V_{CC} = 2.0\text{ V}$	-	40	125	-	150	ns	
		$V_{CC} = 4.5\text{ V}$	-	12	29	-	30	ns	
		$V_{CC} = 6.0\text{ V}$	-	10	21	-	26	ns	
		$V_{CC} = 9.0\text{ V}$	-	7	16	-	20	ns	
t_{dis}	disable time	nE to nY or nZ; see Figure 11		[2]					
		$V_{CC} = 2.0\text{ V}$	-	21	145	-	175	ns	
		$V_{CC} = 4.5\text{ V}$	-	12	29	-	35	ns	
		$V_{CC} = 6.0\text{ V}$	-	11	28	-	33	ns	
		$V_{CC} = 9.0\text{ V}$	-	10	23	-	27	ns	
C_{PD}	power dissipation capacitance	$V_I = \text{GND to } V_{CC}$		[3]					
			-	9	-	-	-	pF	

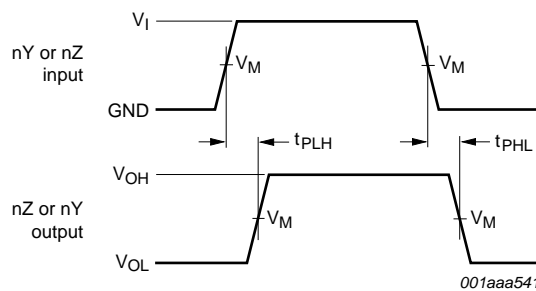
Table 9. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); For test circuit see [Figure 12](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
74HCT2G66								
t_{pd}	propagation delay	nY to nZ or nZ to nY; $R_L = \infty \Omega$; see Figure 10						
		$V_{CC} = 4.5 V$	-	2	15	-	18	ns
t_{en}	enable time	nE to nY or nZ; see Figure 11						
		$V_{CC} = 4.5 V$	-	13	30	-	36	ns
t_{dis}	disable time	nE to nY or nZ; see Figure 11						
		$V_{CC} = 4.5 V$	-	13	44	-	53	ns
C_{PD}	power dissipation capacitance	$V_I = GND$ to $V_{CC} - 1.5 V$		9	-	-	-	pF

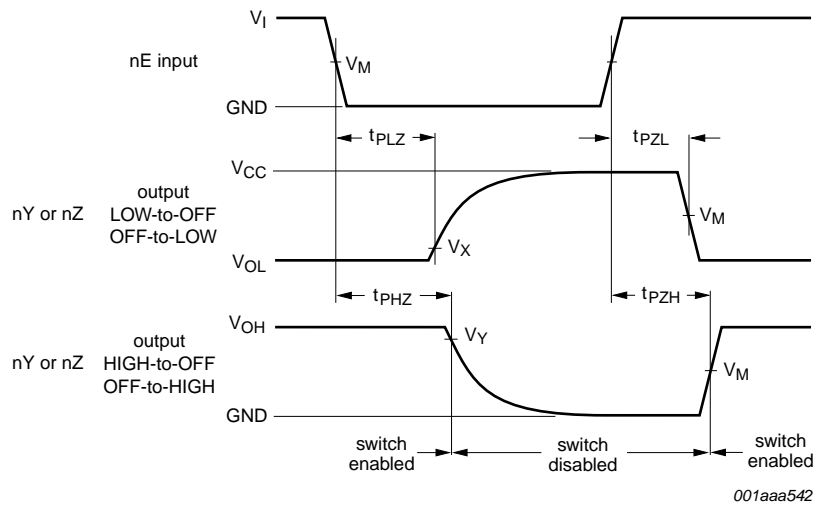
- [1] All typical values are measured at $T_{amb} = 25 \text{ °C}$.
- [2] t_{pd} is the same as t_{PLH} and t_{PHL} .
 t_{en} is the same as t_{PZL} and t_{PZH} .
 t_{dis} is the same as t_{PLZ} and t_{PHZ} .
- [3] C_{PD} is used to determine the dynamic power dissipation P_D (μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma((C_L \times C_{SW}) \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 C_L = output load capacitance in pF;
 C_{SW} = maximum switch capacitance in pF (see [Table 7](#));
 V_{CC} = supply voltage in volts;
 $\Sigma((C_L \times C_{SW}) \times V_{CC}^2 \times f_o)$ = sum of outputs.

11.1 Waveforms and test circuit



Measurement points are given in [Table 10](#).
 Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 10. Input (nY or nZ) to output (nZ or nY) propagation delays



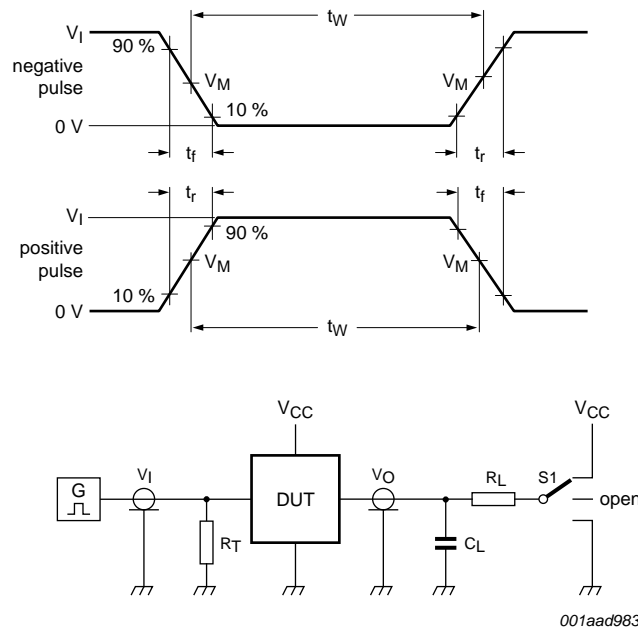
Measurement points are given in [Table 10](#).

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 11. Enable and disable times

Table 10. Measurement points

Type	Input	Output		
	V_M	V_M	V_X	V_Y
74HC2G66	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 10\%$	$V_{OH} - 10\%$
74HCT2G66	1.3 V	1.3 V	$V_{OL} + 10\%$	$V_{OH} - 10\%$



Test data is given in [Table 11](#).

Definitions for test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

S1 = Test selection switch.

Fig 12. Test circuit for measuring switching times

Table 11. Test data

Type	Input		Load		S1 position		
	V_I	t_r, t_f [1]	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74HC2G66	GND to V_{CC}	6 ns	50 pF	1 k Ω	open	GND	V_{CC}
74HCT2G66	GND to 3 V	6 ns	50 pF	1 k Ω	open	GND	V_{CC}

[1] There is no constraint on t_r, t_f with a 50 % duty factor when measuring f_{max} .

11.2 Additional dynamic characteristics

Table 12. Additional dynamic characteristics for 74HC2G66 and 74HCT2G66

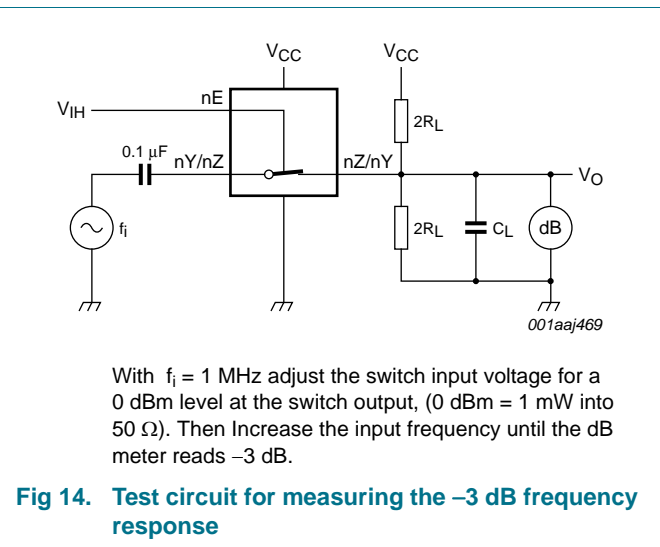
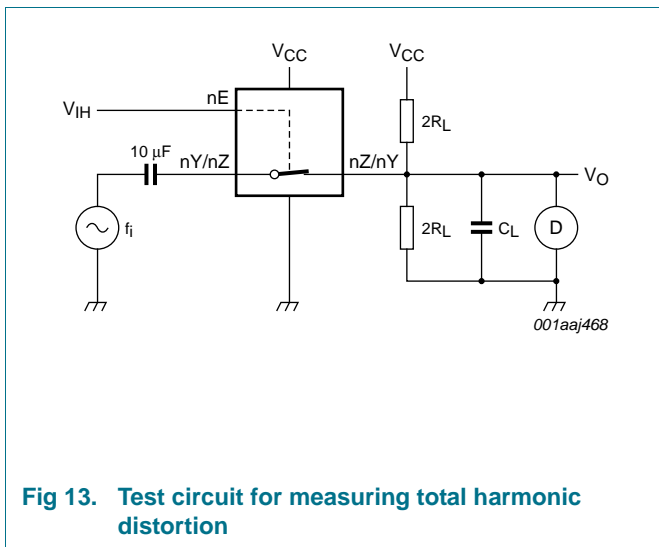
$GND = 0 V$; $t_r = t_f = 6.0 ns$; $C_L = 50 pF$; unless otherwise specified. All typical values are measured at $T_{amb} = 25 ^\circ C$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
THD	total harmonic distortion	$f_i = 1 kHz$; $R_L = 10 k\Omega$; see Figure 13				%	
		$V_{CC} = 4.5 V$; $V_I = 4.0 V$ (p-p)	-	0.04	-	%	
		$V_{CC} = 9.0 V$; $V_I = 8.0 V$ (p-p)	-	0.02	-	%	
		$f_i = 10 kHz$; $R_L = 10 k\Omega$; see Figure 13					%
		$V_{CC} = 4.5 V$; $V_I = 4.0 V$ (p-p)	-	0.12	-	%	
		$V_{CC} = 9.0 V$; $V_I = 8.0 V$ (p-p)	-	0.06	-	%	

Table 12. Additional dynamic characteristics for 74HC2G66 and 74HCT2G66 ...continued
GND = 0 V; $t_r = t_f = 6.0$ ns; $C_L = 50$ pF; unless otherwise specified. All typical values are measured at $T_{amb} = 25$ °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{(-3dB)}$	-3 dB frequency response	$R_L = 50 \Omega$; $C_L = 10$ pF; see Figure 14 and 15				
		$V_{CC} = 4.5$ V	-	180	-	MHz
		$V_{CC} = 9.0$ V	-	200	-	MHz
α_{iso}	isolation (OFF-state)	$R_L = 600 \Omega$; $f_i = 1$ MHz; see Figure 16 and 17				
		$V_{CC} = 4.5$ V	-	-50	-	dB
		$V_{CC} = 9.0$ V	-	-50	-	dB
V_{ct}	crosstalk voltage	between digital input and switch (peak to peak value); $R_L = 600 \Omega$; $f_i = 1$ MHz; see Figure 18				
		$V_{CC} = 4.5$ V	-	110	-	mV
		$V_{CC} = 9.0$ V	-	220	-	mV
Xtalk	crosstalk	between switches; $R_L = 600 \Omega$; $f_i = 1$ MHz; see Figure 19				
		$V_{CC} = 4.5$ V	-	-60	-	dB
		$V_{CC} = 9.0$ V	-	-60	-	dB

11.3 Test circuits and graphs



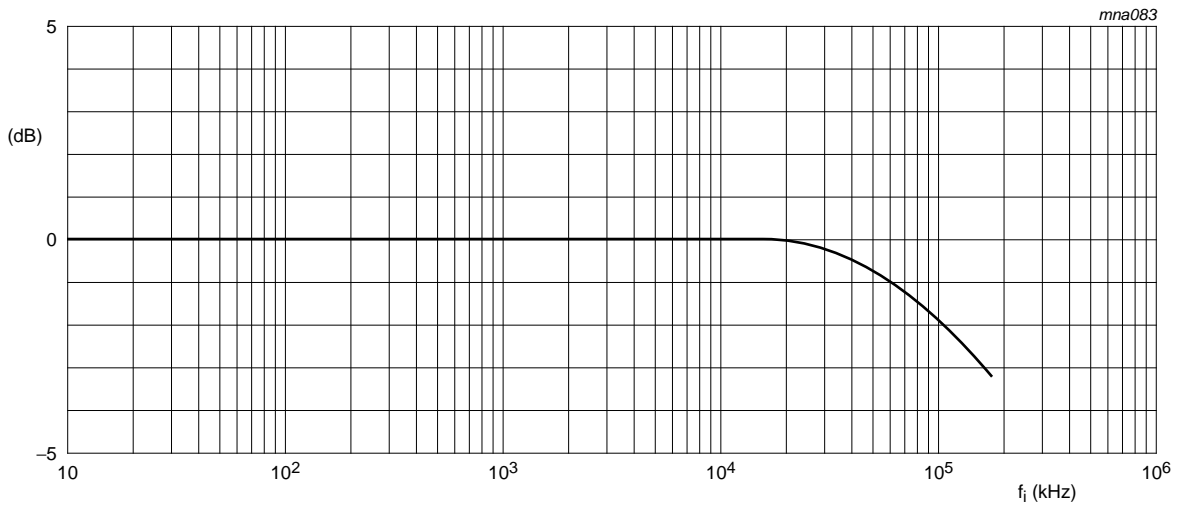
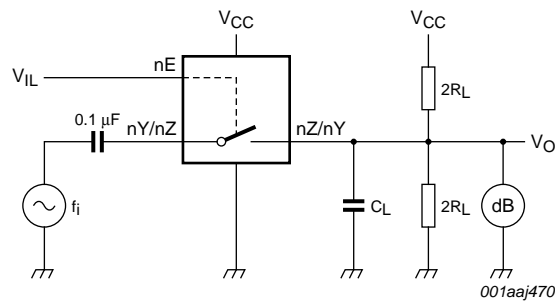
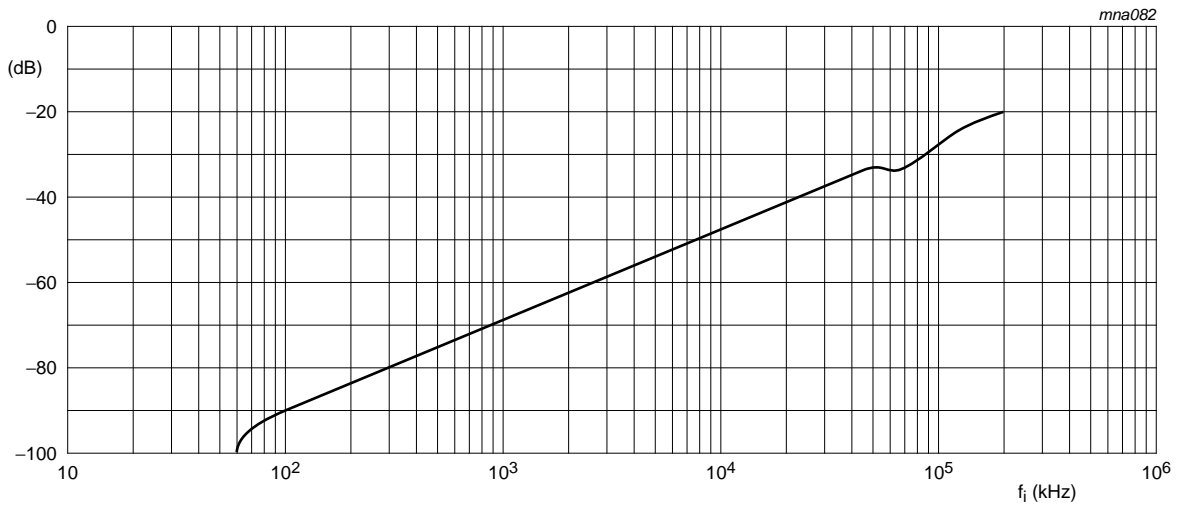


Fig 15. Typical -3 dB frequency response



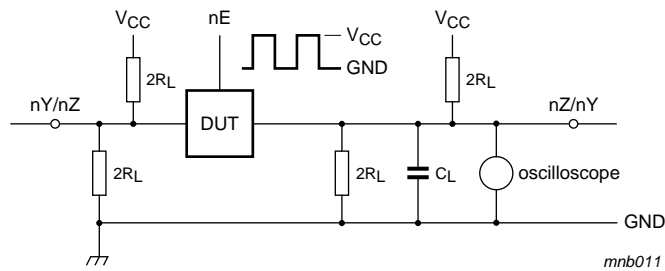
Adjust the switch input voltage for a 0 dBm level (0 dBm = 1 mW into 600 Ω)

Fig 16. Test circuit for measuring isolation (OFF-state)

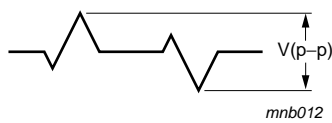


Test conditions: $V_{CC} = 4.5\text{ V}$; $GND = 0\text{ V}$; $R_L = 50\ \Omega$; $R_{SOURCE} = 1\text{ k}\Omega$.

Fig 17. Typical isolation (OFF-state) as a function of frequency



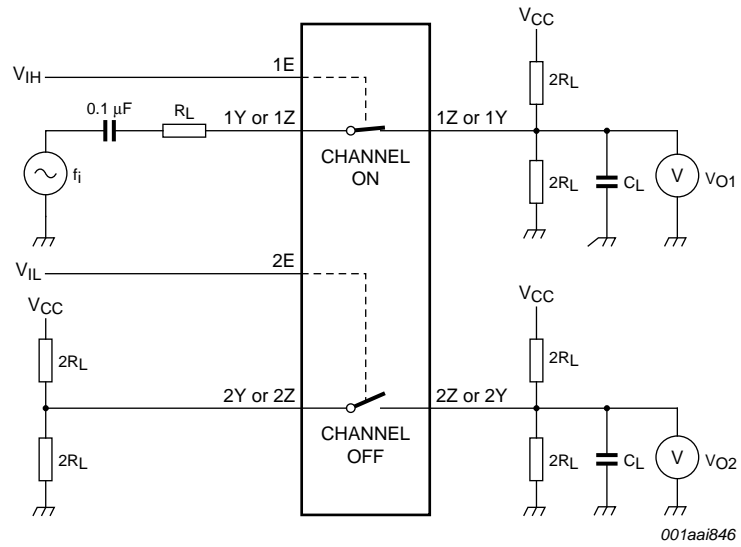
a. Circuit



b. Crosstalk voltage

Adjust the switch input voltage for a 0 dBm level (0 dBm = 1 mW into 600 Ω)

Fig 18. Test circuit for measuring crosstalk voltage (between the digital input and the switch)



Adjust the switch input voltage for a 0 dBm level (0 dBm = 1 mW into 600 Ω)

Fig 19. Test circuit for measuring crosstalk (between the switches)

12. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2

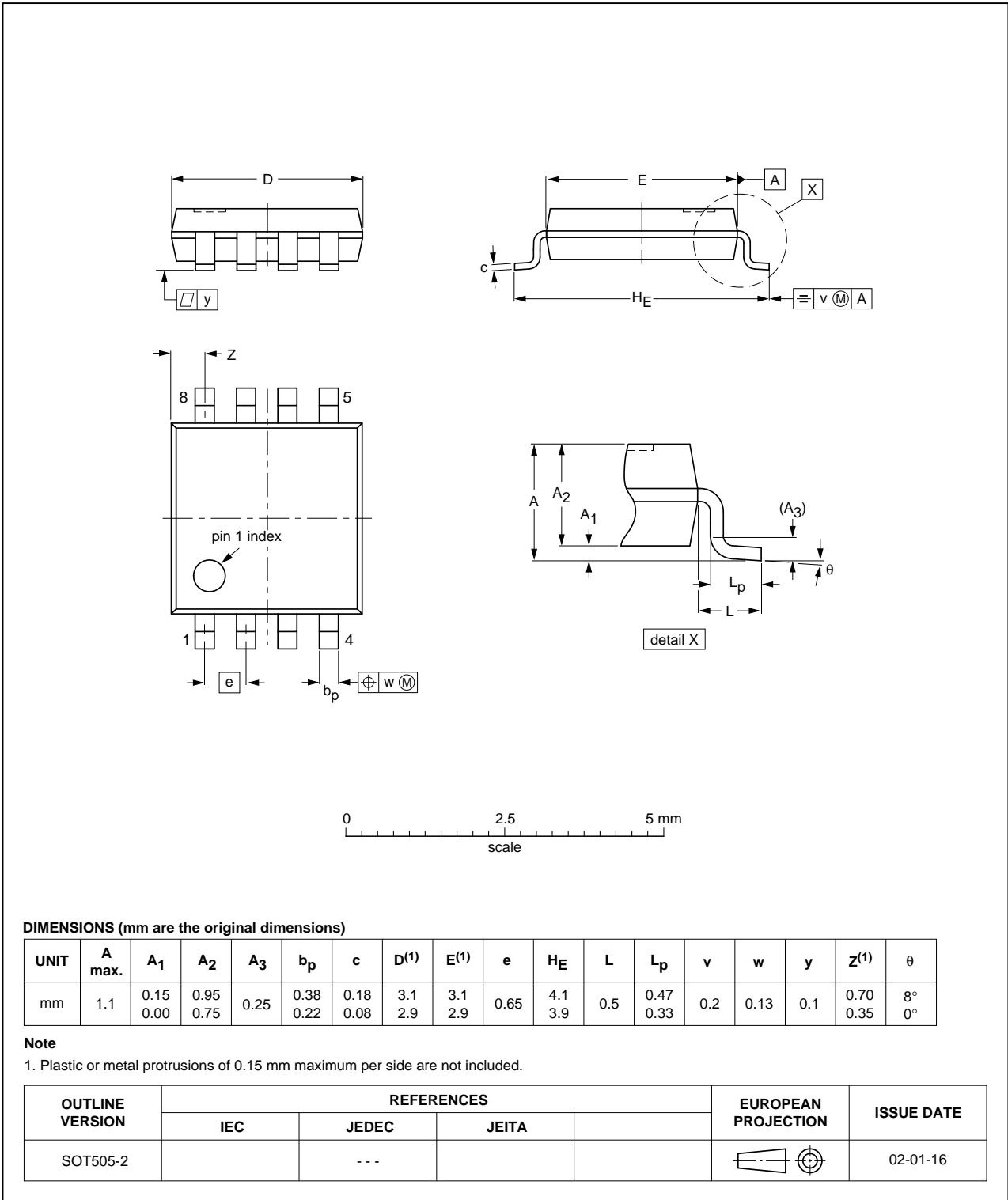


Fig 20. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1

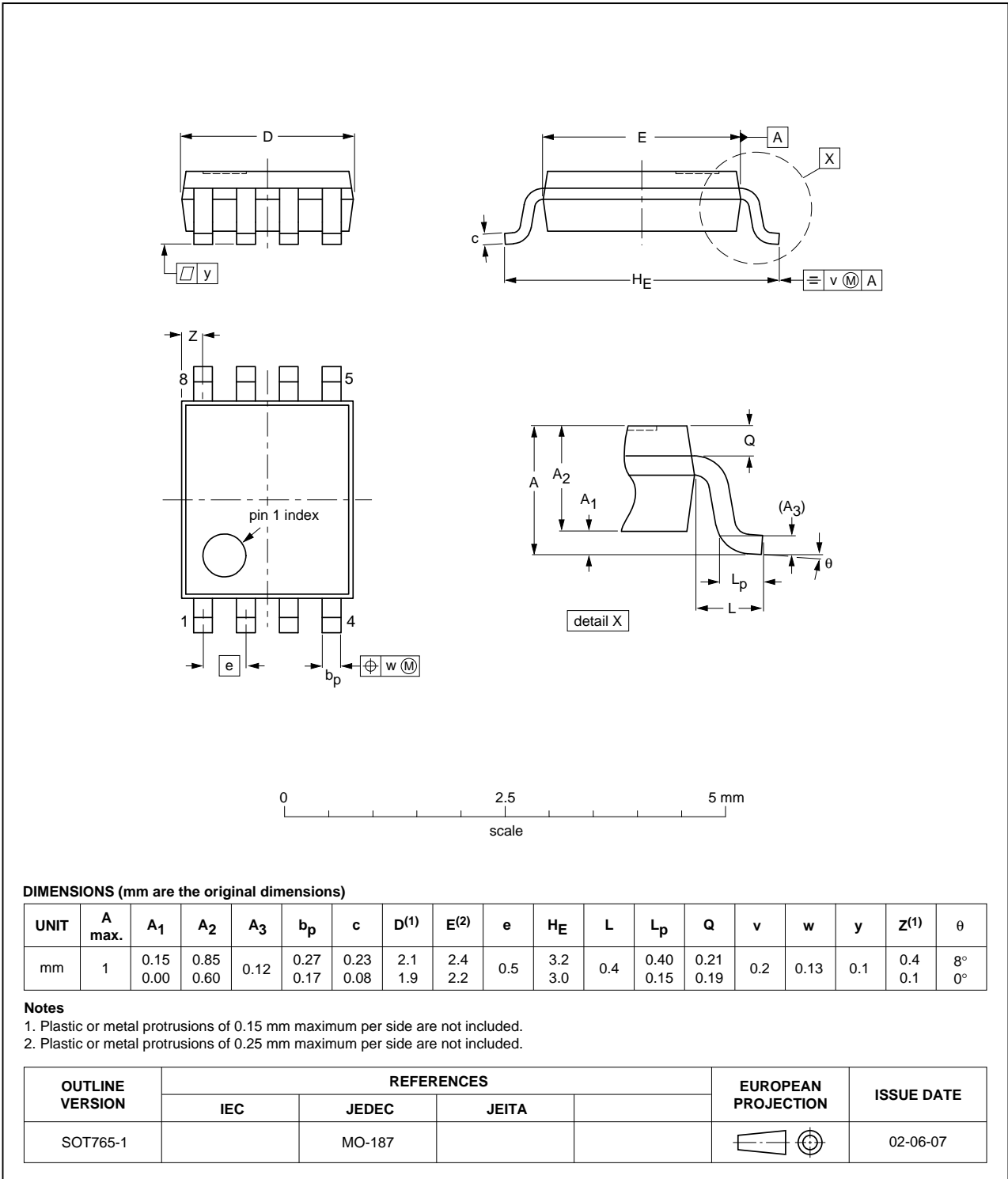


Fig 21. Package outline SOT765-1 (VSSOP8)

XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm

SOT833-1

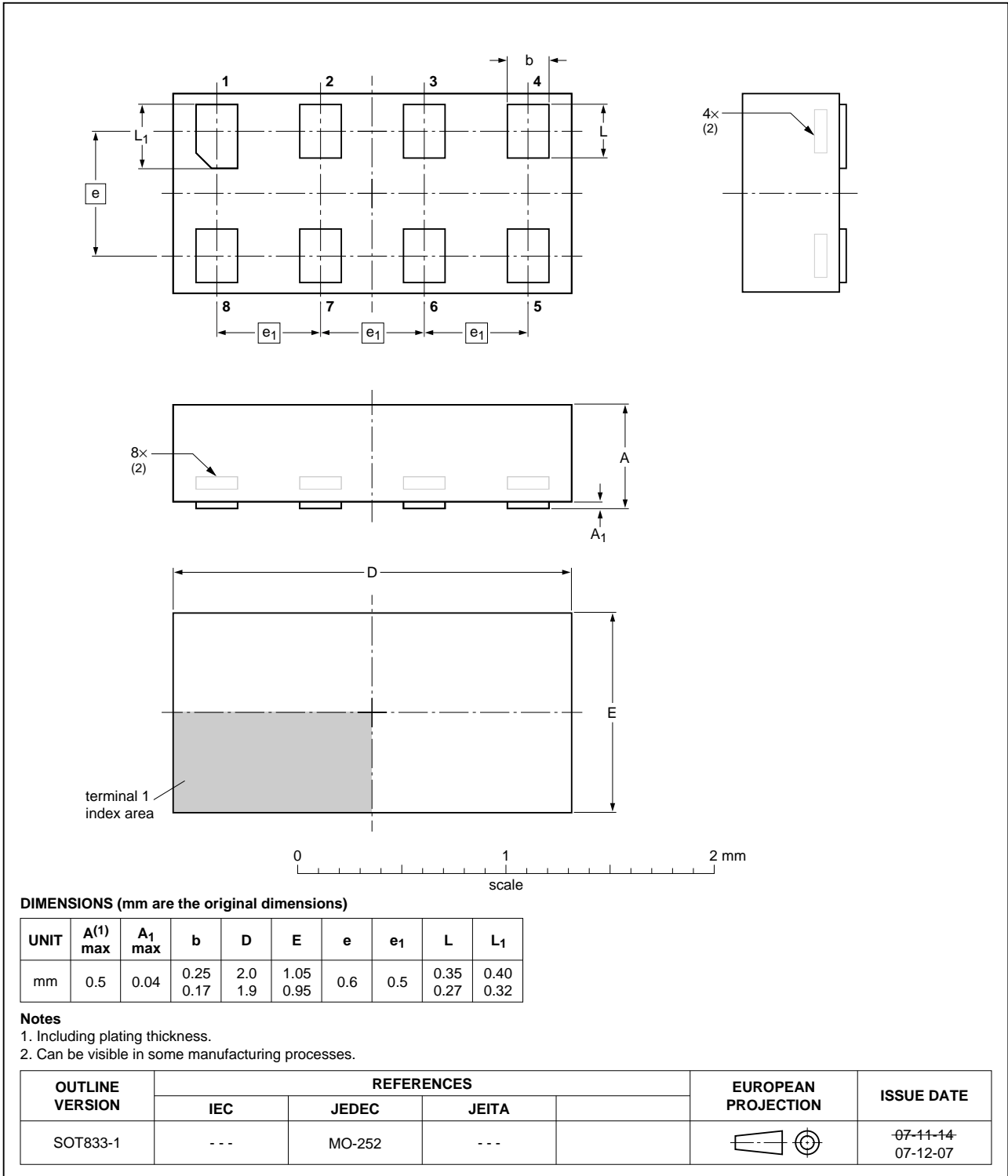


Fig 22. Package outline SOT833-1 (XSON8)

XSON8: plastic extremely thin small outline package; no leads;
8 terminals; body 3 x 2 x 0.5 mm

SOT996-2



Fig 23. Package outline SOT996-2 (XSON8)

13. Abbreviations

Table 13. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
DUT	Device Under Test

14. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT2G66 v.10	20131003	Product data sheet	-	74HC_HCT2G66 v.9
Modifications:	<ul style="list-style-type: none"> For type numbers 74HC2G66GD and 74HCT2G66GD XSON8U has changed to XSON8. 			
74HC_HCT2G66 v.9	20111213	Product data sheet	-	74HC_HCT2G66 v.8
74HC_HCT2G66 v.8	20100923	Product data sheet	-	74HC_HCT2G66 v.7
74HC_HCT2G66 v.7	20100914	Product data sheet	-	74HC_HCT2G66 v.6
74HC_HCT2G66 v.6	20100402	Product data sheet	-	74HC_HCT2G66 v.5
74HC_HCT2G66 v.5	20090126	Product data sheet	-	74HC_HCT2G66 v.4
74HC_HCT2G66 v.4	20040519	Product specification	-	74HC_HCT2G66 v.3
74HC_HCT2G66 v.3	20031126	Product specification	-	74HC_HCT2G66 v.2
74HC_HCT2G66 v.2	20030808	Product specification	-	74HC_HCT2G66 v.1
74HC_HCT2G66 v.1	20030625	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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