# HEF4517B

## Dual 64-bit static shift register

**Rev. 7 — 11 November 2011**     **Product data sheet**

## 1. General description

The HEF4517B consists of two identical, independent 64-bit static shift registers. Each register has separate clock (nCP), data input (nD), parallel input-enable/output-enable (nPE/$\overline{\text{OE}}$) and four 3-state outputs of the 16th, 32nd, 48th, and 64th bit positions (nQ16 to nQ64). Data at the nD input is entered into the first bit on the LOW-to-HIGH transition of the clock, regardless of the state of nPE/$\overline{\text{OE}}$.

When nPE/$\overline{\text{OE}}$ is LOW, the outputs are enabled and it is in the 64-bit serial mode.

When nPE/$\overline{\text{OE}}$ is HIGH, the outputs are disabled (high-impedance OFF-state), the 64-bit shift register is divided into four 16-bit shift registers with nD, nQ16, nQ32 and nQ48 as data inputs of the 1st, 17th, 33rd, and 49th bit respectively. Schmitt-trigger action in the clock input makes the circuit highly tolerant of slower clock rise and fall times.

It operates over a recommended $V_{DD}$ power supply range of 3 V to 15 V referenced to $V_{SS}$ (usually ground). Unused inputs must be connected to $V_{DD}$, $V_{SS}$, or another input.

## 2. Features and benefits

- Tolerant of slow clock rise and fall times
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Specified from −40 °C to +85 °C
- Complies with JEDEC standard JESD 13-B

## 3. Ordering information

**Table 1.  Ordering information**
*All types operate from −40 °C to +85 °C*

| Type number | Package | | | |
|---|---|---|---|---|
| | **Name** | **Description** | | **Version** |
| HEF4517BP | DIP16 | plastic dual in-line package; 16 leads (300 mil) | | SOT38-4 |
| HEF4517BT | SO16 | plastic small outline package; 16 leads; body width 7.5 mm | | SOT162-1 |

## 4. Functional diagram



Fig 1.    Functional diagram
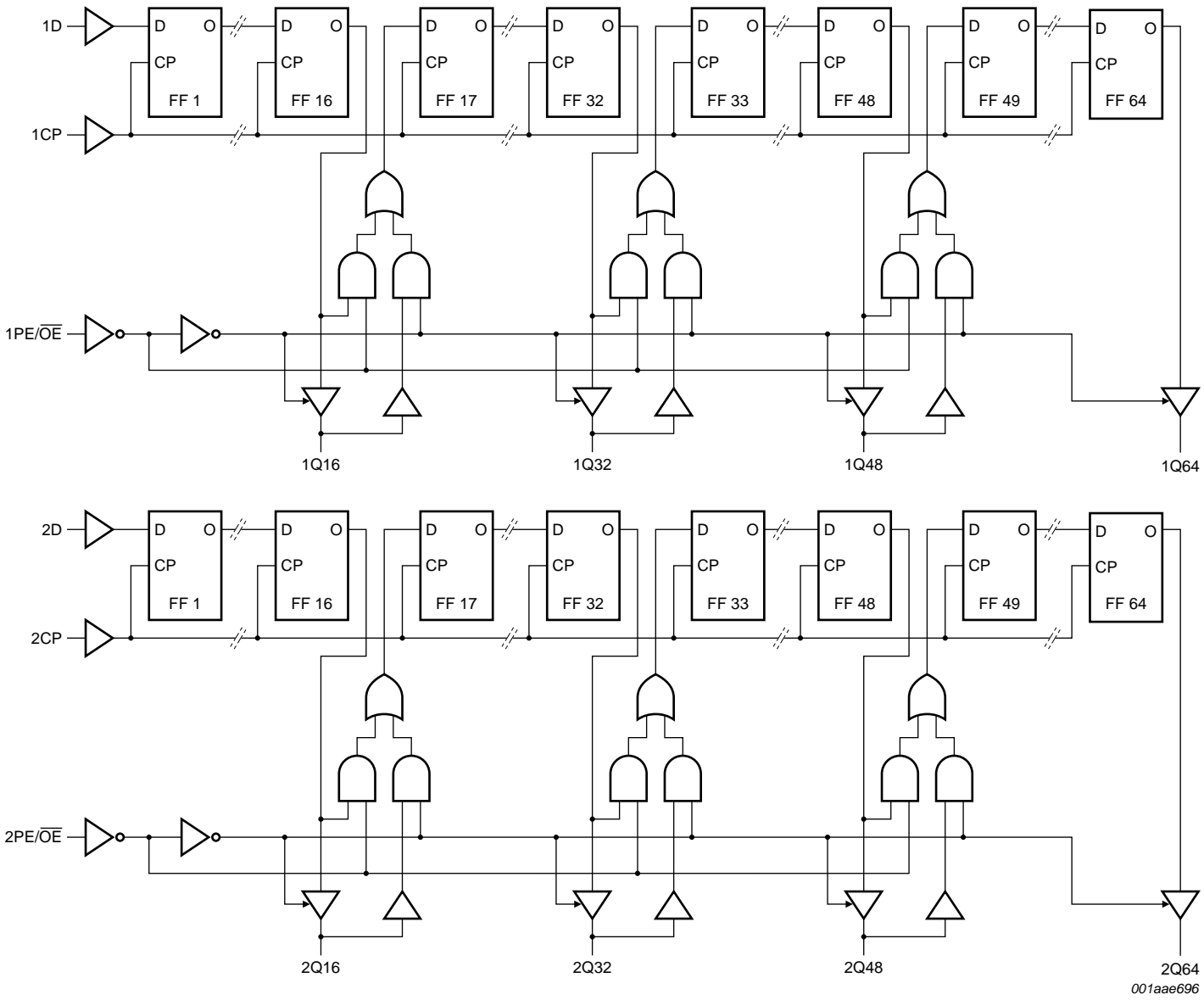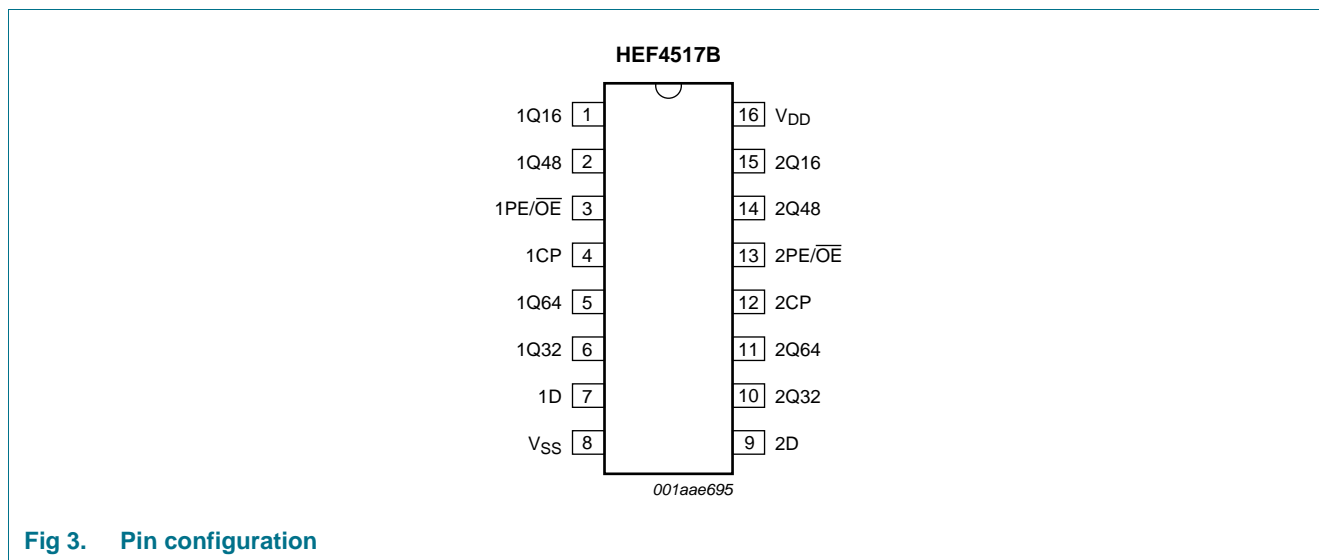
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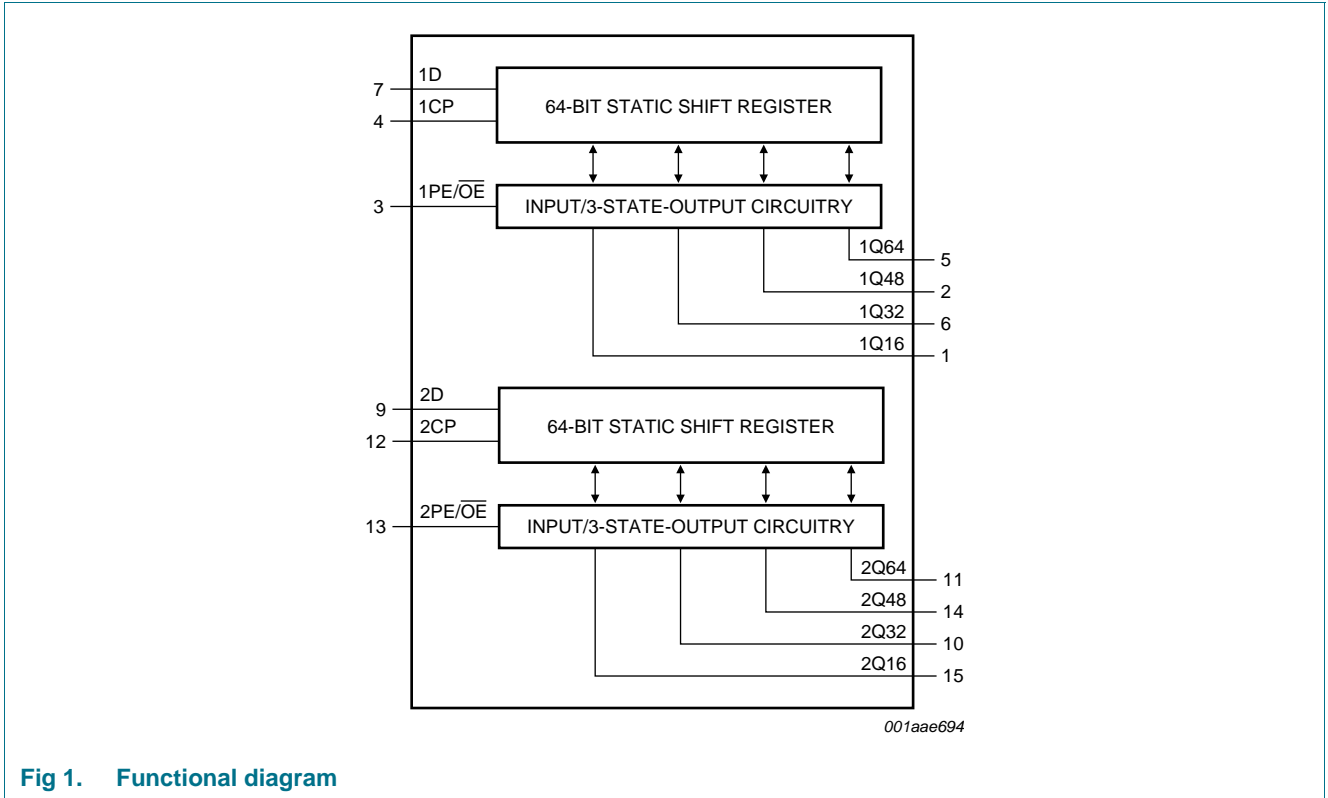
**Fig 2.** Logic diagram

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## 5. Pinning information

### 5.1 Pinning

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| | | | |
|---|---|---|---|
| 1Q16 | 1 | 16 | V_DD |
| 1Q48 | 2 | 15 | 2Q16 |
| 1PE/OE | 3 | 14 | 2Q48 |
| 1CP | 4 | 13 | 2PE/OE |
| 1Q64 | 5 | 12 | 2CP |
| 1Q32 | 6 | 11 | 2Q64 |
| 1D | 7 | 10 | 2Q32 |
| V_SS | 8 | 9 | 2D |

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**Fig 3.    Pin configuration**

### 5.2 Pin description

**Table 2.    Pin description**

| Symbol | Pin | Description |
|---|---|---|
| 1Q16, 2Q16 | 1, 15 | 3-state input/output |
| 1Q48, 2Q48 | 2, 14 | 3-state input/output |
| 1PE/$\overline{OE}$, 2PE/$\overline{OE}$ | 3, 13 | parallel input-enable/output-enable input |
| 1CP, 2CP | 4, 12 | clock input |
| 1Q64, 2Q64 | 5, 11 | 3-state input/output |
| 1Q32, 2Q32 | 6, 10 | 3-state input/output |
| 1D, 2D | 7, 9 | data input |
| V$_{SS}$ | 8 | ground supply voltage |
| V$_{DD}$ | 16 | supply voltage |

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## 6. Functional description

**Table 3.    Function table[1]**

| Inputs | | | Inputs/outputs | | | | Mode |
|---|---|---|---|---|---|---|---|
| nCP | nD | nPE/$\overline{OE}$ | nQ16 | nQ32 | nQ48 | nQ64 | |
| ↑ | data entered into 1st bit | L | content of 16th bit displayed | content of 32nd bit displayed | content of 48th bit displayed | content of 64th bit displayed | One 64-bit shift register. The content of the shift register is shifted over one stage |
| ↑ | data entered into 1st bit | H | data at nQ16 entered into 17th bit | data at nQ32 entered into 33rd bit | data at nQ48 entered into 49th bit | remains in 'Z' state | Four 16-bit shift register. The content of the shift registers is shifted over one stage |
| ↓ | X | L | no change | no change | no change | no change | no change |
| ↓ | X | H | Z | Z | Z | Z | no change |

[1]    H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance state;
      ↑ = positive-going transition; ↓ = negative-going transition.

## 7. Limiting values

**Table 4.    Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | supply voltage | | | −0.5 | +18 | V |
| $I_{IK}$ | input clamping current | $V_I < -0.5$ V or $V_I > V_{DD} + 0.5$ V | | - | ±10 | mA |
| $V_I$ | input voltage | | | −0.5 | $V_{DD} + 0.5$ | V |
| $I_{OK}$ | output clamping current | $V_O < -0.5$ V or $V_O > V_{DD} + 0.5$ V | | - | ±10 | mA |
| $I_{I/O}$ | input/output current | | | - | ±10 | mA |
| $I_{DD}$ | supply current | | | - | 50 | mA |
| $T_{stg}$ | storage temperature | | | −65 | +150 | °C |
| $T_{amb}$ | ambient temperature | | | −40 | +85 | °C |
| $P_{tot}$ | total power dissipation | DIP16 package | [1] | - | 750 | mW |
| | | SO16 package | [2] | - | 500 | mW |
| P | power dissipation | per output | | - | 100 | mW |

[1]    For DIP16 package: $P_{tot}$ derates linearly with 12 mW/K above 70 °C.

[2]    For SO16 package: $P_{tot}$ derates linearly with 8 mW/K above 70 °C.

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## 8. Recommended operating conditions

**Table 5.    Recommended operating conditions**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | supply voltage | | 3 | - | 15 | V |
| $V_I$ | input voltage | | 0 | - | $V_{DD}$ | V |
| $T_{amb}$ | ambient temperature | in free air | −40 | - | +85 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{DD}$ = 5 V | - | - | 3.75 | μs/V |
| | | $V_{DD}$ = 10 V | - | - | 0.5 | μs/V |
| | | $V_{DD}$ = 15 V | - | - | 0.08 | μs/V |

## 9. Static characteristics

**Table 6.    Static characteristics**
$V_{SS}$ = 0 V; $V_I$ = $V_{SS}$ or $V_{DD}$ unless otherwise specified.

| Symbol | Parameter | Conditions | $V_{DD}$ | $T_{amb}$ = −40 °C | | $T_{amb}$ = 25 °C | | $T_{amb}$ = 85 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | Min | Max | |
| $V_{IH}$ | HIGH-level input voltage | $\|I_O\|$ < 1 μA | 5 V | 3.5 | - | 3.5 | - | 3.5 | - | V |
| | | | 10 V | 7.0 | - | 7.0 | - | 7.0 | - | V |
| | | | 15 V | 11.0 | - | 11.0 | - | 11.0 | - | V |
| $V_{IL}$ | LOW-level input voltage | $\|I_O\|$ < 1 μA | 5 V | - | 1.5 | - | 1.5 | - | 1.5 | V |
| | | | 10 V | - | 3.0 | - | 3.0 | - | 3.0 | V |
| | | | 15 V | - | 4.0 | - | 4.0 | - | 4.0 | V |
| $V_{OH}$ | HIGH-level output voltage | $\|I_O\|$ < 1 μA | 5 V | 4.95 | - | 4.95 | - | 4.95 | - | V |
| | | | 10 V | 9.95 | - | 9.95 | - | 9.95 | - | V |
| | | | 15 V | 14.95 | - | 14.95 | - | 14.95 | - | V |
| $V_{OL}$ | LOW-level output voltage | $\|I_O\|$ < 1 μA | 5 V | - | 0.05 | - | 0.05 | - | 0.05 | V |
| | | | 10 V | - | 0.05 | - | 0.05 | - | 0.05 | V |
| | | | 15 V | - | 0.05 | - | 0.05 | - | 0.05 | V |
| $I_{OH}$ | HIGH-level output current | $V_O$ = 2.5 V | 5 V | - | −1.7 | - | −1.4 | - | −1.1 | mA |
| | | $V_O$ = 4.6 V | 5 V | - | −0.52 | - | −0.44 | - | −0.36 | mA |
| | | $V_O$ = 9.5 V | 10 V | - | −1.3 | - | −1.1 | - | −0.9 | mA |
| | | $V_O$ = 13.5 V | 15 V | - | −3.6 | - | −3.0 | - | −2.4 | mA |
| $I_{OL}$ | LOW-level output current | $V_O$ = 0.4 V | 5 V | 0.52 | - | 0.44 | - | 0.36 | - | mA |
| | | $V_O$ = 0.5 V | 10 V | 1.3 | - | 1.1 | - | 0.9 | - | mA |
| | | $V_O$ = 1.5 V | 15 V | 3.6 | - | 3.0 | - | 2.4 | - | mA |
| $I_I$ | input leakage current | | 15 V | - | ±0.3 | - | ±0.3 | - | ±1.0 | μA |
| $I_{DD}$ | supply current | $I_O$ = 0 A | 5 V | - | 50 | - | 50 | - | 375 | μA |
| | | | 10 V | - | 100 | - | 100 | - | 750 | μA |
| | | | 15 V | - | 200 | - | 200 | - | 1500 | μA |
| $C_I$ | input capacitance | | - | - | - | - | 7.5 | - | - | pF |

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## 10. Dynamic characteristics

**Table 7.    Dynamic characteristics**

$V_{SS} = 0$ V; $T_{amb} = 25$ °C; for test circuit see Figure 8; unless otherwise specified.

| Symbol | Parameter | Conditions | $V_{DD}$ | | Extrapolation formula | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| $t_{PHL}$ | HIGH to LOW propagation delay | nCP to nQn; see Figure 4 | 5 V | [1] | 193 ns + (0.55 ns/pF)$C_L$ | - | 220 | 440 | ns |
| | | | 10 V | | 74 ns + (0.23 ns/pF)$C_L$ | - | 85 | 170 | ns |
| | | | 15 V | | 52 ns + (0.16 ns/pF)$C_L$ | - | 60 | 120 | ns |
| $t_{PLH}$ | LOW to HIGH propagation delay | nCP to nQn; see Figure 4 | 5 V | [1] | 163 ns + (0.55 ns/pF)$C_L$ | - | 190 | 380 | ns |
| | | | 10 V | | 64 ns + (0.23 ns/pF)$C_L$ | - | 75 | 150 | ns |
| | | | 15 V | | 42 ns + (0.16 ns/pF)$C_L$ | - | 50 | 100 | ns |
| $t_{PHZ}$ | HIGH to OFF-state propagation delay | nPE/$\overline{OE}$ to nQn; see Figure 5 | 5 V | | | - | 40 | 80 | ns |
| | | | 10 V | | | - | 30 | 60 | ns |
| | | | 15 V | | | - | 25 | 50 | ns |
| $t_{PZH}$ | OFF-state to HIGH propagation delay | nPE/$\overline{OE}$ to nQn; see Figure 5 | 5 V | | | - | 45 | 90 | ns |
| | | | 10 V | | | - | 25 | 50 | ns |
| | | | 15 V | | | - | 20 | 40 | ns |
| $t_{PLZ}$ | LOW to OFF-state propagation delay | nPE/$\overline{OE}$ to nQn; see Figure 5 | 5 V | | | - | 50 | 100 | ns |
| | | | 10 V | | | - | 30 | 60 | ns |
| | | | 15 V | | | - | 25 | 50 | ns |
| $t_{PZL}$ | OFF-state to LOW propagation delay | nPE/$\overline{OE}$ to nQn; see Figure 5 | 5 V | | | - | 60 | 120 | ns |
| | | | 10 V | | | - | 30 | 60 | ns |
| | | | 15 V | | | - | 25 | 50 | ns |
| $t_t$ | transition time | nQn; see Figure 6 | 5 V | [1] | 10 ns + (1.00 ns/pF)$C_L$ | - | 60 | 120 | ns |
| | | | 10 V | | 9 ns + (0.42 ns/pF)$C_L$ | - | 30 | 60 | ns |
| | | | 15 V | | 6 ns + (0.28 ns/pF)$C_L$ | - | 20 | 40 | ns |
| $t_{su}$ | set-up time | nQn, nD to nCP; see Figure 7 | 5 V | | | 30 | 10 | - | ns |
| | | | 10 V | | | 25 | 5 | - | ns |
| | | | 15 V | | | 20 | 5 | - | ns |
| $t_h$ | hold time | nQn, nD to nCP; see Figure 7 | 5 V | | | 45 | 15 | - | ns |
| | | | 10 V | | | 30 | 10 | - | ns |
| | | | 15 V | | | 25 | 10 | - | ns |
| $t_W$ | pulse width | nQn, nD to nCP; see Figure 7 | 5 V | | | - | 95 | 190 | ns |
| | | | 10 V | | | - | 40 | 80 | ns |
| | | | 15 V | | | - | 30 | 60 | ns |
| $f_{max}$ | maximum frequency | see Figure 7 | 5 V | | | 2 | 5 | - | MHz |
| | | | 10 V | | | 6 | 12 | - | MHz |
| | | | 15 V | | | 8 | 16 | - | MHz |

[1]  The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown ($C_L$ in pF).

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**Table 8.** **Dynamic power dissipation $P_D$**

*$P_D$ can be calculated from the formulas shown. $V_{SS}$ = 0 V; $t_r$ = $t_f$ ≤ 20 ns; $T_{amb}$ = 25 ℃.*

| Symbol | Parameter | $V_{DD}$ | Typical formula for $P_D$ ($\mu$W) | where: |
|--------|-----------|----------|-----------------------------------|--------|
| $P_D$ | dynamic power dissipation | 5 V | $P_D = 7000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ | $f_i$ = input frequency in MHz, |
| | | 10 V | $P_D = 28000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ | $f_o$ = output frequency in MHz, |
| | | 15 V | $P_D = 70000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ | $C_L$ = output load capacitance in pF, |
| | | | | $V_{DD}$ = supply voltage in V, |
| | | | | $\Sigma(f_o \times C_L)$ = sum of the outputs. |

## 11. Waveforms



Measurement points are given in Table 9

The logic levels $V_{OH}$ and $V_{OL}$ are typical voltage output levels that occur with the output load.

**Fig 4.** **Propagation delays for nCP to nQn**
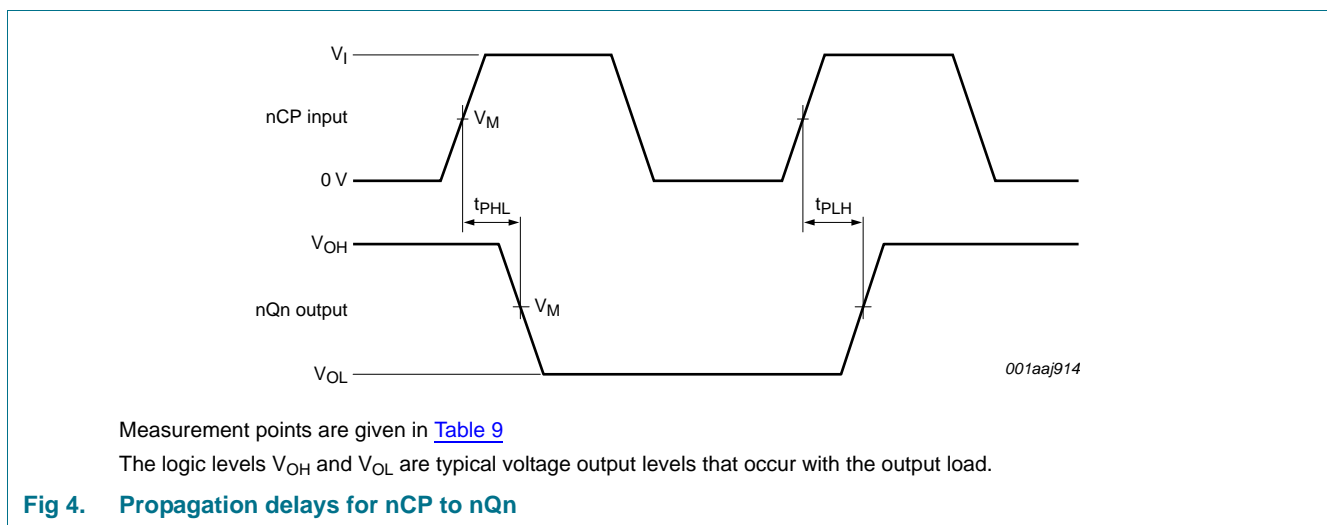
**Table 9.** **Measurement points**

| Input | Output | | |
|-------|--------|---|---|
| $V_M$ | $V_M$ | $V_X$ | $V_Y$ |
| 0.5$V_I$ | 0.5$V_{DD}$ | 0.1$V_{DD}$ | 0.9$V_{DD}$ |
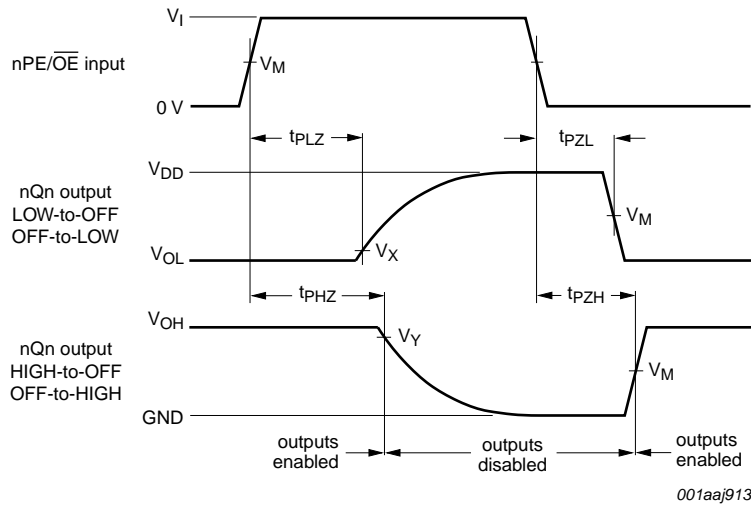
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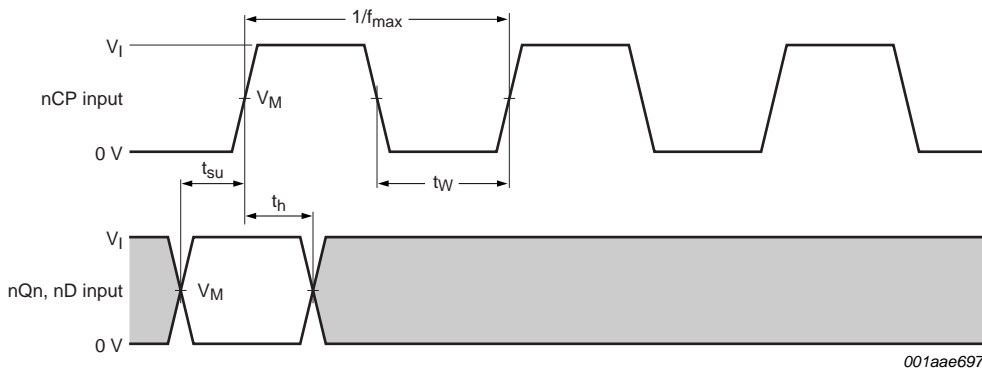Measurement points are given in Table 9

The logic levels $V_{OH}$ and $V_{OL}$ are typical voltage output levels that occur with the output load.

**Fig 5.** **Enable and disable times and 3-state propagation delays**
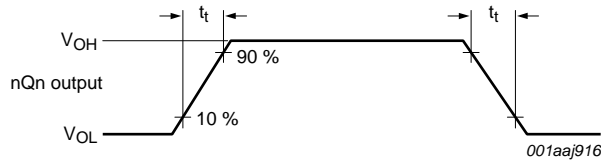


The logic levels $V_{OH}$ and $V_{OL}$ are typical voltage output levels that occur with the output load.

**Fig 6.** **Transition times for nQn**



The shading indicates where the data (nQn and nD) is permitted to change for predictable output changes.

Measurement points are given in Table 9

The logic levels $V_{OH}$ and $V_{OL}$ are typical voltage output levels that occur with the output load.

**Fig 7.** **Waveforms showing minimum clock pulse width and maximum frequency and set-up and hold times for nQn (as data input) or nD to nCP**

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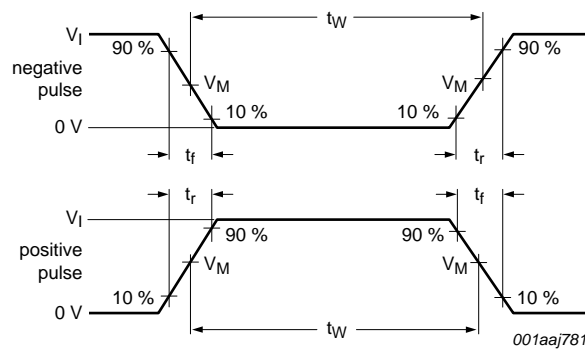
a. Input waveforms
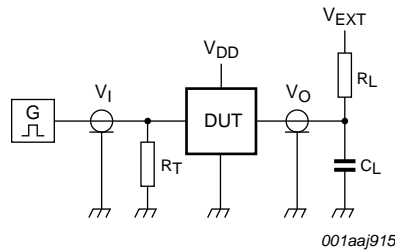


b. Test circuit

Test data is given in Table 10.

Definitions for test circuit:

DUT = Device Under Test;

$R_L$ = Load resistance;

$C_L$ = Load capacitance including jig and probe capacitance;

$R_T$ = Termination resistance should be equal to output impedance $Z_o$ of the pulse generator.

**Fig 8.   Test circuit for switching times**

**Table 10.   Test data**

| Supply voltage | Input | | Load | | $V_{EXT}$ | | |
|---|---|---|---|---|---|---|---|
| | $V_I$ | $t_r$, $t_f$ | $C_L$ | $R_L$ | $t_{PLH}$, $t_{PHL}$ | $t_{PLZ}$, $t_{PZL}$ | $t_{PHZ}$, $t_{PZH}$ |
| 5 V to 15 V | $V_{DD}$ | $\leq 20$ ns | 50 pF | 1 kΩ | open | $2V_{DD}$ | GND |

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## 12. Package outline

**DIP16: plastic dual in-line package; 16 leads (300 mil)**                                    **SOT38-4**



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | A₁ min. | A₂ max. | b | b₁ | b₂ | c | D (1) | E (1) | e | e₁ | L | M_E | M_H | w | Z (1) max. |
|------|--------|---------|---------|---|----|----|---|-------|-------|---|----|---|-----|-----|---|------------|
| mm | 4.2 | 0.51 | 3.2 | 1.73 1.30 | 0.53 0.38 | 1.25 0.85 | 0.36 0.23 | 19.50 18.55 | 6.48 6.20 | 2.54 | 7.62 | 3.60 3.05 | 8.25 7.80 | 10.0 8.3 | 0.254 | 0.76 |
| inches | 0.17 | 0.02 | 0.13 | 0.068 0.051 | 0.021 0.015 | 0.049 0.033 | 0.014 0.009 | 0.77 0.73 | 0.26 0.24 | 0.1 | 0.3 | 0.14 0.12 | 0.32 0.31 | 0.39 0.33 | 0.01 | 0.03 |

**Note**

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|---|---|---|---------------------|------------|
| | IEC | JEDEC | JEITA | | | |
| SOT38-4 | | | | | | 95-01-14 03-02-13 |

**Fig 9.  Package outline SOT38-4 (DIP16)**

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**SO16: plastic small outline package; 16 leads; body width 7.5 mm**

**SOT162-1**



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | A₁ | A₂ | A₃ | bₚ | c | D[1] | E[1] | e | H_E | L | Lₚ | Q | v | w | y | Z[1] | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2.65 | 0.3 0.1 | 2.45 2.25 | 0.25 | 0.49 0.36 | 0.32 0.23 | 10.5 10.1 | 7.6 7.4 | 1.27 | 10.65 10.00 | 1.4 | 1.1 0.4 | 1.1 1.0 | 0.25 | 0.25 | 0.1 | 0.9 0.4 | 8° 0° |
| inches | 0.1 | 0.012 0.004 | 0.096 0.089 | 0.01 | 0.019 0.014 | 0.013 0.009 | 0.41 0.40 | 0.30 0.29 | 0.05 | 0.419 0.394 | 0.055 | 0.043 0.016 | 0.043 0.039 | 0.01 | 0.01 | 0.004 | 0.035 0.016 | |

**Note**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT162-1 | 075E03 | MS-013 | | | | ~~99-12-27~~ 03-02-19 |

**Fig 10. Package outline SOT162-1 (SO16)**

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## 13. Revision history

**Table 11.   Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| HEF4517B v.7 | 20111111 | Product data sheet | - | HEF4517B v.6 |
| Modifications: | • Section Applications removed<br>• Table 6: $I_{OH}$ minimum values changed to maximum<br>• Figure 8: added "DUT = Device Under Test" | | | |
| HEF4517B v.6 | 20091210 | Product data sheet | - | HEF4517B v.5 |
| HEF4517B v.5 | 20090728 | Product data sheet | - | HEF4517B v.4 |
| HEF4517B v.4 | 20090406 | Product data sheet | - | HEF4517B_CNV v.3 |
| HEF4517B_CNV v.3 | 19950101 | Product specification | - | HEF4517B_CNV v.2 |
| HEF4517B_CNV v.2 | 19950101 | Product specification | - | - |

## 14. Legal information

### 14.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
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| Product [short] data sheet | Production | This document contains the product specification. |

[1]  Please consult the most recently issued document before initiating or completing a design.

[2]  The term 'short data sheet' is explained in section "Definitions".

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