Freescale Semiconductor
Data Sheet: Technical Data

Document Number: PXN20
Rev. 1, 09/2011

RoHS

PXN20 PXN21

PXN20 Microcontroller Data Sheet

MAPBGA–208
17 mm x 17 mm

PXN20 features:

- 32-bit CPU core complex (e200z650)
  - Compliant with Power Architecture embedded category
  - 32 KB unified cache with line locking and eight-entry store buffer16
  - Execution speed static to 116 MHz
- 32-bit I/O processor (e200z0)
  - Execution speed static to 1/2 CPU core speed (58 MHz)
- 2 MB on-chip flash
  - Supports read during program and erase operations, and multiple blocks allowing EEPROM emulation
- 512 KB + 80 KB (592 KB) on-chip ECC SRAM (PXN20)
- 128 KB on-chip ECC SRAM (PXN21)
- 16-entry Memory Protection Unit (PXN21 only)
- Direct memory access controller
  - 16-channel on PXN20
  - 32-channel on PXN21
- Fast ethernet controller
  - Supports 10-Mbps and 100-Mbps IEEE 802.3 MII, 10-Mbps 7-wire interface
  - IEEE 802.3 MAC (compliant with IEEE 802.3 1998 edition)
- Media Local Bus (MLB) interface (PXN20 only)
  - Supports 16 logical channels, max speed 1024 Fs
- Interrupt controller (INTC) supports 316 external interrupt vectors (22 are reserved)
- System clocks
  - Frequency-modulated phase-locked loop (FMPLL)
  - 4 – 40 MHz crystal oscillator (XTAL)
  - 32 kHz crystal oscillator (XTAL)
  - Dedicated 16 MHz and 128 kHz internal RC oscillators
- Analog to Digital Converter (ADC) module
  - 10-bit A/D resolution
  - 32 external channels
  - 36 internal channels (PXN20)
  - 64 internal channels (PXN21)
- Cross-Triggering Unit (PXN21 only)
  - Internal conversion triggering for ADC
  - Triggerable by internal timers or eMIOS200
- Deserial Serial Peripheral Interface (DSPI)
  - Four individual DSPI modules
  - Full duplex, synchronous transfers
  - Master or slave operation
- Inter-IC communication (I^2C) interface
  - Four individual I^2C modules
  - Multi-master operation
- Serial Communication Interface (eSCI) module
  - Two-channel DMA interface
  - Configurable as LIN bus master
- eMIOS200 timed input/output
  - 24 channels, 16-bit timers (PXN20)
  - 32 channels, 16-bit timers (PXN21)
- Controller Area Network (FlexCAN) module
  - Compliant with CAN protocol specification, Version 2.0B active
  - 64 mailboxes, each configurable as transmit or receive
- Dual-channel FlexRay controller
  - Full implementation of FlexRay Protocol Specification 2.1, RevA
  - 128 message buffers
- JTAG controller (PXN20 only)
  - Compliant with the IEEE 1149.1-2001
- Nexus Development Interface (NDI)
  - Available in 256 MAPBGA package only
  - Compliant with IEEE-ISTO 5001-2003
  - Nexus class 3 development support on e200z650
  - Nexus class 2+ development support on e200z0
- Internal voltage regulator allows operation from single 3.3 V or 5 V supply

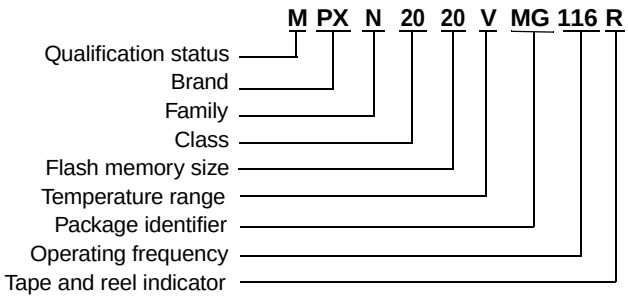
freescale™ semiconductor

Table of Contents

1 Ordering information

1.1 Orderable parts

Table 1 shows the orderable part numbers for the PXN20 family.



Qualification status
P = Pre-qualification (engineering samples)
M = Fully spec. qualified, general market flow
S = Fully spec. qualified, automotive flow

Family
D = Display Graphics
N = Connectivity/Network
R = Performance/Real Time Control
S = Safety

Flash Memory Size
20 = 2 MB

Temperature range
V = –40 °C to 105 °C (ambient)

Package identifier
MG = 208 MAPBGA

Operating frequency
116 = 116 MHz

Tape and reel status
R = Tape and reel
(blank) = Trays

Note: Not all options are available on all devices. See Table 1 for more information.

Figure 1. PXN20 orderable part number description

Table 1. PXN20 orderable part number summary

Part number	Flash/SRAM	Package	Speed (MHz)
MPXN2020VMG116	2 MB / 592 KB	208 MAPBGA (17 mm x 17 mm)	116
MPXN2120VMG116	2 MB / 128 KB	208 MAPBGA (17 mm x 17 mm)	116

1.2 PXN20 family feature set

Table 2. PXN20 family feature set

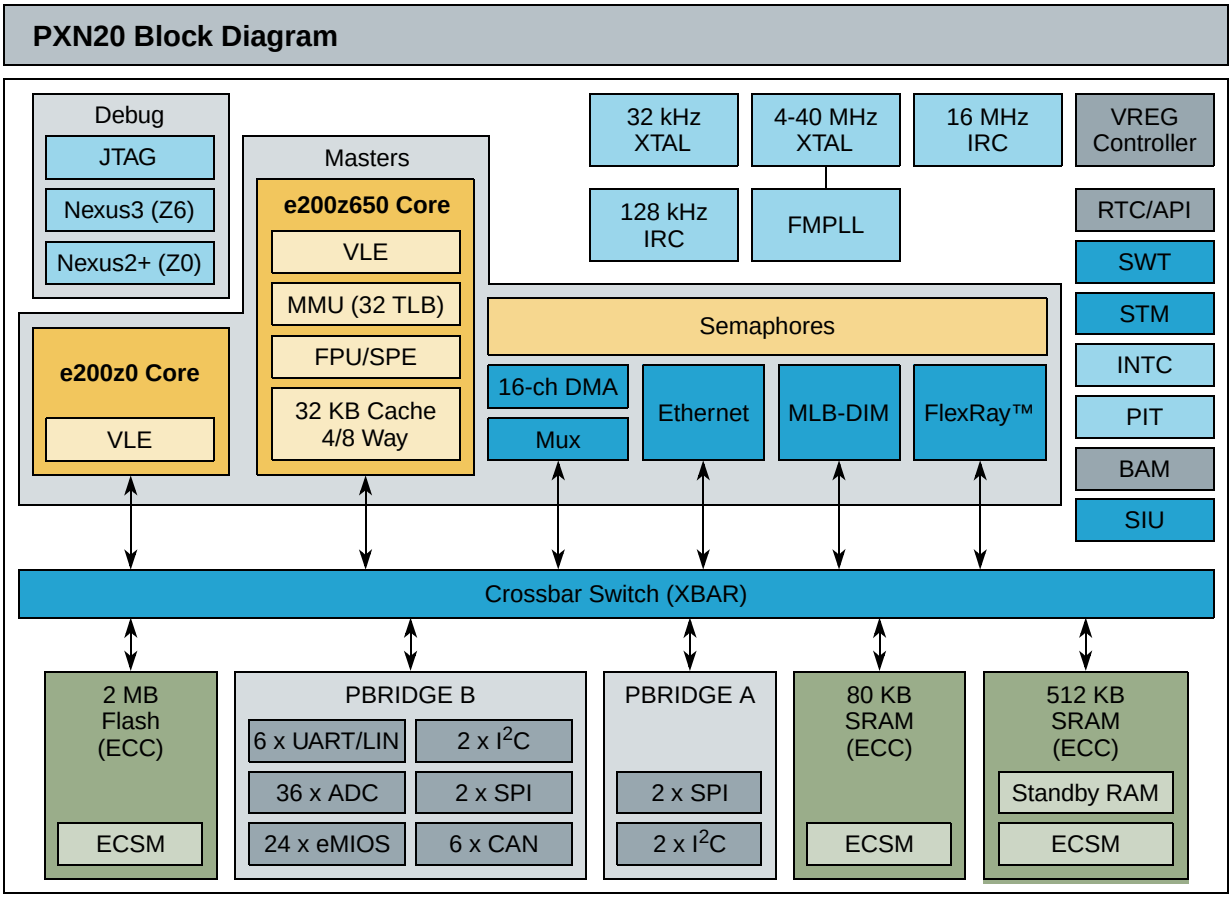
Feature	PXN20	PXN21
Central Processing Unit (CPU)	e200z650	e200z650
Cache	32K, 4/8way	32K, 4/8way
Floating Point Unit (FPU)	Yes	Yes
Signal Processing Engine (SPE)	Yes	Yes
Memory Management Unit (MMU)	32 entry	32 entry

Table 2. PXN20 family feature set (continued)

Feature	PXN20	PXN21
CPU Execution Speed	Static, 116 MHz	Static, 116 MHz
Input/Output Processor (IOP)	e200z0	e200z0
IOP Execution Speed	1/2 CPU execution speed	1/2 CPU execution speed
Flash with ECC	2 MB	2 MB
Data Flash Block	8x16 KB	8x16 KB
RAM with ECC	592 KB	128 KB
Memory Protection Unit (MPU)	No	16 entry
Direct Memory Access Unit (eDMA)	16 Channel	32 Channel
Ethernet (FEC)	Yes	No
MediaLB (MLB-DIM)	Yes	No
FlexRay Controller	Yes (128 Message Buffers)	No
Analog-to-Digital Converter (ADC)	36 internal channels, 10-bit Supports 32 external channels	64 internal channels, 10-bit Supports 32 external channels
Total Timer I/O (eMIOS200)	24 channels, 16-bit	32 channels, 16-bit
Cross Trigger Unit (CTU)	No	Yes
Asynchronous Serial Interfaces (UART)	6	12
Synchronous Serial Interfaces (SPI)	4	4
Controller Area Network (CAN) Controller	6	5
Inter-Integrated Circuit (I^2C) Controller	4	4
Frequency Modulated PLL (FMPLL)	Yes	Yes
4 – 40 MHz XTAL Oscillator	Yes	Yes
16 MHz IRC Oscillator	Yes	Yes
32 kHz XTAL Oscillator	Yes	Yes
128 kHz IRC Oscillator	Yes	Yes
Real Time Counter/ Autonomous Periodic Interrupts (RTC/API)	Yes	Yes
Periodic Interrupt Timer (PIT)	8	8
System Timer Module (STM)	Yes	Yes
Software Watchdog Timer (SWT)	Yes	Yes
General-Purpose I/O (GPIO)	155	155
Clock Monitor (FMPLL)	Yes	Yes
JTAG	Yes	Yes
Nexus Debug (Only supported on emulation package)	Nexus3 (e200Z6) Nexus2+ (e200Z0)	Nexus3 (e200Z6) Nexus2+ (e200Z0)
Production Package	208 MAPBGA	208 MAPBGA
Emulation Package (for development use only)	256 MAPBGA	256 MAPBGA

2 PXN20 block diagrams

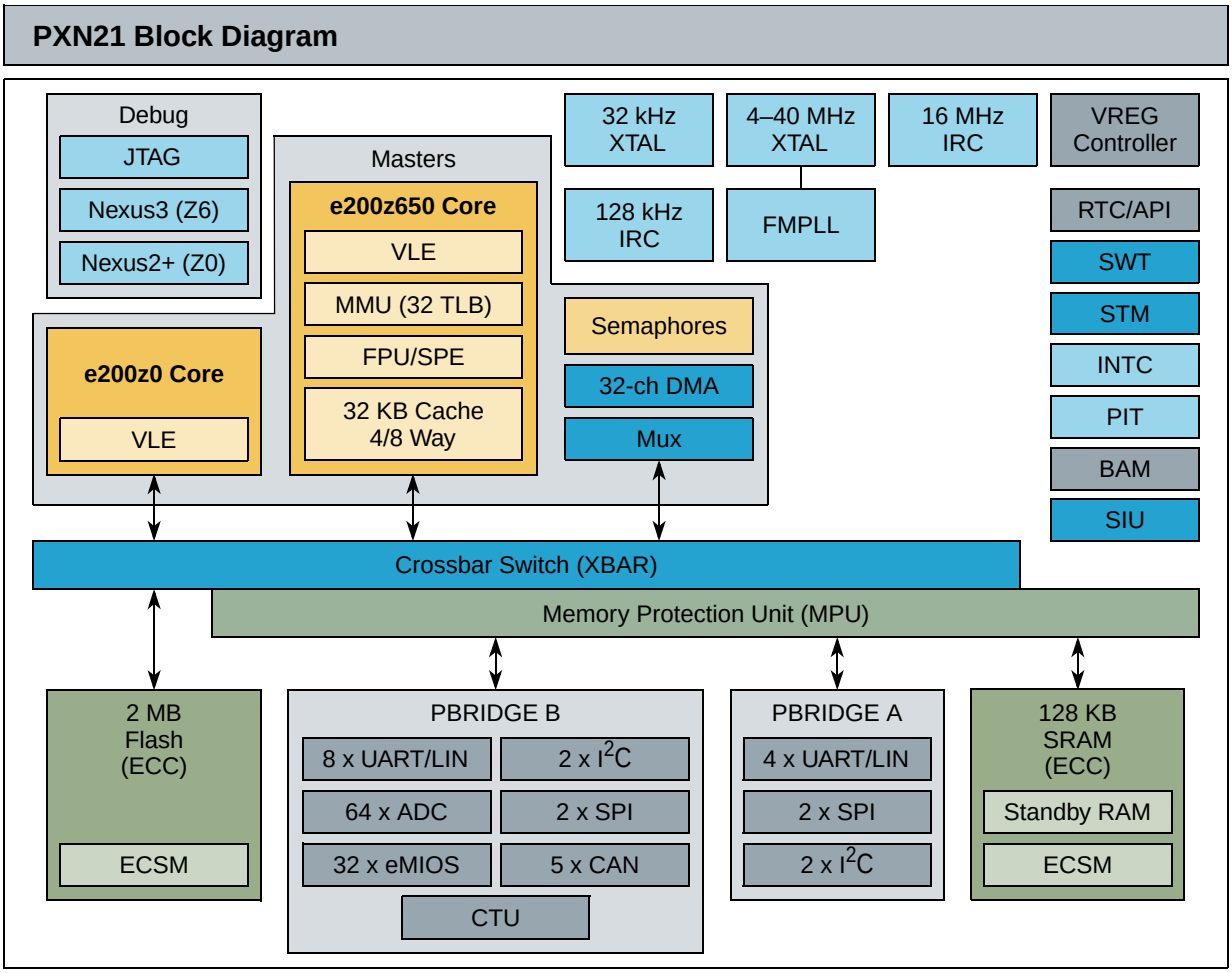
Figure 2 shows a top-level block diagram of the PXN20 device.



ADC – Analog-to-digital converter
BAM – Boot assist module
CAN – Controller area network controller
ECC – Error correction code
ECSM – Error correction status module
eMIOS – Timed input/output
eDMA – Enhanced direct memory access controller
FEC – Fast ethernet controller
FlexRay™ – FlexRay bus controller
FMPLL – Frequency-modulated phase-locked loop
I²C – Inter-integrated circuit controller
INTC – Interrupt controller
JTAG – Joint Test Action Group interface
MLB-DIM – Media Local Bus device interface module
NDI – Nexus debug interface
PBRIDGE – Peripheral I/O bridge
PIT – Periodic interrupt timer
RTC – Real time clock
SIU – System integration unit
SPI – Serial peripheral interface controller
STM – System timer module
SWT – Software watchdog timer
UART/LIN – Universal asynchronous receiver/transmitter/ local interconnect network
VREG – Voltage regator

Figure 2. PXN20 block diagram

Figure 3 shows a top level block diagram for the PXN21 device.



ADC – Analog-to-digital converter
BAM – Boot assist module
CAN – Controller area network controller
CTU – Cross triggering unit
ECC – Error correction code
ECSM – Error correction status module
eDMA – Enhanced direct memory access controller
eMIOS – Timed input/output
FMPLL – Frequency-modulated phase-locked loop
I2C – Inter-integrated circuit controller
INTC – Interrupt controller
JTAG – Joint Test Action Group interface
MPU – Memory protection unit
NDI – Nexus debug interface
PBRIDGE – Peripheral I/O bridge
PIT – Periodic interrupt timer
RTC – Real time clock
SIU – System integration unit
SPI – Serial peripheral interface controller
STM – System timer module
SWT – Software watchdog timer
UART/LIN – Universal asynchronous receiver/transmitter/ local interconnect network
VREG – Voltage regulator

Figure 3. PXN21 block diagram

3 Pin assignments

3.1 208-ball MAPBGA pin assignments

Figure 4 shows the 208-ball MAPBGA pin assignments.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	V_{SS}	PD0	PG1	PC12	PC9	PC7	PC2	PB13	PB10	PB8	RESET	V_{DDSYN}	XTAL	EXTAL	V_{SSSYN}	V_{SS}	A
B	PD2	PD1	PG0	PC11	PC10	PC8	PC3	PB14	PB11	V_{RC}	V_{RCCTL}	PB9	PB2	PB0	V_{DDA}	V_{RH}	B
C	PD3	PD4	PD14	PC14	PC13	PC5	PC6	PC1	PB15	PB12	PB6	PB4	PB3	PB1	V_{SSA}	V_{RL}	C
D	PD5	PD6	PD15	V_{DD}	PC15	V_{DDE1}	V_{SS}	PC4	PC0	V_{DD}	PB7	PB5	PA10	PA12	PA0	PA14	D
E	PD7	PD8	PE0	PE1									PA11	PA9	PA1	PA15	E
F	PD9	PD10	PE3	PE2									PA13	PA8	PA3	PA2	F
G	PD11	PD12	PE4	V_{SS}				V_{SS}	V_{SS}	V_{SS}	V_{SS}		V_{DD}	PA7	PA5	PA4	G
H	PD13	PF0	PE5	V_{DD}				V_{SS}	V_{SS}	V_{SS}	V_{SS}		V_{RCSEL}	PG2	PG6	PA6	H
J	PF1	PF2	TDI	PE8				V_{SS}	V_{SS}	V_{SS}	V_{SS}		V_{DDE3}	PG3	PG7	PG11	J
K	PK1	PK2	JCOMP	V_{DDEMLB}				V_{SS}	V_{SS}	V_{SS}	V_{SS}		V_{DD}	PG4	PG8	PG12	K
L	PK0	PE7	TMS	V_{DDE2}									V_{DD33}	PG5	PG9	PG13	L
M	PF4	PE6	TDO	PE9									TEST	PF13	PG10	PG14	M
N	PF6	PF3	PE10	PE11	V_{DD}	PE15	PE14	PH9	PH11	V_{DDE4}	PH15	PJ10	V_{SS}	PF12	PH3	PG15	N
P	PF8	PF5	TCK	PE12	PE13	PK10	PH8	PH10	PH12	PH13	PH14	PJ11	PF15	PF14	PH4	PH1	P
R	PF10	PF7	PF11	PK4	PK6	PK8	PJ0	PJ2	PJ4	PJ6	PJ9	PJ12	PJ14	PH5	PH6	PH2	R
T	V_{SS}	PF9	PK3	PK5	PK7	PK9	PJ1	PJ3	PJ5	PJ7	PJ8	PJ13	PJ15	PH0	PH7	V_{SS}	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Figure 4. PXN20 208-ball MAPBGA (full diagram)

3.2 Pin muxing and reset states

Table 3 shows the signals properties for each pin on PXN20. For all port pins that have an associated SIU_PCR*n* register to control pin properties, the supported functions column lists the functions associated with the programming of the SIU_PCR*n*[PA] bit in the order: general-purpose input/output (GPIO), function 1, function 2, and function 3 (see Figure 5). When an alternate function is not implemented for a value of SIU_PCR*n*[PA], a dash is shown in the Description column and the respective value in the PA bit field is reserved.

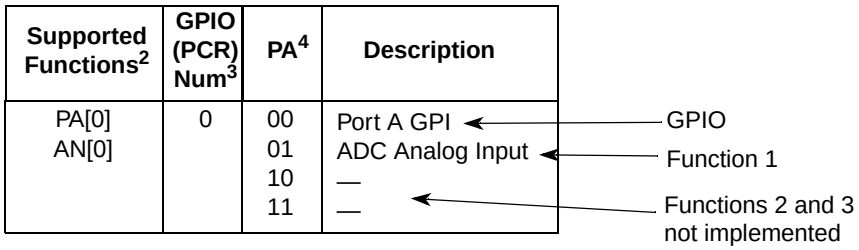


Figure 5. Supported functions example

Table 3. PXN20 signal properties

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Volt-age	Pad Type[5]	Status		Package Pin Locations
								During Reset[6]	After Reset[7]	208 BGA
Port A (16)										
PA0	PA[0] AN[0]	0	00 01 10 11	Port A GPI ADC Analog Input — —	I I — —	V_{DDA}	IHA	—	—	D15
PA1	PA[1] AN[1]	1	00 01 10 11	Port A GPI ADC Analog Input — —	I I — —	V_{DDA}	IHA	—	—	E15
PA2	PA[2] AN[2]	2	00 01 10 11	Port A GPI ADC Analog Input — —	I I — —	V_{DDA}	IHA	—	—	F16
PA3	PA[3] AN[3]	3	00 01 10 11	Port A GPI ADC Analog Input — —	I I — —	V_{DDA}	IHA	—	—	F15
PA4	PA[4] AN[4]	4	00 01 10 11	Port A GPI ADC Analog Input — —	I I — —	V_{DDA}	IHA	—	—	G16
PA5	PA[5] AN[5]	5	00 01 10 11	Port A GPI ADC Analog Input — —	I I — —	V_{DDA}	IHA	—	—	G15

Table 3. PXN20 signal properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Volt-age	Pad Type[5]	Status		Package Pin Locations
								During Reset[6]	After Reset[7]	208 BGA
PA6	PA[6] AN[6]	6	00 01 10 11	Port A GPI ADC Analog Input — —	I I — —	V_{DDA}	IHA	—	—	H16
PA7	PA[7] AN[7]	7	00 01 10 11	Port A GPI ADC Analog Input — —	I I — —	V_{DDA}	IHA	—	—	G14
PA8	PA[8] AN[8]	8	00 01 10 11	Port A GPI ADC Analog Input — —	I I — —	V_{DDA}	IHA	—	—	F14
PA9	PA[9] AN[9]	9	00 01 10 11	Port A GPI ADC Analog Input — —	I I — —	V_{DDA}	IHA	—	—	E14
PA10	PA[10] AN[10]	10	00 01 10 11	Port A GPI ADC Analog Input — —	I I — —	V_{DDA}	IHA	—	—	D13
PA11	PA[11] AN[11]	11	00 01 10 11	Port A GPI ADC Analog Input — —	I I — —	V_{DDA}	IHA	—	—	E13
PA12	PA[12] AN[12]	12	00 01 10 11	Port A GPI ADC Analog Input — —	I I — —	V_{DDA}	IHA	—	—	D14
PA13	PA[13] AN[13]	13	00 01 10 11	Port A GPI ADC Analog Input — —	I I — —	V_{DDA}	IHA	—	—	F13
PA14	PA[14] AN[14] EXTAL32	14	00 01 10 11	Port A GPI ADC Analog Input External 32 kHz Crystal In —	I I I —	V_{DDA}	IHA	—	—	D16
PA15	PA[15] AN[15] XTAL32	15	00 01 10 11	Port A GPI ADC Analog Input External 32 kHz Crystal Out —	I I O —	V_{DDA}	IHA	—	—	E16

Table 3. PXN20 signal properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Volt-age	Pad Type[5]	Status		Package Pin Locations
								During Reset[6]	After Reset[7]	208 BGA
Port B (16)										
PB0	PB[0] AN[16]/ANW	16	00 01 10 11	Port B GPIO ADC Analog Input/Mux In — —	I/O I — —	V_{DDE1}	SHA	—	—	B14
PB1	PB[1] AN[17]/ANX	17	00 01 10 11	Port B GPIO ADC Analog Input/Mux In — —	I/O I — —	V_{DDE1}	SHA	—	—	C14
PB2	PB[2] AN[18]/ANY	18	00 01 10 11	Port B GPIO ADC Analog Input/Mux In — —	I/O I — —	V_{DDE1}	SHA	—	—	B13
PB3	PB[3] AN[19]/ANZ	19	00 01 10 11	Port B GPIO ADC Analog Input/Mux In — —	I/O I — —	V_{DDE1}	SHA	—	—	C13
PB4	PB[4] AN[20]	20	00 01 10 11	Port B GPIO ADC Analog Input — —	I/O I — —	V_{DDE1}	SHA	—	—	C12
PB5	PB[5] AN[21]	21	00 01 10 11	Port B GPIO ADC Analog Input — —	I/O I — —	V_{DDE1}	SHA	—	—	D12
PB6	PB[6] AN[22]	22	00 01 10 11	Port B GPIO ADC Analog Input — —	I/O I — —	V_{DDE1}	SHA	—	—	C11
PB7	PB[7] AN[23]	23	00 01 10 11	Port B GPIO ADC Analog Input — —	I/O I — —	V_{DDE1}	SHA	—	—	D11
PB8	PB[8] AN[24] PCS_A[2]	24	00 01 10 11	Port B GPIO ADC Analog Input DSPI_A Peripheral Chip Select —	I/O I O —	V_{DDE1}	SHA	—	—	A10
PB9	PB[9] AN[25] PCS_A[3]	25	00 01 10 11	Port B GPIO ADC Analog Input DSPI_A Peripheral Chip Select —	I/O I O —	V_{DDE1}	SHA	—	—	B12

Table 3. PXN20 signal properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Volt-age	Pad Type[5]	Status		Package Pin Locations
								During Reset[6]	After Reset[7]	208 BGA
PB10	PB[10] AN[26] PCS_B[4]	26	00 01 10 11	Port B GPIO ADC Analog Input DSPI_B Peripheral Chip Select —	I/O I O —	V_{DDE1}	SHA	—	—	A9
PB11	PB[11] AN[27] PCS_B[5]	27	00 01 10 11	Port B GPIO ADC Analog Input DSPI_B Peripheral Chip Select —	I/O I O —	V_{DDE1}	SHA	—	—	B9
PB12	PB[12] AN[28] PCS_C[1]	28	00 01 10 11	Port B GPIO ADC Analog Input DSPI_C Peripheral Chip Select —	I/O I O —	V_{DDE1}	SHA	—	—	C10
PB13	PB[13] AN[29] PCS_C[2]	29	00 01 10 11	Port B GPIO ADC Analog Input DSPI_C Peripheral Chip Select —	I/O I O —	V_{DDE1}	SHA	—	—	A8
PB14	PB[14] AN[30] PCS_D[3]	30	00 01 10 11	Port B GPIO ADC Analog Input DSPI_D Peripheral Chip Select —	I/O I O —	V_{DDE1}	SHA	—	—	B8
PB15	PB[15] AN[31] PCS_D[4]	31	00 01 10 11	Port B GPIO ADC Analog Input DSPI_D Peripheral Chip Select —	I/O I O —	V_{DDE1}	SHA	—	—	C9
Port C (16)										
PC0	PC[0] AN[32]	32	00 01 10 11	Port C GPIO ADC Analog Input — —	I/O I — —	V_{DDE1}	SHA	—	—	D9
PC1	PC[1] AN[33]	33	00 01 10 11	Port C GPIO ADC Analog Input — —	I/O I — —	V_{DDE1}	SHA	—	—	C8
PC2	PC[2] AN[34] EVTI	34	00 01 10 11	Port C GPIO ADC Analog Input Nexus Event In —	I/O I I —	V_{DDE1}	SHA	—	—	A7
PC3	PC[3] AN[35] EVTO	35	00 01 10 11	Port C GPIO ADC Analog Input Nexus Event Out —	I/O I O —	V_{DDE1}	SHA	—	—	B7

Table 3. PXN20 signal properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Volt-age	Pad Type[5]	Status		Package Pin Locations
								During Reset[6]	After Reset[7]	208 BGA
PC4	PC[4] AN[36]	36	00 01 10 11	Port C GPIO ADC Analog Input — —	I/O I — —	V_{DDE1}	SHA	—	—	D8
PC5	PC[5] AN[37] Z6NMI	37	00 01 10 11	Port C GPIO ADC Analog Input Z6 Core Non-Maskable Interrupt —	I/O I I —	V_{DDE1}	SHA	—	—	C6
PC6	PC[6] AN[38] Z0NMI	38	00 01 10 11	Port C GPIO ADC Analog Input Z0 Core Non-Maskable Interrupt —	I/O I I —	V_{DDE1}	SHA	—	—	C7
PC7	PC[7] AN[39] FR_DBG3	39	00 01 10 11	Port C GPIO ADC Analog Input FlexRay Debug —	I/O I O —	V_{DDE1}	SHA	—	—	A6
PC8	PC[8] AN[40] FR_DBG2	40	00 01 10 11	Port C GPIO ADC Analog Input FlexRay Debug —	I/O I O —	V_{DDE1}	SHA	—	—	B6
PC9	PC[9] AN[41] FR_DBG1	41	00 01 10 11	Port C GPIO ADC Analog Input FlexRay Debug —	I/O I O —	V_{DDE1}	SHA	—	—	A5
PC10	PC[10] AN[42] FR_DBG0	42	00 01 10 11	Port C GPIO ADC Analog Input FlexRay Debug —	I/O I O —	V_{DDE1}	SHA	—	—	B5
PC11	PC[11] AN[43] SCL_C	43	00 01 10 11	Port C GPIO ADC Analog Input I^2C_C Serial Clock —	I/O I I/O —	V_{DDE1}	SHA	—	—	B4
PC12	PC[12] AN[44] SDA_C	44	00 01 10 11	Port C GPIO ADC Analog Input I^2C_C Serial Data —	I/O I I/O —	V_{DDE1}	SHA	—	—	A4
PC13	PC[13] AN[45] — MA[0]	45	00 01 10 11	Port C GPIO ADC Analog Input — ADC Ext. Mux Address Select	I/O I — O	V_{DDE1}	SHA	—	—	C5
PC14	PC[14] AN[46] MA[1]	46	00 01 10 11	Port C GPIO ADC Analog Input ADC Ext. Mux Address Select —	I/O I — O	V_{DDE1}	SHA	—	—	C4

Table 3. PXN20 signal properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Volt-age	Pad Type[5]	Status		Package Pin Locations
								During Reset[6]	After Reset[7]	208 BGA
PC15	PC[15] AN[47] MA[2]	47	00 01 10 11	Port C GPIO ADC Analog Input ADC Ext. Mux Address Select —	I/O I O —	V_{DDE1}	SHA	—	—	D5
Port D (16)										
PD0	PD[0] CNTX_A	48	00 01 10 11	Port D GPIO FlexCAN_A Transmit — —	I/O O — —	V_{DDE2}	SH	—	—	A2
PD1	PD[1] CNRX_A	49	00 01 10 11	Port D GPIO FlexCAN_A Receive — —	I/O I — —	V_{DDE2}	SH	—	—	B2
PD2	PD[2] CNTX_B	50	00 01 10 11	Port D GPIO FlexCAN_B Transmit — —	I/O O — —	V_{DDE2}	SH	—	—	B1
PD3	PD[3] CNRX_B	51	00 01 10 11	Port D GPIO FlexCAN_B Receive — —	I/O I — —	V_{DDE2}	SH	—	—	C1
PD4	PD[4] CNTX_C	52	00 01 10 11	Port D GPIO FlexCAN_C Transmit — —	I/O O — —	V_{DDE2}	SH	—	—	C2
PD5	PD[5] CNRX_C	53	00 01 10 11	Port D GPIO FlexCAN_C Receive — —	I/O I — —	V_{DDE2}	SH	—	—	D1
PD6	PD[6] CNTX_D TXD_K SCL_B	54	00 01 10 11	Port D GPIO FlexCAN_D Transmit SCI_K Transmit I^2C_B Serial Clock	I/O O O I/O	V_{DDE2}	SH	—	—	D2
PD7	PD[7] CNRX_D RXD_K SDA_B	55	00 01 10 11	Port D GPIO FlexCAN_D Receive SCI_K Receive I^2C_B Serial Data	I/O I I I/O	V_{DDE2}	SH	—	—	E1
PD8	PD[8] CNTX_E TXD_L SCL_C	56	00 01 10 11	Port D GPIO FlexCAN_E Transmit SCI_L Transmit I^2C_C Serial Clock	I/O O O I/O	V_{DDE2}	SH	—	—	E2

Table 3. PXN20 signal properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Volt-age	Pad Type[5]	Status		Package Pin Locations
								During Reset[6]	After Reset[7]	208 BGA
PD9	PD[9] CNRX_E RXD_L SDA_C	57	00 01 10 11	Port D GPIO FlexCAN_E Receive SCI_L Receive I^2C_C Serial Data	I/O I I I/O	V_{DDE2}	SH	—	—	F1
PD10	PD[10] CNTX_F TXD_M SCL_D	58	00 01 10 11	Port D GPIO FlexCAN_F Transmit SCI_M Transmit I^2C_D Serial Clock	I/O O O I/O	V_{DDE2}	SH	—	—	F2
PD11	PD[11] CNRX_F RXD_M SDA_D	59	00 01 10 11	Port D GPIO FlexCAN_F Receive SCI_M Receive I^2C_D Serial Data	I/O I I I/O	V_{DDE2}	SH	—	—	G1
PD12	PD[12] TXD_A	60	00 01 10 11	Port D GPIO eSCI_A Transmit — —	I/O O — —	V_{DDE2}	SH	—	—	G2
PD13	PD[13] RXD_A	61	00 01 10 11	Port D GPIO eSCI_A Receive — —	I/O I — —	V_{DDE2}	SH	—	—	H1
PD14	PD[14] TXD_B	62	00 01 10 11	Port D GPIO eSCI_B Transmit — —	I/O O — —	V_{DDE2}	SH	—	—	C3
PD15	PD[15] RXD_B	63	00 01 10 11	Port D GPIO eSCI_B Receive — —	I/O I — —	V_{DDE2}	SH	—	—	D3
Port E (16)										
PE0	PE[0] TXD_C eMIOS[31]	64	00 01 10 11	Port E GPIO eSCI_C Transmit eMIOS Channel —	I/O O I/O —	V_{DDE2}	SH	—	—	E3
PE1	PE[1] RXD_C eMIOS[30]	65	00 01 10 11	Port E GPIO eSCI_C Receive eMIOS Channel —	I/O I I/O	V_{DDE2}	SH	—	—	E4
PE2	PE[2] TXD_D eMIOS[29]	66	00 01 10 11	Port E GPIO eSCI_D Transmit eMIOS Channel —	I/O O I/O	V_{DDE2}	SH	—	—	F4

Table 3. PXN20 signal properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Volt-age	Pad Type[5]	Status		Package Pin Locations
								During Reset[6]	After Reset[7]	208 BGA
PE3	PE[3] RXD_D eMIOS[28]	67	00 01 10 11	Port E GPIO eSCI_D Receive eMIOS Channel —	I/O I I/O	V_{DDE2}	SH	—	—	F3
PE4	PE[4] TXD_E eMIOS[27]	68	00 01 10 11	Port E GPIO eSCI_E Transmit eMIOS Channel —	I/O O I/O	V_{DDE2}	SH	—	—	G3
PE5	PE[5] RXD_E eMIOS[26]	69	00 01 10 11	Port E GPIO eSCI_E Receive eMIOS Channel —	I/O I I/O	V_{DDE2}	SH	—	—	H3
PE6	PE[6] TXD_F eMIOS[25]	70	00 01 10 11	Port E GPIO eSCI_F Transmit eMIOS Channel —	I/O O I/O	V_{DDE2}	SH	—	—	M2
PE7	PE[7] RXD_F eMIOS[24]	71	00 01 10 11	Port E GPIO eSCI_F Receive eMIOS Channel —	I/O I I/O	V_{DDE2}	SH	—	—	L2
PE8	PE[8] TXD_G PCS_A[1]	72	00 01 10 11	Port E GPIO eSCI_G Transmit DSPI_A Peripheral Chip Select —	I/O O O	V_{DDE2}	SH	—	—	J4
PE9	PE[9] RXD_G PCS_A[4]	73	00 01 10 11	Port E GPIO eSCI_G Receive DSPI_A Peripheral Chip Select —	I/O I O	V_{DDE2}	SH	—	—	M4
PE10	PE[10] TXD_H PCS_B[3]	74	00 01 10 11	Port E GPIO eSCI_H Transmit DSPI_B Peripheral Chip Select —	I/O O O	V_{DDE2}	SH	—	—	N3
PE11	PE[11] RXD_H PCS_B[2]	75	00 01 10 11	Port E GPIO eSCI_H Receive DSPI_B Peripheral Chip Select —	I/O I O	V_{DDE2}	SH	—	—	N4
PE12	PE[12] TXD_J PCS_C[5]	76	00 01 10 11	Port E GPIO eSCI_J Transmit DSPI_C Peripheral Chip Select —	I/O O O	V_{DDE2}	SH	—	—	P4
PE13	PE[13] RXD_J PCS_C[3]	77	00 01 10 11	Port E GPIO eSCI_J Receive DSPI_C Peripheral Chip Select —	I/O I O	V_{DDE2}	SH	—	—	P5

Table 3. PXN20 signal properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Volt-age	Pad Type[5]	Status		Package Pin Locations
								During Reset[6]	After Reset[7]	208 BGA
PE14	PE[14] SCL_A PCS_D[2]	78	00 01 10 11	Port E GPIO I^2C_A Serial Clock DSPI_D Peripheral Chip Select —	I/O I/O O —	V_{DDE2}	SH	—	—	N7
PE15	PE[15] SDA_A PCS_D[5]	79	00 01 10 11	Port E GPIO I^2C_A Serial Data DSPI_D Peripheral Chip Select —	I/O I/O O —	V_{DDE2}	SH	—	—	N6
Port F (16)										
PF0	PF[0] SCK_A	80	00 01 10 11	Port F GPIO DSPI_A Serial Clock — —	I/O I/O — —	V_{DDE2}	MH	—	—	H2
PF1	PF[1] SOUT_A	81	00 01 10 11	Port F GPIO DSPI_A Serial Data Out — —	I/O O — —	V_{DDE2}	MH	—	—	J1
PF2	PF[2] SIN_A	82	00 01 10 11	Port F GPIO DSPI_A Serial Data In — —	I/O I — —	V_{DDE2}	SH	—	—	J2
PF3	PF[3] PCS_A[0] PCS_B[5] PCS_C[4]	83	00 01 10 11	Port F GPIO DSPI_A Peripheral Chip Select DSPI_B Peripheral Chip Select DSPI_C Peripheral Chip Select	I/O I/O O O	V_{DDE2}	SH	—	—	N2
PF4	PF[4] SCK_B PCS_A[1] PCS_C[2]	84	00 01 10 11	Port F GPIO DSPI_B Serial Clock DSPI_A Peripheral Chip Select DSPI_C Peripheral Chip Select	I/O I/O O O	V_{DDE2}	MH	—	—	M1
PF5	PF[5] SOUT_B PCS_A[2] PCS_C[3]	85	00 01 10 11	Port F GPIO DSPI_B Serial Data Out DSPI_A Peripheral Chip Select DSPI_C Peripheral Chip Select	I/O O O O	V_{DDE2}	MH	—	—	P2
PF6	PF[6] SIN_B PCS_A[3] PCS_C[5]	86	00 01 10 11	Port F GPIO DSPI_B Serial Data In DSPI_A Peripheral Chip Select DSPI_C Peripheral Chip Select	I/O I O O	V_{DDE2}	SH	—	—	N1
PF7	PF[7] PCS_B[0] PCS_C[5] PCS_D[4]	87	00 01 10 11	Port F GPIO DSPI_B Peripheral Chip Select DSPI_C Peripheral Chip Select DSPI_D Peripheral Chip Select	I/O I/O O O	V_{DDE2}	SH	—	—	R2

Table 3. PXN20 signal properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Volt-age	Pad Type[5]	Status		Package Pin Locations
								During Reset[6]	After Reset[7]	208 BGA
PF8	PF[8] SCK_C	88	00 01 10 11	Port F GPIO DSPI_C Serial Clock — —	I/O I/O — —	V_{DDE2}	MH	—	—	P1
PF9	PF[9] SOUT_C	89	00 01 10 11	Port F GPIO DSPI_C Serial Data Out — —	I/O O — —	V_{DDE2}	MH	—	—	T2
PF10	PF[10] SIN_C	90	00 01 10 11	Port F GPIO DSPI_C Serial Data In — —	I/O I — —	V_{DDE2}	SH	—	—	R1
PF11	PF[11] PCS_C[0] PCS_D[5] PCS_A[4]	91	00 01 10 11	Port F GPIO DSPI_C Peripheral Chip Select DSPI_D Peripheral Chip Select DSPI_A Peripheral Chip Select	I/O I/O O O	V_{DDE2}	SH	—	—	R3
PF12	PF[12] SCK_D	92	00 01 10 11	Port F GPIO DSPI_D Serial Clock — —	I/O I/O — —	V_{DDE3}	MH	—	—	N14
PF13	PF[13] SOUT_D	93	00 01 10 11	Port F GPIO DSPI_D Serial Data Out — —	I/O O — —	V_{DDE3}	MH	—	—	M14
PF14	PF[14] SIN_D	94	00 01 10 11	Port F GPIO DSPI_D Serial Data In — —	I/O I — —	V_{DDE3}	SH	—	—	P14
PF15	PF[15] PCS_D[0] PCS_A[5] PCS_B[4]	95	00 01 10 11	Port F GPIO DSPI_D Peripheral Chip Select DSPI_A Peripheral Chip Select DSPI_B Peripheral Chip Select	I/O I/O O O	V_{DDE3}	SH	—	—	P13
Port G (16)										
PG0	PG[0] PCS_A[4] PCS_B[3] AN[48]	96	00 01 10 11	Port G GPIO DSPI_A Peripheral Chip Select DSPI_B Peripheral Chip Select ADC Analog Input	I/O O O I	V_{DDE2}	SHA	—	—	B3
PG1	PG[1] PCS_A[5] PCS_B[4] AN[49]	97	00 01 10 11	Port G GPIO DSPI_A Peripheral Chip Select DSPI_B Peripheral Chip Select ADC Analog Input	I/O O O I	V_{DDE2}	SHA	—	—	A3

Table 3. PXN20 signal properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Volt-age	Pad Type[5]	Status		Package Pin Locations
								During Reset[6]	After Reset[7]	208 BGA
PG2	PG[2] PCS_D[1] SCL_C AN[50]	98	00 01 10 11	Port G GPIO DSPI_D Peripheral Chip Select I^2C_C Serial Clock ADC Analog Input	I/O O I/O I	V_{DDE3}	SHA	—	—	H14
PG3	PG[3] PCS_D[2] SDA_C AN[51]	99	00 01 10 11	Port G GPIO DSPI_D Peripheral Chip Select I^2C_C Serial Data ADC Analog Input	I/O O I/O I	V_{DDE3}	SHA	—	—	J14
PG4	PG[4] PCS_D[3] SCL_B AN[52]	100	00 01 10 11	Port G GPIO DSPI_D Peripheral Chip Select I^2C_B Serial Clock ADC Analog Input	I/O O I/O I	V_{DDE3}	SHA	—	—	K14
PG5	PG[5] PCS_D[4] SDA_B AN[53]	101	00 01 10 11	Port G GPIO DSPI_D Peripheral Chip Select I^2C_B Serial Data ADC Analog Input	I/O O I/O I	V_{DDE3}	SHA	—	—	L14
PG6	PG[6] PCS_C[1] FEC_MDC AN[54]	102	00 01 10 11	Port G GPIO DSPI_C Peripheral Chip Select Ethernet Mgmt. Data Clock ADC Analog Input	I/O O O I	V_{DDE3}	MHA	—	—	H15
PG7	PG[7] PCS_C[2] FEC_MDIO AN[55]	103	00 01 10 11	Port G GPIO DSPI_C Peripheral Chip Select Ethernet Mgmt. Data I/O ADC Analog Input	I/O O I/O I	V_{DDE3}	MHA	—	—	J15
PG8	PG[8] eMIOS[7] FEC_TX_CLK AN[56]	104	00 01 10 11	Port G GPIO eMIOS Channel Ethernet Transmit Clock ADC Analog Input	I/O I/O I I	V_{DDE3}	SHA	—	—	K15
PG9	PG[9] eMIOS[6] FEC_CRS AN[57]	105	00 01 10 11	Port G GPIO eMIOS Channel Ethernet Carrier Sense ADC Analog Input	I/O I/O I I	V_{DDE3}	SHA	—	—	L15
PG10	PG[10] eMIOS[5] FEC_TX_ER AN[58]	106	00 01 10 11	Port G GPIO eMIOS Channel Ethernet Transmit Error ADC Analog Input	I/O I/O O I	V_{DDE3}	MHA	—	—	M15
PG11	PG[11] eMIOS[4] FEC_RX_CLK AN[59]	107	00 01 10 11	Port G GPIO eMIOS Channel Ethernet Receive Clock ADC Analog Input	I/O I/O I I	V_{DDE3}	SHA	—	—	J16
PG12	PG[12] eMIOS[3] FEC_TXD[0] AN[60]	108	00 01 10 11	Port G GPIO eMIOS Channel Ethernet Transmit Data ADC Analog Input	I/O I/O O I	V_{DDE3}	MHA	—	—	K16

Table 3. PXN20 signal properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Volt-age	Pad Type[5]	Status		Package Pin Locations
								During Reset[6]	After Reset[7]	208 BGA
PG13	PG[13] eMIOS[2] FEC_TXD[1] AN[61]	109	00 01 10 11	Port G GPIO eMIOS Channel Ethernet Transmit Data ADC Analog Input	I/O I/O O I	V_{DDE3}	MHA	—	—	L16
PG14	PG[14] eMIOS[1] FEC_TXD[2] AN[62]	110	00 01 10 11	Port G GPIO eMIOS Channel Ethernet Transmit Data ADC Analog Input	I/O I/O O I	V_{DDE3}	MHA	—	—	M16
PG15	PG[15] eMIOS[0] FEC_TXD[3] AN[63]	111	00 01 10 11	Port G GPIO eMIOS Channel Ethernet Transmit Data ADC Analog Input	I/O I/O O I	V_{DDE3}	MHA	—	—	N16
Port H (16)										
PH0	PH[0] eMIOS[31] FEC_COL	112	00 01 10 11	Port H GPIO eMIOS Channel Ethernet Collision —	I/O I/O I —	V_{DDE3}	SH	—	—	T14
PH1	PH[1] eMIOS[30] FEC_RX_DV	113	00 01 10 11	Port H GPIO eMIOS Channel Ethernet Receive Data Valid —	I/O I/O I —	V_{DDE3}	SH	—	—	P16
PH2	PH[2] eMIOS[29] FEC_TX_EN	114	00 01 10 11	Port H GPIO eMIOS Channel Ethernet Transmit Enable —	I/O I/O O —	V_{DDE3}	MH	—	—	R16
PH3	PH[3] eMIOS[28] FEC_RX_ER	115	00 01 10 11	Port H GPIO eMIOS Channel Ethernet Receive Error —	I/O I/O I —	V_{DDE3}	SH	—	—	N15
PH4	PH[4] eMIOS[27] FEC_RXD[0]	116	00 01 10 11	Port H GPIO eMIOS Channel Ethernet Receive Data —	I/O I/O I —	V_{DDE3}	SH	—	—	P15
PH5	PH[5] eMIOS[26] FEC_RXD[1]	117	00 01 10 11	Port H GPIO eMIOS Channel Ethernet Receive Data —	I/O I/O I —	V_{DDE3}	SH	—	—	R14
PH6	PH[6] eMIOS[25] FEC_RXD[2]	118	00 01 10 11	Port H GPIO eMIOS Channel Ethernet Receive Data —	I/O I/O I —	V_{DDE3}	SH	—	—	R15

Table 3. PXN20 signal properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Volt-age	Pad Type[5]	Status		Package Pin Locations
								During Reset[6]	After Reset[7]	208 BGA
PH7	PH[7] eMIOS[24] FEC_RXD[3]	119	00 01 10 11	Port H GPIO eMIOS Channel Ethernet Receive Data —	I/O I/O I —	V_{DDE3}	SH	—	—	T15
PH8	PH[8] eMIOS[23]	120	00 01 10 11	Port H GPIO eMIOS Channel — —	I/O I/O — —	V_{DDE4}	SH	—	—	P7
PH9	PH[9] eMIOS[22]	121	00 01 10 11	Port H GPIO eMIOS Channel — —	I/O I/O — —	V_{DDE4}	SH	—	—	N8
PH10	PH[10] eMIOS[21]	122	00 01 10 11	Port H GPIO eMIOS Channel — —	I/O I/O — —	V_{DDE4}	SH	—	—	P8
PH11	PH[11] eMIOS[20]	123	00 01 10 11	Port H GPIO eMIOS Channel — —	I/O I/O — —	V_{DDE4}	SH	—	—	N9
PH12	PH[12] eMIOS[19]	124	00 01 10 11	Port H GPIO eMIOS Channel — —	I/O I/O — —	V_{DDE4}	SH	—	—	P9
PH13	PH[13] eMIOS[18]	125	00 01 10 11	Port H GPIO eMIOS Channel — —	I/O I/O — —	V_{DDE4}	SH	—	—	P10
PH14	PH[14] eMIOS[17]	126	00 01 10 11	Port H GPIO eMIOS Channel — —	I/O I/O — —	V_{DDE4}	SH	—	—	P11
PH15	PH[15] eMIOS[16]	127	00 01 10 11	Port H GPIO eMIOS Channel — —	I/O I/O — —	V_{DDE4}	SH	—	—	N11
Port J (16)										
PJ0	PJ[0] eMIOS[15] PCS_A[4]	128	00 01 10 11	Port J GPIO eMIOS Channel DSPI_A Peripheral Chip Select —	I/O I/O O —	V_{DDE4}	SH	—	—	R7

Table 3. PXN20 signal properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Volt-age	Pad Type[5]	Status		Package Pin Locations
								During Reset[6]	After Reset[7]	208 BGA
PJ1	PJ[1] eMIOS[14] PCS_A[5]	129	00 01 10 11	Port J GPIO eMIOS Channel DSPI_A Peripheral Chip Select —	I/O I/O O —	V_{DDE4}	SH	—	—	T7
PJ2	PJ[2] eMIOS[13] PCS_B[1]	130	00 01 10 11	Port J GPIO eMIOS Channel DSPI_B Peripheral Chip Select —	I/O I/O O —	V_{DDE4}	SH	—	—	R8
PJ3	PJ[3] eMIOS[12] PCS_B[2]	131	00 01 10 11	Port J GPIO eMIOS Channel DSPI_B Peripheral Chip Select —	I/O I/O O —	V_{DDE4}	SH	—	—	T8
PJ4	PJ[4] eMIOS[11] PCS_C[3]	132	00 01 10 11	Port J GPIO eMIOS Channel DSPI_C Peripheral Chip Select —	I/O I/O O —	V_{DDE4}	SH	—	—	R9
PJ5	PJ[5] eMIOS[10] PCS_C[4]	133	00 01 10 11	Port J GPIO eMIOS Channel DSPI_C Peripheral Chip Select —	I/O I/O O —	V_{DDE4}	SH	—	—	T9
PJ6	PJ[6] eMIOS[09] PCS_D[5]	134	00 01 10 11	Port J GPIO eMIOS Channel DSPI_D Peripheral Chip Select —	I/O I/O O —	V_{DDE4}	SH	—	—	R10
PJ7	PJ[7] eMIOS[08] PCS_D[1]	135	00 01 10 11	Port J GPIO eMIOS Channel DSPI_D Peripheral Chip Select —	I/O I/O O —	V_{DDE4}	SH	—	—	T10
PJ8	PJ[8] eMIOS[07]	136	00 01 10 11	Port J GPIO eMIOS Channel — —	I/O I/O — —	V_{DDE4}	SH	—	—	T11
PJ9	PJ[9] eMIOS[06]	137	00 01 10 11	Port J GPIO eMIOS Channel — —	I/O I/O — —	V_{DDE4}	SH	—	—	R11
PJ10	PJ[10] eMIOS[05]	138	00 01 10 11	Port J GPIO eMIOS Channel — —	I/O I/O — —	V_{DDE4}	SH	—	—	N12
PJ11	PJ[11] eMIOS[04]	139	00 01 10 11	Port J GPIO eMIOS Channel — —	I/O I/O — —	V_{DDE4}	SH	—	—	P12

Table 3. PXN20 signal properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Volt-age	Pad Type[5]	Status		Package Pin Locations
								During Reset[6]	After Reset[7]	208 BGA
PJ12	PJ[12] eMIOS[03]	140	00 01 10 11	Port J GPIO eMIOS Channel — —	I/O I/O — —	V_{DDE4}	SH	—	—	R12
PJ13	PJ[13] eMIOS[02]	141	00 01 10 11	Port J GPIO eMIOS Channel — —	I/O I/O — —	V_{DDE4}	SH	—	—	T12
PJ14	PJ[14] eMIOS[01]	142	00 01 10 11	Port J GPIO eMIOS Channel — —	I/O I/O — —	V_{DDE4}	SH	—	—	R13
PJ15	PJ[15] eMIOS[00]	143	00 01 10 11	Port J GPIO eMIOS Channel — —	I/O I/O — —	V_{DDE4}	SH	—	—	T13
Port K (11)										
PK0	PK[0] MLBCLK SCK_B CLKOUT	144	00 01 10 11	Port K GPIO Media Local Bus Clock DSPI_B Serial Clock CLKOUT (Test Only)	I/O I I/O O	V_{DDEMLB}	F	—	—	L1
PK1	PK[1] MLBSIG SOUT_B PCS_D[4]	145	00 01 10 11	Port K GPIO Media Local Bus Signal DSPI_B Serial Data Out DSPI_D Peripheral Chip Select	I/O I/O O O	V_{DDEMLB}	F	—	—	K1
PK2	PK[2] MLBDAT SIN_B PCS_D[5]	146	00 01 10 11	Port K GPIO Media Local Bus Data DSPI_B Serial Data In DSPI_D Peripheral Chip Select	I/O I/O I O	V_{DDEMLB}	F	—	—	K2
PK3	PK[3] FR_A_RX MA[0] PCS_C[1]	147	00 01 10 11	Port K GPIO FlexRay A Receive Data ADC Ext. Mux Address Select DSPI_C Peripheral Chip Select	I/O I O O	V_{DDE2}	SH	—	—	T3
PK4	PK[4] FR_A_TX MA[1] PCS_C[2]	148	00 01 10 11	Port K GPIO FlexRay A Transmit Data ADC Ext. Mux Address Select DSPI_C Peripheral Chip Select	I/O O O O	V_{DDE2}	MH	—	—	R4
PK5	PK[5] FR_A_TX_EN MA[2] PCS_C[3]	149	00 01 10 11	Port K GPIO FlexRay A Transmit Enable ADC Ext. Mux Address Select DSPI_C Peripheral Chip Select	I/O O O O	V_{DDE2}	MH	—	—	T4

Table 3. PXN20 signal properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Volt-age	Pad Type[5]	Status		Package Pin Locations
								During Reset[6]	After Reset[7]	208 BGA
PK6	PK[6] FR_B_RX PCS_B[1] PCS_C[4]	150	00 01 10 11	Port K GPIO FlexRay B Receive Data DSPI_B Peripheral Chip Select DSPI_C Peripheral Chip Select	I/O I O O	V_{DDE2}	SH	—	—	R5
PK7	PK[7] FR_B_TX PCS_B[2] PCS_C[5]	151	00 01 10 11	Port K GPIO FlexRay B Transmit Data DSPI_B Peripheral Chip Select DSPI_C Peripheral Chip Select	I/O O O O	V_{DDE2}	MH	—	—	T5
PK8	PK[8] FR_B_TX_EN PCS_B[3] PCS_A[1]	152	00 01 10 11	Port K GPIO FlexRay B Transmit Enable DSPI_B Peripheral Chip Select DSPI_A Peripheral Chip Select	I/O O O O	V_{DDE2}	MH	—	—	R6
PK9	PK[9] CLKOUT PCS_D[1] PCS_A[2] BOOTCFG	153	00 01 10 11	Port K GPIO CLKOUT (User mode) DSPI_D Peripheral Chip Select DSPI_A Peripheral Chip Select Boot Configuration	I/O O O O I	V_{DDE2}	MH	BOOT CFG (Pull-down)	GPIO	T6
PK10	PK[10] PCS_B[5] PCS_D[2] PCS_A[3]	154	00 01 10 11	Port K GPIO DSPI_B Peripheral Chip Select DSPI_D Peripheral Chip Select DSPI_A Peripheral Chip Select	I/O O O O	V_{DDE2}	SH	—	—	P6
Miscellaneous Pins (9)										
EXTAL	EXTAL EXTCLK	—	—	Main Crystal Oscillator Input External Clock Input	I I	V_{DDSYN}	A	EXTAL		A14
XTAL	XTAL	—	—	Main Crystal Oscillator Output	O	V_{DDSYN}	A	XTAL		A13
TDI	TDI	—	—	JTAG Test Data Input	I	V_{DDE2}	SH	TDI (Pull Up)		J3
TDO	TDO	—	—	JTAG Test Data Output	O	V_{DDE2}	MH	TDO (Pull Up[8])		M3
TMS	TMS	—	—	JTAG Test Mode Select Input	I	V_{DDE2}	MH	TMS (Pull Up)		L3
TCK	TCK	—	—	JTAG Test Clock Input	I	V_{DDE2}	SH	TCK (Pull Down)		P3
JCOMP	JCOMP	—	—	JTAG Compliancy	I	V_{DDE2}	SH	JCOMP (Pull Down)		K3
TEST	TEST	—	—	Test Mode Select	I	V_{DDE3}	IH	TEST[9]		M13
$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	—	—	External Reset	I/O	V_{DDE1}	MH	$\overline{\text{RESET}}$ (Pull Up)		A11

1 The primary signal name is used as the pin label on the BGA map for identification purposes.

2 Each line in the Signal Name column corresponds to a separate signal function on the pin. For all device I/O pins, the primary, alternate, or GPIO signal functions are designated in the PA field of the System Integration Unit (SIU) PCR registers except where explicitly noted.

3 The GPIO number is the same as the corresponding pad configuration register (SIU_PCR*n*) number.

4 The PA bitfield in the SIU_PCR*n* register selects the signal function for the pin. A dash in the Description field of this table indicates that this value for PC is reserved on this pin, and should not be used.

[5] The pad type is indicated by one or more of the following abbreviations: A–analog, F—fast speed, H–high voltage, I—input-only, M–medium speed, S–slow speed. For example, pad type SH designates a slow high-voltage pad.

[6] The Status During Reset pin is sampled after the internal POR is negated. Prior to exiting POR, the signal has a high impedance. The terminology used in this column is: O – output, I – input, Up – weak pull up enabled, Down – weak pulldown enabled, Low – output driven low, High – output driven high. A dash on the left side of the slash denotes that both the input and output buffers for the pin are off. A dash on the right side of the slash denotes that there is no weak pull up/down enabled on the pin. The signal name to the left or right of the slash indicates the pin is enabled.

[7] The Function After Reset of a GPI function is general purpose input. A dash on the left side of the slash denotes that both the input and output buffers for the pin are off. A dash on the right side of the slash denotes that there is no weak pull up/down enabled on the pin.

[8] Pullup is enabled only when JCOMP is negated.

[9] Tie to V_{SS} for normal operation.

3.2.1 Power and ground supply summary

Table 4. PXN20 power/ground

Pin Name	Function Description	Voltage[1]	Package Pin Locations
			208
V_{DD}	Internal Logic Power	1.2 V	D4, D10, H4, G13, K13, N5
V_{DDE1}	External I/O Power	3.3–5.0 V	D6
V_{DDE2}			L4
V_{DDE3}			J13
V_{DDE4}			N10
V_{DDA}	Analog Power	3.3–5.0 V	B15
V_{DD33}	3.3 V I/O Power	3.3 V	L13
V_{DDEMLB}	Media Local Bus Power	2.5 or 3.3 V	K4
V_{RCSEL}	Voltage Regulator Select	V_{SSA} / V_{DDA}	H13
V_{RC}	Voltage Regulator Control Voltage	3.3–5.0 V	B10
V_{RCCTL}	Voltage Regulator Control Output	—[2]	B11
V_{DDSYN}	Clock Synthesizer Power	3.3 V	A12
V_{RH}	Analog High Voltage Reference	3.3–5.0 V	B16
V_{RL}	Analog Low Voltage Reference	0 V	C16
V_{SS}	Ground	0 V	A1, A16, D7, G4, G[7:10], H[7:10], J[7:10], K[7:10], N13, T1, T16
V_{SSA}	Analog Ground	0 V	C15
V_{SSSYN}	Clock Synthesizer Ground	0 V	A15

1 Nominal voltages.

2 Base current to external NPN power transistor. Voltage may vary.

4 Electrical characteristics

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the PXN20.

4.1 Maximum ratings

Table 5. Absolute maximum ratings[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	1.2 V Core Supply Voltage[2]	V_{DD}	–0.3	1.32[3]	V
2	3.3 V Clock Synthesizer Voltage[2, 4]	V_{DDSYN}	–0.3	3.6	V
3	3.3 V I/O Buffer Voltage [2, 4]	V_{DD33}	–0.3	3.6	V
4	3.3–5.0 V Voltage Regulator Control Voltage [2, 5, 6]	V_{RC}	–0.3	5.5	V
5	3.3–5.0 V Analog Supply Voltage (reference to V_{SSA}) [2, 5]	V_{DDA}	–0.3	5.5	V
6	3.3–5.0 V External I/O Supply Voltage [2, 5, 7]	V_{DDE1}[8] V_{DDE2}[8] V_{DDE3}[8] V_{DDE4}[8]	–0.3 –0.3 –0.3 –0.3	5.5 5.5 5.5 5.5	V
7	2.5–3.3 V External I/O Supply Voltage (MLB) [2, 4]	V_{DDEMLB}[8]	–0.3	3.6	V
9	DC Input Voltage[9] V_{DDE1}, V_{DDE2}, V_{DDE3}, V_{DDE4} V_{DDEMLB}, V_{DDENEX}	V_{IN}	 –1.0[10] –1.0[9]	 V_{DDEx} + 0.3 V[11] V_{DDEx} + 0.3 V[10]	V
10	Analog Reference High Voltage	V_{RH}	–0.3	Minimum of 5.5 or V_{DDA} + 0.3	V
11	Analog Reference Low Voltage	V_{RL}	–0.3	5.5	V
12	V_{SS} to V_{SSA} Differential Voltage	$V_{SS} – V_{SSA}$	–100	100	mV
13	V_{SS} to V_{SSSYN} Differential Voltage	$V_{SS} – V_{SSSYN}$	–100	100	mV
14	Maximum DC Digital Input Current[12] (per pin, applies to all digital F, MH, SH, and IH pins)	I_{MAXD}	–2	2	mA
15	Maximum DC Analog Input Current[13] (per pin, applies to all analog AE and A pins)	I_{MAXA}	–3	3	mA
16	Storage Temperature Range	T_{STG}	–55.0	150.0	°C
17	Maximum Solder Temperature[14]	T_{SDR}	—	235.0	°C
18	Moisture Sensitivity Level[15]	MSL	—	3	

1 Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.

2 Voltage overshoots during a high-to-low or low-to-high transition must not exceed 10 seconds per instance.

3 2.0 V for 10 hours cumulative time, 1.2 V +10% for time remaining.

4 5.3 V for 10 hours cumulative time, 3.3 V +10% for time remaining.

5 6.4 V for 10 hours cumulative time, 5.0 V +10% for time remaining.

6 VRC cannot be 100mV higher than VDDA. VDDSYN and VDD33 cannot be 100 mV higher than VRC.

7 All functional non-supply I/O pins are clamped to V_{SS} and V_{DDEx}.

[8] V_{DDEx} are separate power segments and may be powered independently with no differential voltage constraints between the power segments.

[9] AC signal over and undershoot of the input voltages of up to ±2.0 V is permitted for a cumulative duration of 60 hours over the complete lifetime of the device (injection current does not need to be limited for this duration).

[10] Internal structures will hold the input voltage above –1.0 V if the injection current limit of 2 mA is met.

[11] Internal structures hold the input voltage below this maximum voltage on all pads powered by V_{DDE} supplies, if the maximum injection current specification is met (25 mA for all pins) and V_{DDE} is within Operating Voltage specifications.

[12] Total injection current for all pins (including both digital and analog) must not exceed 25 mA.

[13] Total injection current for all analog input pins must not exceed 15 mA.

[14] Solder profile per CDF-AEC-Q100.

[15] Moisture sensitivity per JEDEC test method A112.

4.2 Thermal characteristics

Table 6. Thermal characteristics

Spec	Characteristic	Symbol	Unit	Value	
				208 MAPBGA	256 MAPBGA
1	Junction to Ambient[1, 2] Natural Convection (Single layer board)	$R_{\theta JA}$	°C/W	39	39
2	Junction to Ambient[1, 3] Natural Convection (Four layer board 2s2p)	$R_{\theta JA}$	°C/W	24	24
3	Junction to Ambient[1, 3] (@200 ft./min., Single layer board)	$R_{\theta JMA}$	°C/W	31	31
4	Junction to Ambient[1, 3] (@200 ft./min., Four layer board 2s2p)	$R_{\theta JMA}$	°C/W	20	20
5	Junction to Board[4]	$R_{\theta JB}$	°C/W	13	13
6	Junction to Case[5]	$R_{\theta JC}$	°C/W	6	6
7	Junction to Package Top[6] Natural Convection	Ψ_{JT}	°C/W	2	2

[1] Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

[2] Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.

[3] Per JEDEC JESD51-6 with the board horizontal.

[4] Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

[5] Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.

[6] Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

4.2.1 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D) \qquad \textit{Eqn. 1}$$

where:

T_A = ambient temperature for the package (^oC)

$R_{\theta JA}$ = junction to ambient thermal resistance ($^oC/W$)

P_D = power dissipation in the package (W)

The supplied thermal resistances are provided based on JEDEC JESD51 series of standards to provide consistent values for estimations and comparisons. The difference between the values determined on the single-layer (1s) board and on the four-layer board with two signal layers and a power and a ground plane (2s2p) clearly demonstrate that the effective thermal resistance of the component is not a constant. It depends on the construction of the application board (number of planes), the effective size of the board which cools the component, how well the component is thermally and electrically connected to the planes, and the power being dissipated by adjacent components.

Connect all the ground and power balls to the respective planes with one via per ball. Using fewer vias to connect the package to the planes reduces the thermal performance. Thinner planes also reduce the thermal performance. When the clearance between through vias leave the planes virtually disconnected, the thermal performance is also greatly reduced.

As a general rule, the value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the application board has one oz. (35 micron nominal thickness) internal planes, the components are well separated, and the overall power dissipation on the board is less than 0.02 W/cm^2.

The thermal performance of any component depends strongly on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D) \qquad \textit{Eqn. 2}$$

where:

T_J = junction temperature (^oC)

T_B = board temperature at the package perimeter ($^oC/W$)

$R_{\theta JB}$ = junction to board thermal resistance ($^oC/W$) per JESD51-8

P_D = power dissipation in the package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition, with the component soldered to a board with internal planes.

Historically, the thermal resistance has frequently been expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \qquad \textit{Eqn. 3}$$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance ($^oC/W$)

$R_{\theta JC}$ = junction to case thermal resistance ($^oC/W$)

$R_{\theta CA}$ = case to ambient thermal resistance ($^oC/W$)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the air flow around the device, add a heat sink, change the

mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This description is most useful for packages with heat sinks where some 90% of the heat flow is through the case to the heat sink to ambient. For most packages, a better model is required.

A more accurate two-resistor thermal model can be constructed from the junction to board thermal resistance and the junction to case thermal resistance. The junction to case covers the situation where a heat sink will be used or where a substantial amount of heat is dissipated from the top of the package. The junction to board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. This model can be used for either hand estimations or for a computational fluid dynamics (CFD) thermal model.

To determine the junction temperature of the device in the application after prototypes are available, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D) \qquad \textit{Eqn. 4}$$

where:

T_T = thermocouple temperature on top of the package (^oC)

Ψ_{JT} = thermal characterization parameter ($^oC/W$)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

References:

Semiconductor Equipment and Materials International
3081 Zanker Road
San Jose, CA 95134
(408) 943-6900

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the WEB at http://www.jedec.org.

1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
2. G. Kromann, S. Shidore, and S. Addison, “Thermal Modeling of a PBGA for Air-Cooled Applications,” Electronic Packaging and Production, pp. 53–58, March 1998.
3. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

4.3 ESD characteristics

Table 7. ESD ratings[1, 2]

Characteristic	Symbol	Value	Unit
ESD for Human Body Model (HBM)		2000	V
HBM Circuit Description	R1	1500	Ohm
	C	100	pF
ESD for Field Induced Charge Model (FDCM)		750 (corner pins)	V
		250 (all other pins)	
Number of Pulses per pin: Positive Pulses (HBM) Negative Pulses (HBM)	 — —	 1 1	 — —
Interval of Pulses	—	1	second

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

4.4 VRC electrical specifications

Table 8. VRC electrical specifications

Spec	Characteristic	Symbol	Min	Max	Units
1	Current which can be sourced by V_{RCCTL}	I_V_{RCCTL}	6.25 µA	20 mA	—
2	Minimum Required Gain from external circuit: I_{DD} / I_V_{RCCTL} (@V_{DD} = 1.32 V)[1] –40°C 25°C 150°C	BETA	 50 50 50	 500	

1 Assumes “typical usage” currents which will vary with application.

4.5 DC electrical specifications

Table 9. DC electrical specifications

Spec	Characteristic	Symbol	Min	Max	Unit
1	Maximum Operating Temperature Range — Die Junction Temperature	T_J	–40.0	150.0	^oC
2	3.3 V Clock Synthesizer Voltage[1]	V_{DDSYN}	3.0	3.6	V
3	3.3 V I/O Buffer Voltage[1]	V_{DD33}	3.0	3.6	V
4	3.3–5.0 V Voltage Regulator Reference Voltage[1] V_{RCSEL} = V_{SSA} V_{RCSEL} = V_{DDA}	V_{VRC}	 3.0 4.5	 3.6 5.5	V
5	3.3–5.0 V Analog Supply Voltage	V_{DDA}	maximum of 3.0 V or V_{VRC} – 0.1	5.5	V

Table 9. DC electrical specifications

Spec	Characteristic	Symbol	Min	Max	Unit
6	3.3–5.0 V External I/O Supply Voltage[2] V_{DDE1} V_{DDE2} V_{DDE3} V_{DDE4}		 3.0 3.0 3.0 3.0	 5.5 5.5 5.5 5.5	V
7	2.5 V – 3.3 V External I/O Supply Voltage (MLB)	V_{DDEMLB}[3]	2.375	3.6	V
9	Pad Input High Voltage Hysteresis enabled Hysteresis disabled (IHA/SH/SHA/MH/MHA)[4, 5] Hysteresis disabled (F)	V_{IH}	 0.65 × V_{DDE} 0.55 × V_{DDE} 0.55 × V_{DDE}	V_{DDE} + 0.3	V
10	Pad Input Low Voltage Hysteresis enabled Hysteresis disabled (IHA/SH/SHA/MH/MHA)[4, 5] Hysteresis disabled (F)	V_{IL}	V_{SS} – 0.3	 0.35 × V_{DDE} 0.40 × V_{DDE} 0.40 × V_{DDE}	V
11	Pad Input Hysteresis	V_{HYS}	0.1 × V_{DDE}		V
12	Analog (IHA) Input Voltage	V_{INDC}	V_{SSA} – 0.3	V_{DDA} + 0.3	V
13	Pad Output High Voltage[6, 7, 8]	V_{OH}	0.8 × V_{DDE}	—	V
14	Pad Output Low Voltage[8]	V_{OL}	—	0.2 × V_{DDE}	V
15	Input Capacitance (Digital Pins: Pad type F, MH, SH)[4]	C_{IN}	—	7	pF
16	Input Capacitance (Analog Pins: Pad type IHA)[4, 5]	C_{IN_A}	—	10	pF
17	Input Capacitance (Shared digital/analog pins: MHA, SHA)[4]	C_{IN_M}	—	12	pF
18	I/O Weak Pull Up/Down Absolute Current[4, 9] Pad F: 2.375 V – 3.6 V Pad SH/MH/IHA: 3.0 V – 3.6 V Pad SH/MH/IHA: 4.5 V – 5.5 V	I_{ACT}	 25 10 35	 180 95 200	µA
19	I/O Input Leakage Current[10]	I_{INACT_D}	–2.5	2.5	µA
20	DC Injection Current (per pin)	I_{IC}	–1.0	1.0	mA
21	Analog Input Current, Channel Off[11] (Analog pins IHA)[4, 5]	I_{INACT_A}	–150	150	nA
22	Analog Reference High Voltage	V_{RH}	V_{DDA} – 500	V_{DDA}	mV
23	Analog Reference Low Voltage	V_{RL}	V_{SSA}	V_{SSA} + 500	mV
24	V_{SS} to V_{SSA} Differential Voltage	$V_{SS} – V_{SSA}$	–100	100	mV
25	V_{SSSYN} to V_{SS} Differential Voltage	$V_{SSSYN} – V_{SS}$	–100	100	mV
26	Slew rate on V_{DDA}, V_{DDEx}, V_{DDSYN}, V_{DD33}, and V_{RC} power supply pins	V_{Ramp}	—	100	V/ms
27	Capacitive Supply Load (V_{DD})	V_{Load}	8	—	µF
28	Capacitive Supply Load (V_{DD33}, V_{DDSYN})	V_{Load}	1	—	µF

[1] When V_{RCSEL} = V_{SSA} (low), V_{DDSYN} and V_{DD33} are externally supplied. When V_{RCSEL} = V_{DDA} (high), V_{DDSYN} and V_{DD33} are generated by internal voltage regulators. When V_{RCSEL} = V_{SSA} (low), V_{DDSYN} and V_{DD33} cannot be 100 mV higher than V_{RC}.

2 $V_{DDE1} – V_{DDE4}$ are separate power segments and may be powered independently with no differential voltage constraints between the power segments. $V_{DDE1} – V_{DDE3}$ pad power segments contain ADC analog input channels and thus the input analog signal level may be clamped to the V_{DDE} level, resulting in inaccurate ADC results if the V_{DDE} voltage level is less than V_{DDA}.

3 When $V_{RCSEL} = V_{DDA}$ (high), the internally generated V_{DD33} voltage may be used to power V_{DDEMLB} as long as the PK[0:2] pads remain in the disabled default state with their output buffers, input buffers, and pull devices disabled.

4 The pad type is indicated by one or more of the following abbreviations: A–analog, F—fast speed, H–high voltage, I—input-only, M–medium speed, S–slow speed. For example, pad type SH designates a slow high-voltage pad.

5 The IHA pads are related to V_{DDA}.

6 Characterization Based Capability:
IOH_F = {12, 20, 30, 40} mA and IOL_F = {24, 40, 50, 65} mA for {00, 01,10, 11} drive mode with V_{DDE} = 3.0 V;
IOH_F = {7, 13, 18, 25} mA and IOL_F = {18, 30, 35, 50} mA for {00, 01, 10, 11} drive mode with V_{DDE} = 2.25 V;
IOH_F = {3, 7, 10, 15} mA and IOL_F = {12, 20, 27, 35} mA for {00, 01, 10, 11} drive mode with V_{DDE} = 1.62 V.

7 Characterization Based Capability:
IOH_S = {6, 11.6} mA and IOL_S = {9.2, 17.7} mA for {slow, medium} I/O with V_{DDEH} = 4.5 V;
IOH_S = {2.8, 5.4} mA and IOL_S = {4.2, 8.1} mA for {slow, medium} I/O with V_{DDEH} = 3.0 V

8 All V_{OL}/V_{OH} values 100% tested with ±2 mA load.

9 Absolute value of current, measured at V_{IL} and V_{IH}.

10 Weak pull up/down inactive. Measured at V_{DDE} = 5.25 V. Applies to pad types: SH and MH. Leakage specification guaranteed only when power supplies are within specified operating conditions.

11 Maximum leakage occurs at maximum operating temperature. Leakage current decreases by approximately one-half for each 8 to 12 ^{o}C, in the ambient temperature range of 50 to 125 ^{o}C. Applies to pad types: pad_a and pad_ae.

4.6 Operating current specifications

Table 10. Operating currents

Spec	Characteristic	Symbol	Typ[1] 25 °C Ambient	Max[1] –40–150 °C Junction	Unit
Equations	$I_{TOTAL} = I_{DDE} + I_{DDA} + I_{RH} + I_{DD33} + I_{DDSYN} + I_{RC} + I_{DD}$ $I_{DDE} = I_{DDE1} + I_{DDE2} + I_{DDE3} + I_{DDE4} + I_{DDEMLB}$	—	—	—	—
1	V_{DDE} Current $V_{DDE(1,2,3,4)}$ @ 3.0 V – 5.5 V V_{DDEMLB} @ 2.375 V – 3.6 V Static[2] Dynamic[3]	I_{DDE}	 0 Note 3	 30 25	 µA mA
2	V_{DDA} Current V_{DDA} @ 3.0 V – 5.5 V Run mode Sleep mode – Optional 32 kHz osc enabled	I_{DDA}	 1 20 +5	 30 50 +15	 mA µA µA
3	V_{RH} Current V_{RH} @ 3.0 V – 5.5 V Run mode Sleep mode	I_{RH}	 300 1	 700 30	 µA µA
4	V_{DD33} Current V_{DD33} @ 3.0 V – 3.6 V Run mode Sleep mode	I_{DD33}	 10 10	 20 20	 mA µA

Table 10. Operating currents (continued)

Spec	Characteristic	Symbol	Typ[1] 25 °C Ambient	Max[1] –40–150 °C Junction	Unit
5	V_{DDSYN} Current V_{DD33} @ 3.0 V – 3.6 V	I_{DDSYN}			
	Run mode		5	10	mA
	Sleep mode		1	20	µA
	– Optional[4] 4–40 MHz osc enabled w/ no clock		+150	+350	µA
	– Optional[4] 4–40 MHz osc enabled w/ clock		+300	+400	µA
6	V_{RC} Current (excluding I_{DD}, I_{DD33}, I_{DDSYN})[5] V_{RC} @ 3.135 V – 5.5 V	I_{RC}			
	Run mode		1	10	mA
	Sleep mode		0	10	µA
	– Optional[4] 16MIRC enabled		+40	+60	µA
7	V_{DD} Current V_{DD} @ 1.08 V – 1.32 V	I_{DD}			
	Run mode (Maximum @ 116 MHz)[6]		200	340	mA
	Sleep mode		100	900	µA
	– Optional[4] 128KIRC enabled		+5	+10	µA
	– Optional[4] 16MIRC enabled		+200	+220	µA
	– Optional[4] 32 kHz osc enabled		+5	+20	µA
	– Optional[4] 4–40 MHz osc enabled w/ no clock		+5	+20	µA
	– Optional[4] 4–40 MHz osc enabled w/ clock		+150	+200	µA
	– Optional[4] 32 KB RAM		+10	+150	µA
	– Optional[4] 64 KB RAM		+20	+300	µA
	– Optional[4] 128 KB RAM		+40	+600	µA

1 Typ – Nominal voltage levels and functional activity. Max – Maximum voltage levels and functional activity.

2 Static state of pins is when input pins are disabled or not being toggled and driven to a valid input level, output pins are not toggling or driving against any current loads, and internal pull devices are disabled or not pulling against any current loads.

3 Dynamic current from pins is application-specific and depends on active pull devices, switching outputs, output capacitive and current loads, and switching inputs. Refer to Table 11 for more information.

4 Optional currents are values that should be added to their respective current specifications to obtain the actual value for that specification when the optional function is active. The plus sign (+) in the Typ and Max columns indicates these optional currents. For example, V_{DDSYN} in Sleep mode draws 1 .µA (typ). With the optional 4–40 MHz osc enabled w/ no clock, add 150 .µA for a total of 151 .µA (typ).

5 V_{RC} Current excluding the current supply to V_{DD33}, V_{DDSYN} and V_{DD} from V_{RC}.

6 Maximum supply current transition: 50mA per 20µS observation window.

4.7 I/O pad current specifications

The power consumption of an I/O segment depends on the usage of the pins on a particular segment. The power consumption is the sum of all output pin currents for a particular segment. The output pin current can be calculated from Table 11 based on the voltage, frequency, and load on the pin. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in Table 11.

Table 11. I/O pad average I_{DDE} specifications[1]

Spec	Pad Type[2]	Symbol	Period (ns)	Load[3] (pF)	V_{DDE} (V)	Drive/Slew Rate Select	I_{DDE} Avg (mA)	I_{DDE} RMS (mA)
1	Slow	$I_{DRV\_SSR\_HV}$	37	50	5.5	11	14	
2			130	50	5.5	01	5.3	
3			650	50	5.5	00	1.1	
4			840	200	5.5	00	3	
6	Medium	$I_{DRV\_MSR\_HV}$	24	50	5.5	11	9	
7			62	50	5.5	01	2.5	
8			317	50	5.5	00	0.5	
9			425	200	5.5	00	1.5	
11	Fast	I_{DRV_FC}	10	50	3.6	11	50.4	101.6
12			10	30	3.6	10	14.2	57.3
13			10	20	3.6	01	16.4	43.6
14			10	10	3.6	00	9.8	15.9
15			10	50	2.75	11	22.9	45.3
16			10	30	2.75	10	6.7	25.3
17			10	20	2.75	01	4.5	17.3
18			10	10	2.75	00	3	9.6
19	Input	$I_{DRV\_I\_HV}$	7	0.5	5.5	N/A	N/A	N/A

1 These are typical values that are estimated from simulation and not tested. Currents apply to output pins only.

2 Slow = SH or SHA; Medium = MH or MHA; Fast = F; Input = IHA. See Table 3.

3 All loads are lumped.

4.7.1 I/O pad V_{DD33} current specifications

The power consumption of the V_{DD33} supply is dependent on the usage of the pins on all I/O segments. The power consumption is the sum of all input and output pin V_{DD33} currents for all I/O segments. The output pin V_{DD33} current can be calculated from Table 12 based on the voltage, frequency, and load on all Pad F pins. The input pin V_{DD33} current can be calculated from Table 12 based on the voltage, frequency, and load on all Pad MH pins. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in Table 12.

Table 12. I/O pad average I_{DD33} specifications[1]

Spec	Pad Type[2]	Symbol	Period (ns)	Load[3] (pF)	Drive Select	I_{DD33} Avg (µA)	I_{DD33} RMS (µA)
1	Slow	$I_{DRV\_SSR\_HV}$	100	50	11	0.8	235.7
2			200	50	01	0.04	87.4
3			800	50	00	0.06	47.4
4			800	200	00	0.009	47
5	Medium	$I_{DRV\_MSR\_HV}$	40	50	11		
6			100	50	01	0.11	76.5
7			500	50	00	0.02	56.2
8			500	200	00	0.01	56.2
9	Input	$I_{DRV\_I\_HV}$	7	0.5	N/A		

1 These are typical values that are estimated from simulation and not tested. Currents apply to output pins only.

2 Slow = SH or SHA; Medium = MH or MHA; Fast = F; Input = IHA. See Table 3.

3 All loads are lumped.

Table 13. I_{DD33} pad average DC current[1]

Spec	Pad Type[2]	Symbol	Period (ns)	Load[3] (pF)	V_{DD33} (V)	V_{DDE} (V)	Drive Select	I_{DD33} Avg (µA)	I_{DD33} RMS (µA)
1	Fast	I_{DRV_FC}	10	50	3.6	3.6	11	3.32	11.77
2			10	30	3.6	3.6	10	2.28	7.07
3			10	20	3.6	3.6	01	1.73	5.75
4			10	10	3.6	3.6	00	1.39	4.77
5			10	50	3.6	2.75	11	2.3	7.81
6			10	30	3.6	2.75	10	1.64	4.96
7			10	20	3.6	2.75	01	1.37	4.31
8			10	10	3.6	2.75	00	1.06	4.09

1 These are typical values that are estimated from simulation and not tested. Currents apply to output pins only.

2 Slow = SH or SHA; Medium = MH or MHA; Fast = F; Input = IHA. See Table 3.

3 All loads are lumped.

4.8 Low voltage characteristics

Table 14. Low voltage monitors

Spec	Characteristic	Symbol	Min	Typical	Max	Unit
1	Power-on-Reset Assert Level[1]	V_{POR}	1.5	—	2.8	V
2	Low Voltage Monitor 3.3 V[2] Assert Level De-assert Level	 V_{LVI33A} V_{LVI33D}	 3.00 3.04	 3.05 3.12	 3.10 3.19	V
3	Low Voltage Monitor Synthesizer[3] Assert Level De-assert Level	 $V_{LVISYNA}$ $V_{LVISYND}$	 3.00 3.04	 3.05 3.12	 3.10 3.19	V
4	Low Voltage Monitor 3.0 V Low Threshold[1] VRCSEL = V_{SSA} Assert Level De-assert Level VRCSEL = V_{DDA} Assert Level De-assert Level	 $V_{LVI\_VDDA\_LOA}$ $V_{LVI\_VDDA\_LOD}$ $V_{LVI\_VDDA\_LOA}$ $V_{LVI\_VDDA\_LOD}$	 3.00 3.04 3.25 3.35	 3.05 3.12 3.35 3.45	 3.10 3.19 3.48 3.55	V
5	Low Voltage Monitor 5.0 V[1, 4] Assert Level De-assert Level	 $V_{LVI\_VDDA\_A}$ $V_{LVI\_VDDA\_D}$	 4.35 4.45	 4.475 4.575	 4.55 4.65	V
6	Low Voltage Monitor 5.0 V High Threshold[1, 5] Assert Level De-assert Level	 $V_{LVI\_VDDA\_HA}$ $V_{LVI\_VDDA\_HD}$	 4.50 4.50	 4.675 4.675	 4.80 4.80	V

1 Monitors V_{DDA}.

2 Monitors V_{DD33}.

3 Monitors V_{DDSYN}.

4 Disabled when $V_{RCSEL} = V_{SSA}$.

4.9 Oscillators electrical characteristics

Table 15. 3.3 V high frequency external oscillator

Spec	Characteristic	Symbol	Min	Max	Unit
1	Frequency Range	f_{ref}	4[1]	40	MHz
2	Duty Cycle of reference	t_{DC}	40	60	%
3	EXTAL Input High Voltage External crystal mode[2] External clock mode	V_{IHEXT}	 V_{XTAL} + 0.4 0.65 × V_{DDSYN}	 V_{DDSYN} + 0.3 V_{DDSYN} + 0.3	V
4	EXTAL Input Low Voltage External crystal mode[3] External clock mode	V_{ILEXT}	 V_{DDSYN} – 0.3 V_{DDSYN} – 0.3	 V_{XTAL} – 0.4 0.35 × V_{DDSYN}	V
5	XTAL Current[4]	I_{XTAL}	1	3	mA
6	Total On-chip stray capacitance on XTAL	C_{S_XTAL}	—	3	pF
7	Total On-chip stray capacitance on EXTAL	C_{S_EXTAL}	—	3	pF

Table 15. 3.3 V high frequency external oscillator (continued)

Spec	Characteristic	Symbol	Min	Max	Unit
8	Crystal manufacturer's recommended capacitive load	C_L	See crystal specification	See crystal specification	pF
9	Discrete load capacitance to be connected to EXTAL	C_{L_EXTAL}	—	$2\times C_L - C_{S\_EXTAL} - C_{PCB\_EXTAL}$[5]	pF
10	Discrete load capacitance to be connected to XTAL	C_{L_XTAL}	—	$2\times C_L - C_{S\_XTAL} - C_{PCB\_XTAL}$[5]	pF
11	Startup Time	$t_{startup}$	—	10	ms

1 When PLL frequency modulation is active, reference frequencies less than 8 MHz will distort the modulated waveform and the effects of this on emissions is not characterized.

2 This parameter is meant for those who do not use quartz crystals or resonators, but instead use CAN oscillators in crystal mode. In that case, $V_{extal} - V_{xtal} \geq 400$ mV criteria has to be met for oscillator's comparator to produce output clock.

3 This parameter is meant for those who do not use quartz crystals or resonators, but instead use CAN oscillators in crystal mode. In that case, $V_{xtal} - V_{extal} \geq 400$ mV criteria has to be met for oscillator's comparator to produce output clock.

4 I_{xtal} is the oscillator bias current out of the XTAL pin with both EXTAL and XTAL pins grounded.

5 C_{PCB_EXTAL} and C_{PCB_XTAL} are the measured PCB stray capacitances on EXTAL and XTAL, respectively.

Table 16. 5 V low frequency (32 kHz) external oscillator

Spec	Characteristic	Symbol	Min	Max	Unit
1	Frequency Range	f_{ref32}	32	40	kHz
2	Duty Cycle of reference	t_{dc32}	40	60	%
3	XTAL32 Current[1]	I_{XTAL32}	—	3	μA
4	Crystal manufacturer's recommended capacitive load	C_{L32}	See crystal specification	See crystal specification	pF
5	Startup Time	$t_{Startup}$	—	2	s

1 I_{xtal32} is the oscillator bias current out of the XTAL32 pin with both EXTAL32 and XTAL32 pins grounded.

Table 17. 5 V High Frequency (16 MHz) internal RC oscillator

Spec	Characteristic	Symbol	Range	Min	Typ	Max	Unit
1	Frequency before trim[1]	f_{ut}	35%	10.4	16	21.6	MHz
2	Frequency after loading factory trim[2]	f_t	7%	14.9	16	17.1	MHz
3	Application trim resolution[3]	t_s	—	—	—	±0.5	%
4	Application frequency trim step[3]	f_s	—	—	300	—	kHz
5	Startup Time	$t_{Startup}$	—	—	—	500	ns

1 Across process, voltage, and temperature.

2 Across voltage and temperature.

3 Fixed voltage and temperature.

Table 18. 5V low frequency (128 kHz) internal RC oscillator

Spec	Characteristic	Symbol	Range	Min	Typ	Max	Unit
1	Frequency before trim[1]	F_{ut128}	35%	83.2	128	172.8	kHz
2	Frequency after loading factory trim[2]	F_{t128}	7%	119.0	128	137.0	kHz
3	Application trim resolution[3]	T_{s128}	—	—	—	±2	%
4	Application frequency trim step[3]	F_{s128}	—	—	4	—	kHz
5	Startup Time	S_{t128}	—	—	—	100	µs

1 Across process, voltage, and temperature.

2 Across voltage and temperature.

3 Fixed voltage and temperature.

4.10 FMPLL electrical characteristics

Table 19. FMPLL electrical specifications[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	System Frequency[2]	f_{SYS}	—	116	MHz
2	PLL Reference Frequency Range	f_{REF}	4	40	MHz
3	PLL Frequency	f_{PLL}	$\frac{f_{vco(min)}}{(ERFD+1)}$		MHz
4	Loss of Reference Frequency [3]	f_{LOR}	100	2000	kHz
5	Self Clocked Mode Frequency	f_{SCM}	16	64	MHz
6	PLL Lock Time[4]	t_{LPLL}	—	400	µs
7	Duty Cycle of Reference	t_{DC}	40	60	%
8	Frequency un-LOCK Range	f_{UL}	–4.0	4.0	% f_{SYS}
9	Frequency LOCK Range	f_{LCK}	–2.0	2.0	% f_{SYS}
10	CLKOUT Period Jitter,[5] Measured at f_{SYS} Max Cycle-to-cycle Jitter	C_{Jitter}	–5	5	%f_{SYS}
11	CLKOUT Jitter at ≥ 50 µs period	C_{Jitter}	–250	250	ns
12	Peak-to-Peak Frequency Modulation Range Limit [6,7] (f_{SYS}Max must not be exceeded)	C_{mod}	0	4	%f_{SYS}
13	FM Depth Tolerance[8]	C_{mod_err}	–0.50	0.50	%f_{SYS}
14	VCO Frequency[9]	f_{VCO}	192	600	MHz
15	Modulation Rate Limits[10]	f_{MOD}	0.400	1	MHz

1 V_{DDSYN} = 3.0 V to 3.6 V, V_{SS} = V_{SSSYN} = 0 V, T_A = T_L to T_H.

[2] The maximum frequency value is with frequency modulation disabled. If frequency modulation is enabled, the maximum frequency value should be de-rated by the percentage of modulation enabled so that the maximum frequency is not exceeded.

[3] "Loss of Reference Frequency" is the reference frequency detected internally, which transitions the PLL into self clocked mode.

[4] This specification applies to the period required for the PLL to re-lock after changing the MFD frequency control bits in the synthesizer control register (SYNCR). From power up with crystal oscillator reference, lock time will be additive with crystal startup time.

[5] Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of C_{jitter} + C_{mod}.

[6] Modulation depth selected must not result in f_{PLL} value greater than the f_{PLL} maximum specified value.

[7] Maximum and minimum variations from programmed modulation depth are 2%, 3%, and 4% peak-to-peak. Use only these settings.

[8] Depth tolerance is the programmed modulation depth ±0.25% of f_{SYS}.

[9] See the Block Guide for VCO frequency synthesis equations.

[10] Modulation rates less than 400 kHz will result in exceedingly long FM calibration durations. Modulation rates greater than 1 MHz will result in reduced calibration accuracy.

4.11 ADC electrical characteristics

Table 20. ADC conversion specifications (operating)

Spec	Characteristic	Symbol	Min	Max	Unit
1	Analog High Reference Voltage	V_{RH}	V_{DDA} – 0.5	V_{DDA}	V
2	Analog Low Reference Voltage	V_{RL}	0	0.5	V
3	Analog Input Voltage	AV_{IN}	V_{RL}	V_{RH}	V
4	Sampling Frequency	F_S	—	1.53	MHz
5	Maximum ADC Clock Frequency	F_{MAX}	—	60	MHz
6	Sampling Time V_{DDA} = 3.0 V – 3.6 V V_{DDA} > 3.6 V – 5.5 V	t_S	 250 125	—	ns
7	Differential Non Linearity	DNL	–1.0	1.0	LSB
8	Integral Non Linearity	INL	–1.5	1.5	LSB
9	Offset Error	OFS	–1.0	1.0	LSB
10	Gain Error	GNE	–2.0	2.0	LSB
11	Total Unadjusted Error [1]	TUE	–2.0	2.0	LSB

[1] TUE assumes no pin activity on pins adjacent to analog channel or output driver activity on corresponding V_{DDE} segment.

4.12 Flash memory electrical characteristics

Table 21. Flash program and erase specifications[1]

Spec	Characteristic	Symbol	Min	Initial Max[2]	Max[3]	Unit
1	Double Word (64 bits) Program Time[4]	$t_{dwprogram}$	—	—	500	µs
2	Page (128 bits and 256 bits) Program Time[4]	$t_{pprogram}$	—	160	500	µs
3	16 KB Block Pre-program and Erase Time	$t_{16kpperase}$	—	1000	5000	ms
4	64 KB Block Pre-program and Erase Time	$t_{64kpperase}$	—	1800	5000	ms
5	128 KB Block Pre-program and Erase Time	$t_{128kpperase}$	—	2600	7500	ms

Table 21. Flash program and erase specifications[1] (continued)

Spec	Characteristic	Symbol	Min	Initial Max[2]	Max[3]	Unit
6	256 KB Block Pre-program and Erase Time	$t_{256kpperase}$	—	5200	15,000	ms
7	Wait States Relative to System Frequency[5] PFCRP*n*[RWSC] = PFCRP*n*[APC] = 0b000; PFCRP*n*[WWSC] = 0b01 PFCRP*n*[RWSC] = PFCRP*n*[APC] = 0b001; PFCRP*n*[WWSC] = 0b01 PFCRP*n*[RWSC] = PFCRP*n*[APC] = 0b010; PFCRP*n*[WWSC] = 0b01 PFCRP*n*[RWSC] = PFCRP*n*[APC] = 0b011 – 0b111; PFCRP*n*[WWSC] = 0b01	t_{rwsc}	 — — — —	 — — — —	 30 60 90 f_{SYS} max	MHz
8	Recovery Time	$t_{Recover}$	—	—	45	µs

1 Typical program and erase times assume nominal supply values and operation at 25 °C.

2 Initial factory condition: < 100 program/erase cycles, nominal supply values and operation at 25 °C.

3 The maximum time is at worst case conditions after the specified number of program/erase cycles. This maximum value is characterized but not guaranteed.

4 Actual hardware programming time. This does not include software overhead.

5 Wait state timing is based on the system clock frequency and thus is same for all masters.

Table 22. Flash EEPROM Module Life (Full Temperature Range)

Spec	Characteristic	Symbol	Min	Typical[1]	Unit
1	Number of Program/Erase cycles per block for 16 KB and 64 KB blocks over the operating temperature range (T_J)	P/E	100,000	—	cycles
2	Number of Program/Erase cycles per block for 128 KB blocks over the operating temperature range (T_J)	P/E	1,000	100,000	cycles
3	Minimum Data Retention at 85 °C ambient temperature[2] Blocks with 0–1,000 P/E cycles Blocks with 1,001–10,000 P/E cycles Blocks with 10,001–100,000 P/E cycles	Retention	 20 10 1 – 5	—	years

1 Typical endurance is evaluated at 25 °C. Product qualification is performed to the minimum specification. For additional information on the Freescale definition of Typical Endurance, please refer to Engineering Bulletin EB619, *Typical Endurance for Nonvolatile Memory*.

2 Ambient temperature averaged over duration of application, not to exceed product operating temperature range.

4.13 Pad AC specifications

Table 23. Pad AC specifications (5.0 V, 2.5 V)[1]

Spec	Pad Type[2]	SRC/DSC[3]	Output Delay[4,4] (ns)	Rise/Fall[5,6] (ns)	Load Drive (pF)
1	Slow[7]	00	318/343	155/173	50
			408/431	188/204	200
		01	61/67	30/34	50
			80/90	38/44	200
		11	18/18	10/11	50
			27/28	15/17	200

Table 23. Pad AC specifications (5.0 V, 2.5 V)[1] (continued)

Spec	Pad Type[2]	SRC/DSC[3]	Output Delay[4,4] (ns)	Rise/Fall[5,6] (ns)	Load Drive (pF)
2	Medium	00	142/186	65/89	50
			195/253	91/122	200
		01	20/35	8.7/16.6	50
			41/64	24/35	200
		11	12/11	5.3/5.9	50
			32/34	21/23	200
3	Fast[8]	00	2.7	1.5	10
		01			20
		10			30
		11			50
4	Input	N/A	1.9/1.9	1.5/1.5	0.5

1 These are worst case values that are estimated from simulation and not tested. The values in the table are simulated at F_{SYS} = 116 MHz, V_{DD} = 1.08 – 1.32 V, V_{DDE} = 1.62 – 1.98 V, V_{DDEH} = 4.5 – 5.5 V, V_{RC33} and V_{DDPLL} = 3.0 – 3.6 V, $T_A = T_L$ to T_H.

2 Slow = SH or SHA; Medium = MH or MHA; Fast = F; Input = IHA. See Table 3.

3 SRC/DSC are bit fields in the Pad Configuration Registers. SRC—Slew Rate Control (slow and medium pad types only), DSC—Drive Strength Control (fast pad type only).

4 This parameter is supplied for reference and is not guaranteed by design and not tested.

5 This parameter is guaranteed by characterization before qualification rather than 100% tested.

6 Delay and rise/fall are measured to 20% or 80% of the respective signal.

7 Add a maximum of one system clock to the output delay for delay with respect to system clock.

8 Output delay is shown in. Add a maximum of one system clock to the output delay for delay with respect to system clock.

Table 24. De-rated pad AC specifications (3.3 V, 3.3 V)[1]

Spec	Pad Type[2]	SRC/DSC[3]	Out Delay[4,5] (ns)	Rise/Fall[6,] (ns)	Load Drive (pF)
1	Slow[7]	00	408/431	188/204	50
			533/592	250/288	200
		01	80/90	38/44	50
			146/167	82/96	200
		11	27/28	15/17	50
			81/92	57/67	200
2	Medium	00	184/240	79/107	50
			253/330	114/153	200
		01	28/47	11.8/21.8	50
			58/88	34/49	200
		11	18/17	7.6/8.9	50
			46/51	30/35	200

Table 24. De-rated pad AC specifications (3.3 V, 3.3 V)[1] (continued)

Spec	Pad Type[2]	SRC/DSC[3]	Out Delay[4,5] (ns)	Rise/Fall[6], (ns)	Load Drive (pF)
3	Fast[8]	00	2.5	1.2	10
		01		1.2	20
		10		1.2	30
		11		1.2	50
4	Input	N/A	3/3	1.5/1.5	0.5

1 These are worst case values that are estimated from simulation and not tested. The values in the table are simulated at F_{SYS} = 116 MHz, V_{DD} = 1.08 – 1.32 V, V_{DDE} = 3.0 – 3.6 V, V_{DDEH} = 3.0 – 3.6 V, V_{RC33} and V_{DDPLL} = 3.0 – 3.6 V, $T_A = T_L$ to T_H.

2 Slow = SH or SHA; Medium = MH or MHA; Fast = F; Input = IHA. See Table 3.

3 SRC/DSC are bit fields in the Pad Configuration Registers. SRC—Slew Rate Control (slow and medium pad types only), DSC—Drive Strength Control (fast pad type only).

4 This parameter is supplied for reference and is not guaranteed by design and not tested.

5 Delay and rise/fall are measured to 20% or 80% of the respective signal.

6 This parameter is guaranteed by characterization before qualification rather than 100% tested.

7 Add a maximum of one system clock to the output delay for delay with respect to system clock.

8 Output delay is shown in Figure 6. Add a maximum of one system clock to the output delay for delay with respect to system clock.

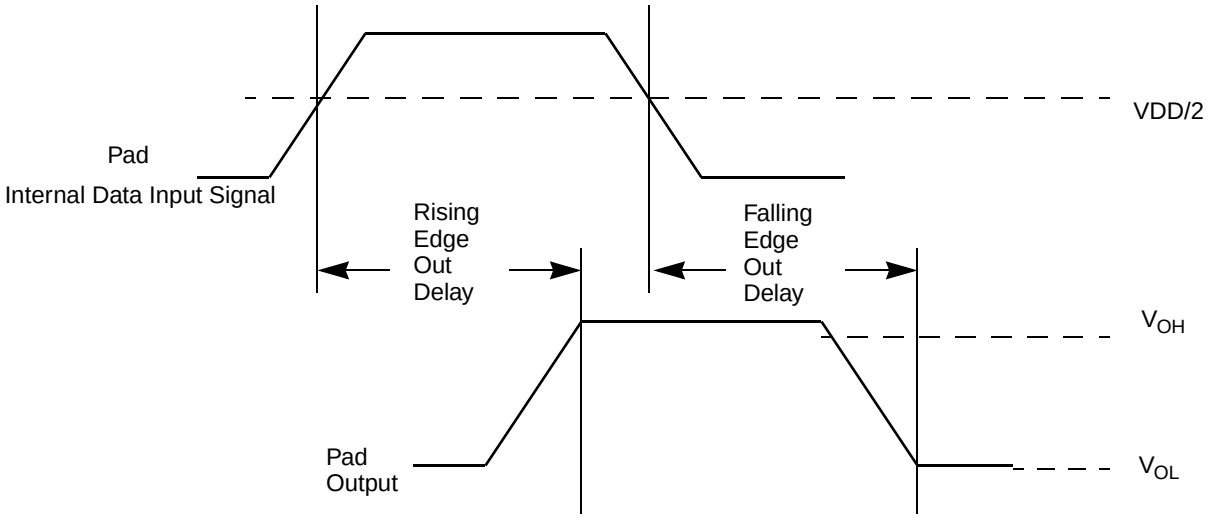


Figure 6. Pad output delay

4.14 AC timing

4.14.1 Reset and boot configuration pins

Table 25. Reset and boot configuration timing

Spec	Characteristic	Symbol	Min	Max	Unit
1	$\overline{\text{RESET}}$ Pulse Width	t_{RPW}	150	—	ns
2	BOOTCFG Setup Time after $\overline{\text{RESET}}$ Valid	t_{RCSU}	—	100	µs
3	BOOTCFG Hold Time from $\overline{\text{RESET}}$ Valid	t_{RCH}	0	—	µs

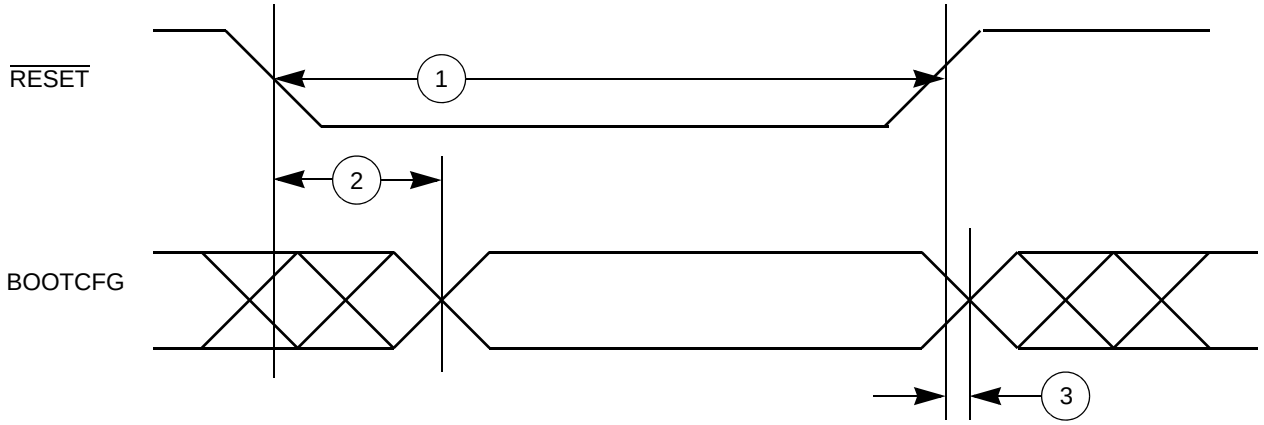


Figure 7. Reset and boot configuration timing

4.14.2 External interrupt (IRQ) and non-maskable interrupt (NMI) pins

Table 26. IRQ/NMI timing

Spec	Characteristic	Symbol	Min	Max	Unit
1	IRQ/NMI Pulse Width Low	t_{IPWL}	3	—	t_{SYS}
2	IRQ/NMI Pulse Width High	T_{IPWH}	3	—	t_{SYS}
3	IRQ/NMI Edge to Edge Time[1]	t_{ICYC}	6	—	t_{SYS}

[1] Applies when IRQ/NMI pins are configured for rising edge or falling edge events, but not both.

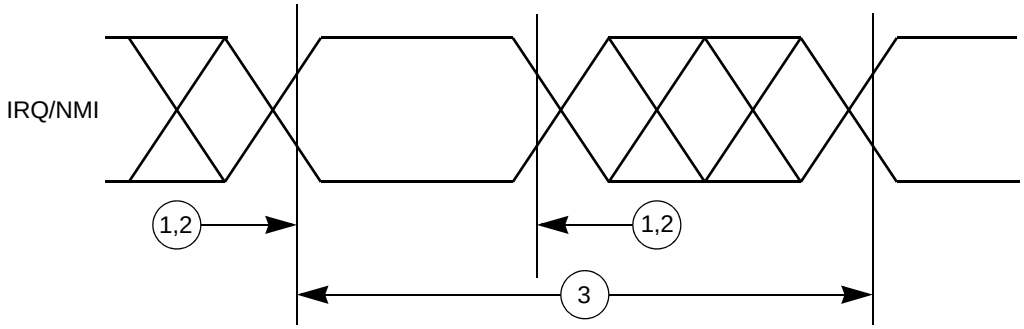


Figure 8. IRQ and NMI timing

4.14.3 JTAG (IEEE 1149.1) interface

Table 27. JTAG interface timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	TCK Cycle Time	t_{JCYC}	100	—	ns
2	TCK Clock Pulse Width (Measured at $V_{DDE}/2$)	t_{JDC}	40	60	ns
3	TCK Rise and Fall Times (40% – 70%)	$t_{TCKRISE}$	—	3	ns
4	TMS, TDI Data Setup Time	t_{TMSS}, t_{TDIS}	5	—	ns
5	TMS, TDI Data Hold Time	t_{TMSH}, t_{TDIH}	25	—	ns
6	TCK Low to TDO Data Valid	t_{TDOV}	—	25	ns
7	TCK Low to TDO Data Invalid	t_{TDOI}	0	—	ns
8	TCK Low to TDO High Impedance	t_{TDOHZ}	—	20	ns
9	JCOMP Assertion Time	t_{JCMPPW}	100	—	ns
10	JCOMP Setup Time to TCK Low	t_{JCMPS}	40	—	ns
11	TCK Falling Edge to Output Valid	t_{BSDV}	—	50	ns
12	TCK Falling Edge to Output Valid out of High Impedance	t_{BSDVZ}	—	50	ns
13	TCK Falling Edge to Output High Impedance	t_{BSDHZ}	—	50	ns
14	Boundary Scan Input Valid to TCK Rising Edge	t_{BSDST}	50	—	ns
15	TCK Rising Edge to Boundary Scan Input Invalid	t_{BSDHT}	50	—	ns

[1] These specifications apply to JTAG boundary scan only. JTAG timing specified at V_{DDE} = 3.0 – 5.5 V, $T_A = T_L$ to T_H, and C_L = 30 pF with SRC = 0b11.

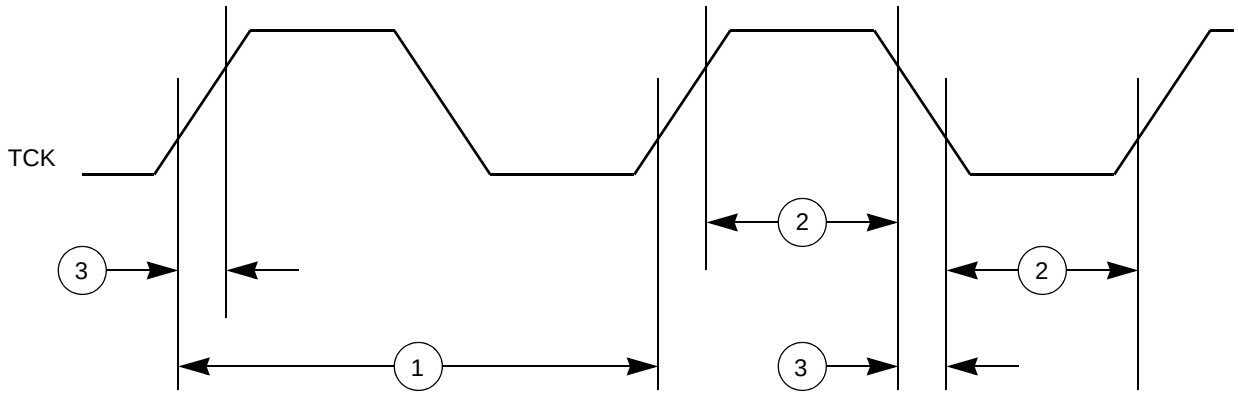


Figure 9. JTAG test clock input timing

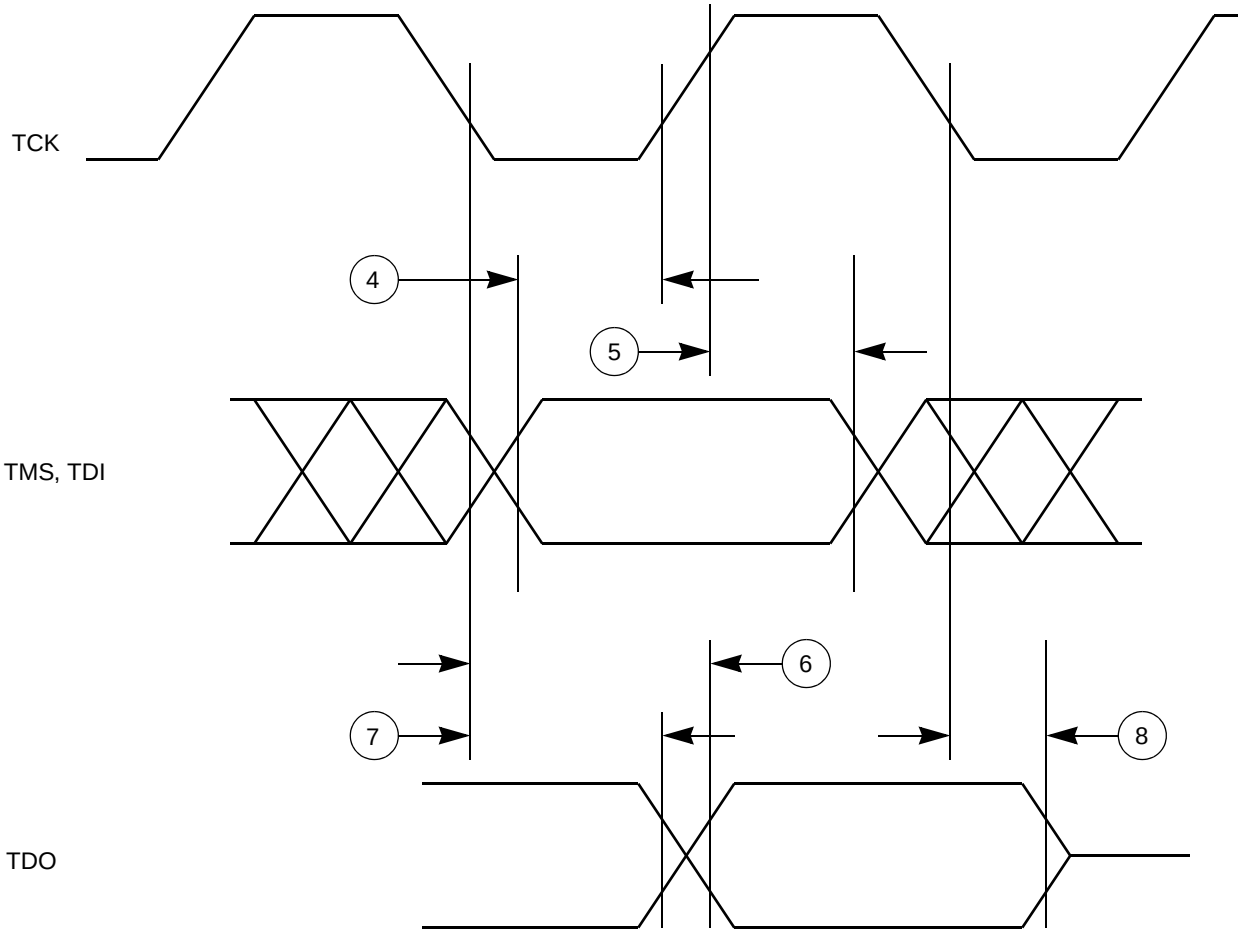


Figure 10. JTAG Test Access Port (TAP) timing

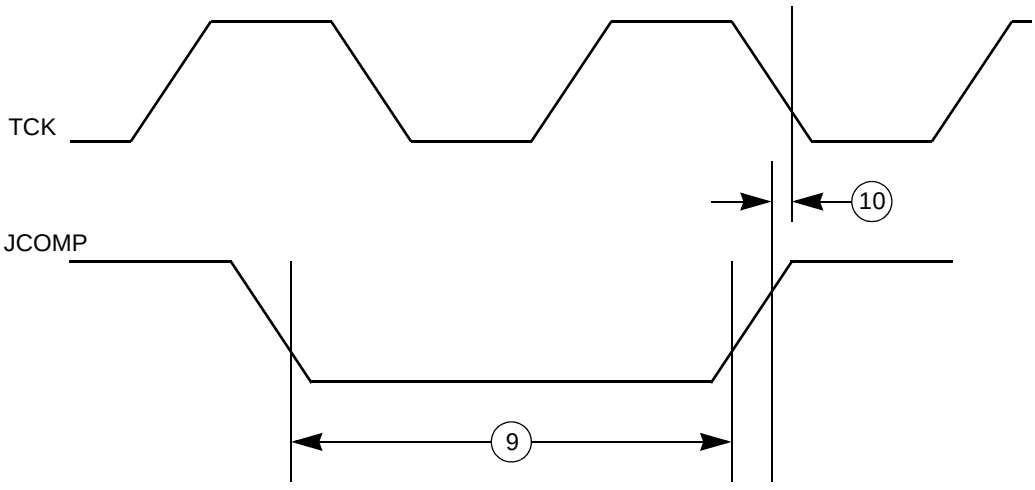


Figure 11. JTAG JCOMP timing

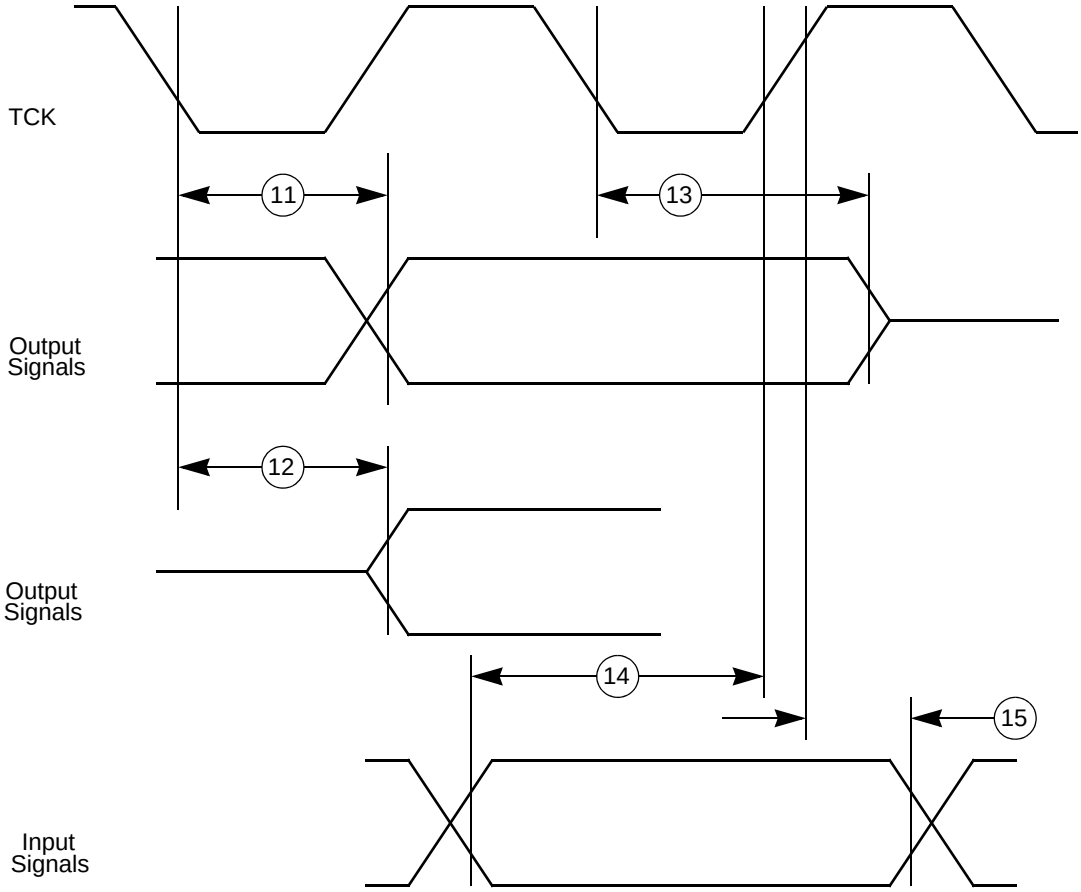


Figure 12. JTAG boundary scan timing

4.14.4 Enhanced Modular I/O Subsystem (eMIOS)

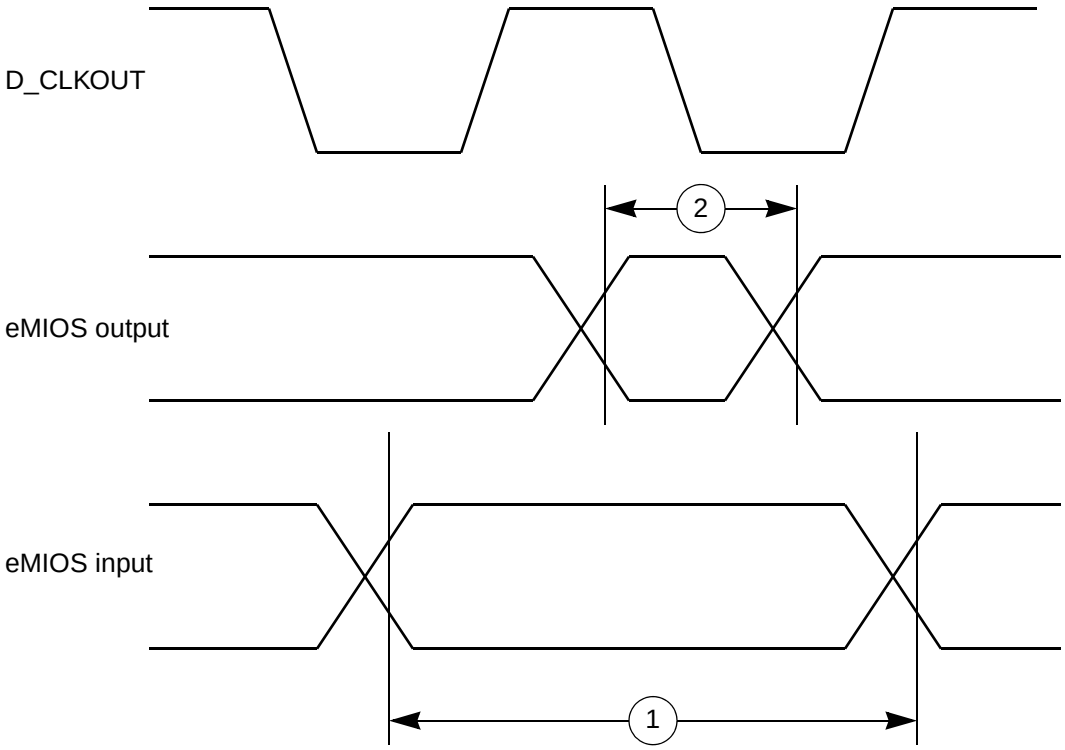
Table 28. eMIOS timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	eMIOS Input Pulse Width	t_{MIPW}	4	—	t_{CYC}
2	eMIOS Output Pulse Width	t_{MOPW}	1[2]	—	t_{CYC}

1 eMIOS timing specified at V_{DDE} = 3.0 – 5.5 V, $T_A = T_L$ to T_H, and CL = 30 pF with SRC = 0b11.

2 This specification does not include the rise and fall times. When calculating the minimum eMIOS pulse width, include the rise and fall times defined in the slew rate control fields (SRC) of the pad configuration registers (PCR).

Figure 13. eMIOS timing



4.14.5 Deserial Serial Peripheral Interface (DSPI)

Table 29. DSPI timing

Spec	Characteristic	Symbol	116 MHz[1]		Unit
			Min. Value	Max. Value	
1	DSPI Cycle Time Master (MTFE = 0) Slave (MTFE = 0) Master (MTFE = 1) Slave (MTFE = 1)	t_{SCK}	 100 100 50 50	 — — — —	 ns ns ns ns
2	PCS to SCK Delay[2]	t_{CSC}	7	—	ns
3	After SCK Delay[3]	t_{ASC}	14	—	ns
4	SCK Duty Cycle	t_{SDC}	$0.4 \times t_{SCK}$	$0.6 \times t_{SCK}$	ns
5	Slave Access Time ($\overline{SS}$ active to SOUT valid)	t_A	—	25	ns
6	Slave SOUT Disable Time ($\overline{SS}$ inactive to SOUT High-Z or invalid)	t_{DIS}	—	25	ns
7	PCSx to $\overline{PCSS}$ time	t_{PCSC}	0	—	ns
8	$\overline{PCSS}$ to PCSx time	t_{PASC}	0	—	ns
9	Data Setup Time for Inputs Master (MTFE = 0) Slave Master (MTFE = 1, CPHA = 0)[4] Master (MTFE = 1, CPHA = 1)	t_{SUI}	 25 5 10 25	 — — — —	 ns ns ns ns
10	Data Hold Time for Inputs Master (MTFE = 0) Slave Master (MTFE = 1, CPHA = 0)[4] Master (MTFE = 1, CPHA = 1)	t_{HI}	 –4 7 12 –4	 — — — —	 ns ns ns ns
11	Data Valid (after SCK edge) Master (MTFE = 0) Slave Master (MTFE = 1, CPHA = 0) Master (MTFE = 1, CPHA = 1)	t_{SUO}	 — — — —	 8 28 15 8	 ns ns ns ns
12	Data Hold Time for Outputs Master (MTFE = 0) Slave Master (MTFE = 1, CPHA = 0) Master (MTFE = 1, CPHA = 1)	t_{HO}	 –7 2 1 –7	 — — — —	 ns ns ns ns

1 116 MHz timing specified at CL = 50 pF with SRC = 0b11.

2 The maximum value is programmable in DSPI_CTAR*n*[PSSCK] and DSPI_CTAR*n*[CSSCK].

3 The maximum value is programmable in DSPI_CTAR*n*[PASC] and DSPI_CTAR*n*[ASC].

4 This number is calculated assuming the SMPL_PT bit field in DSPI_MCR is set to 0b10.

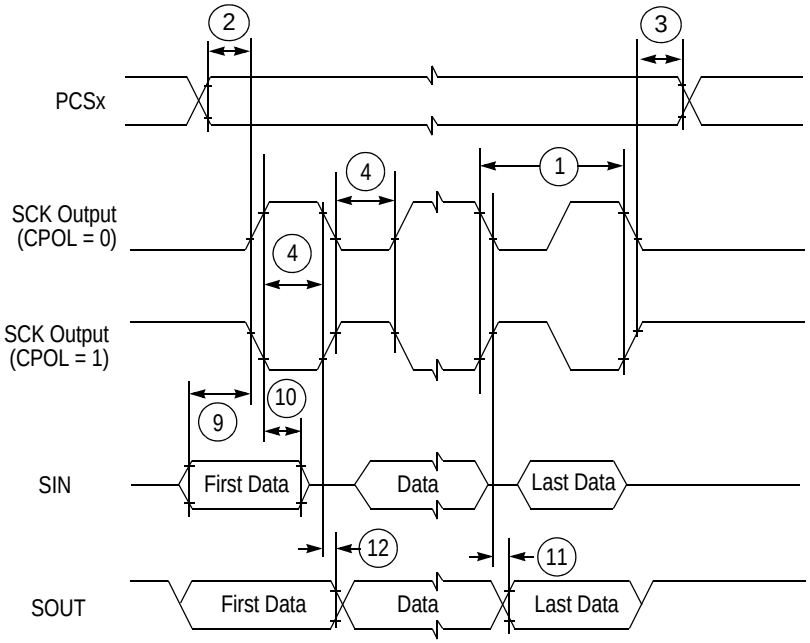


Figure 14. DSPI classic SPI timing — Master, CPHA = 0

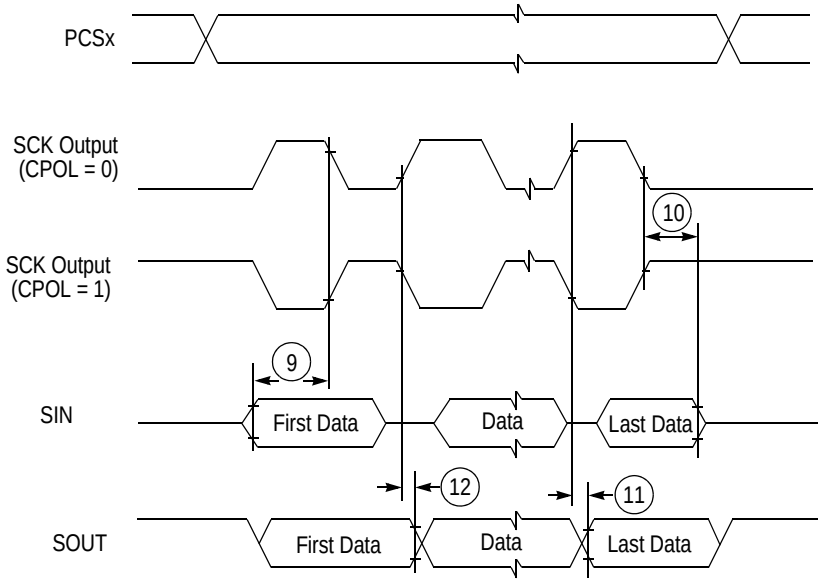


Figure 15. DSPI classic SPI timing — Master, CPHA = 1

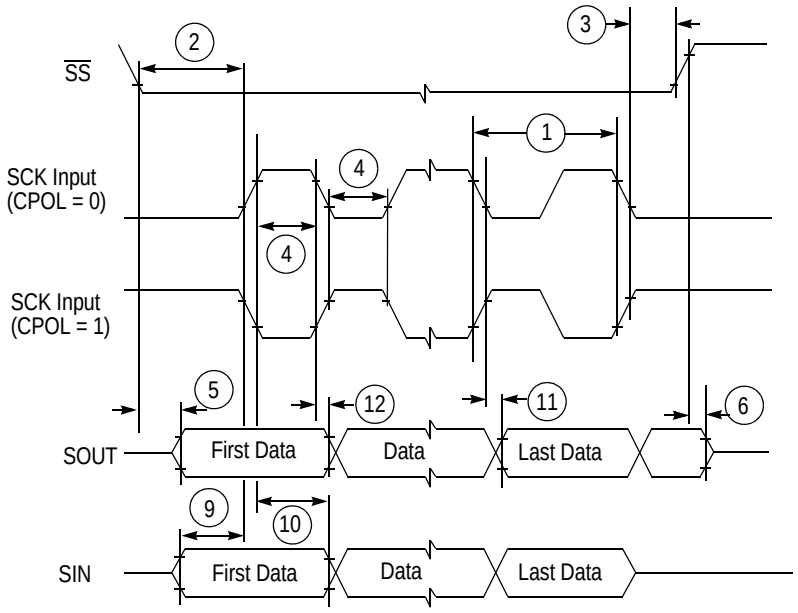


Figure 16. DSPI classic SPI timing — Slave, CPHA = 0

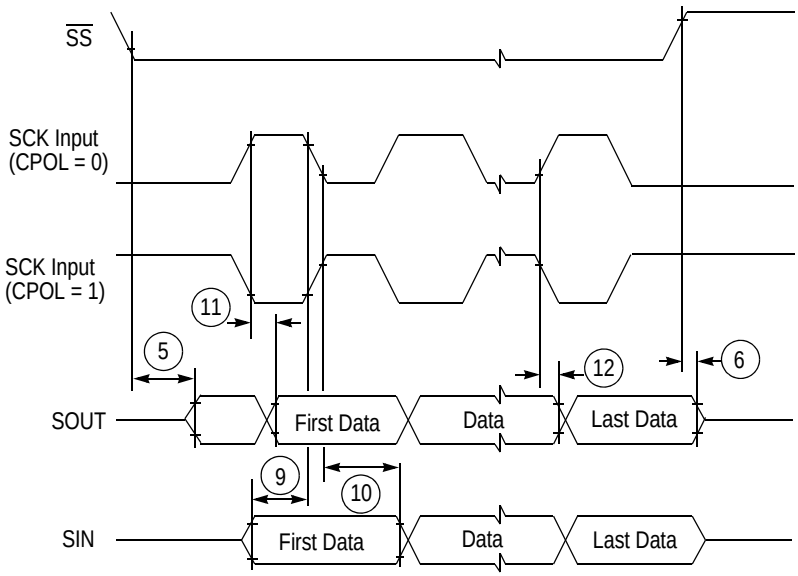


Figure 17. DSPI classic SPI timing — Slave, CPHA = 1

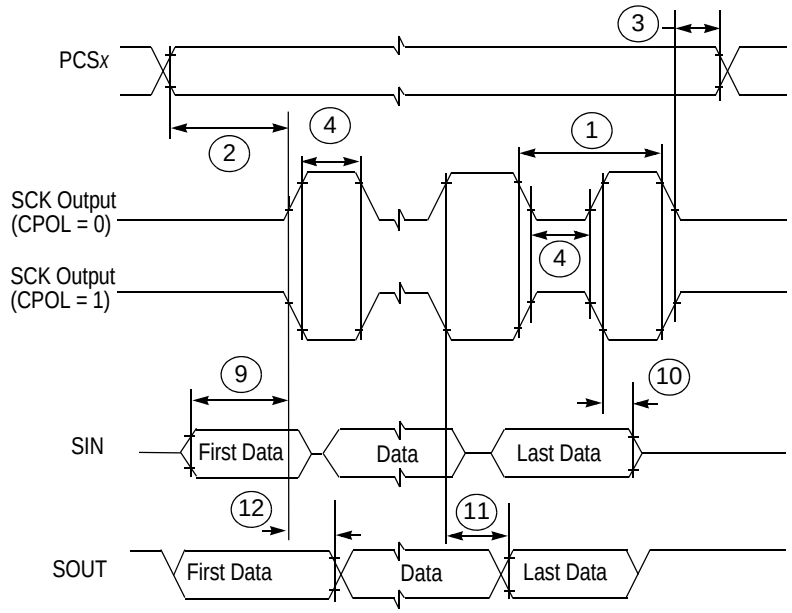


Figure 18. DSPI modified transfer format timing — Master, CPHA = 0

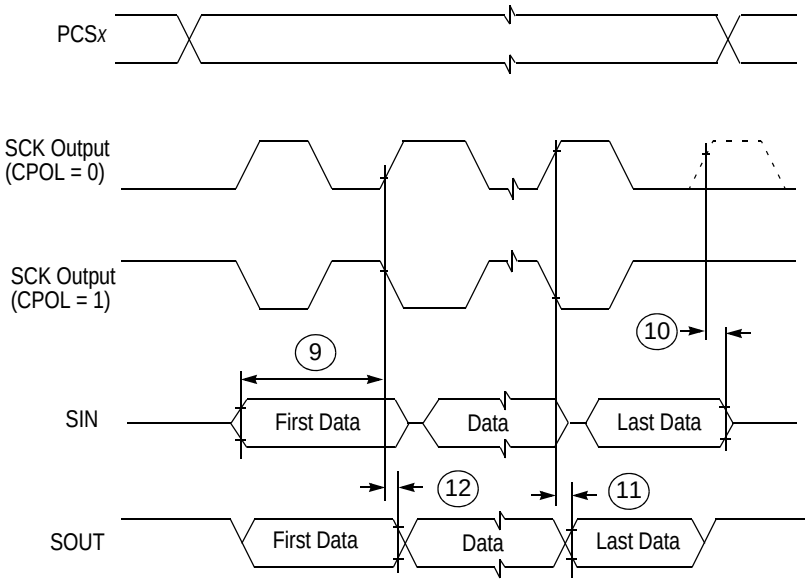


Figure 19. DSPI modified transfer format timing — Master, CPHA = 1

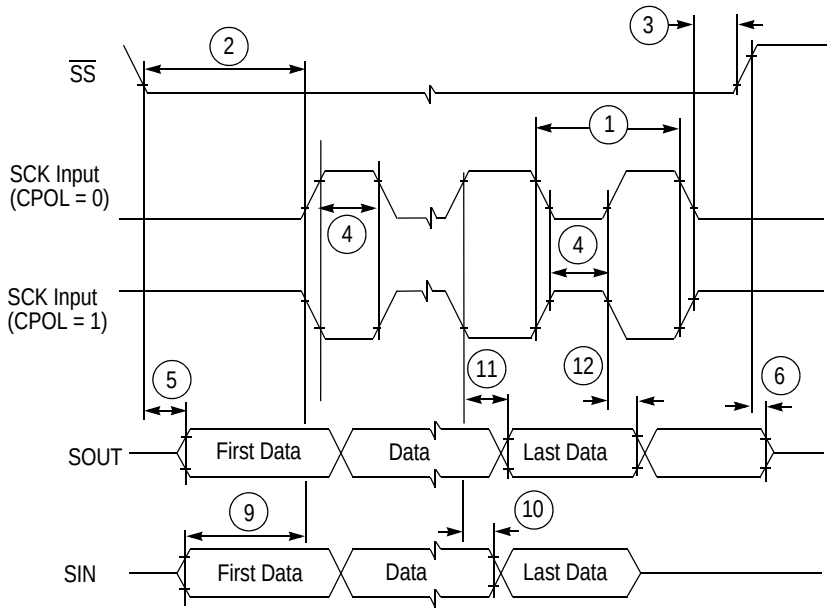


Figure 20. DSPI modified transfer format timing — Slave, CPHA = 0

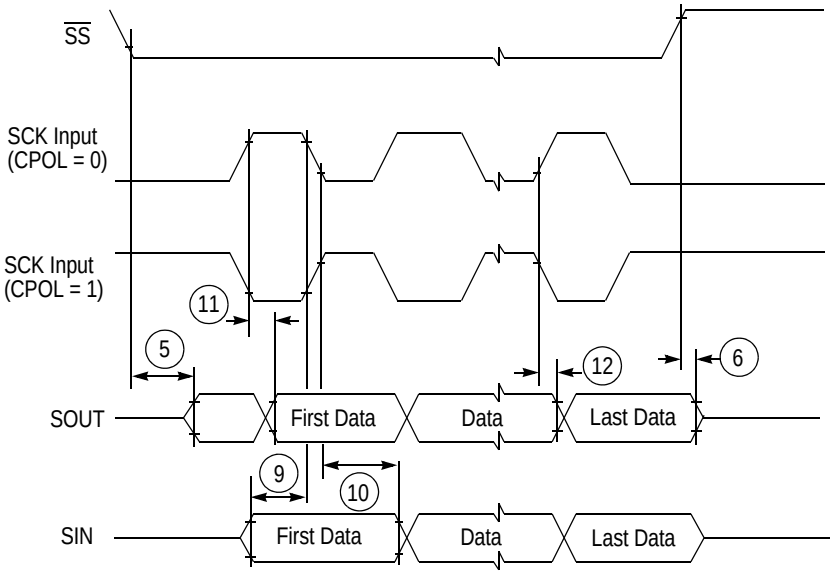


Figure 21. DSPI modified transfer format timing — Slave, CPHA = 1

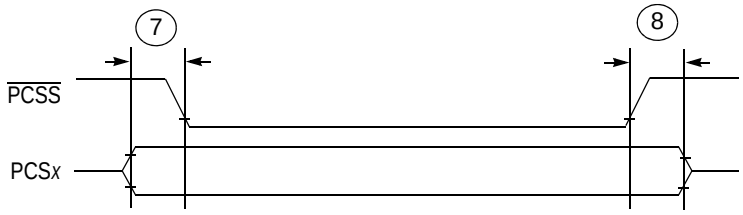


Figure 22. DSPI PCS strobe (PCSS) timing

4.14.6 MLB Interface

4.14.6.1 Media Local Bus DC Electrical Characteristics

Table 30 provides the DC electrical characteristics for the Media Local Bus interface.

Table 30. Media Local Bus DC Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Comments
Maximum Input Voltage	—	—	—	3.6	V	—
Low Level Input Threshold	V_{IL}	—	—	0.7	V	—
High Level Input Threshold	V_{IH}	1.8[1]	—	—	V	—
Low Level Output Threshold	V_{OL}	—	—	0.4	V	I_{OL} = 6 mA
High Level Output Threshold	V_{OH}	2.0	—	—	V	I_{OH} = –6 mA
Input Leakage Current	I_L	—	—	±1	µA	$0 < V_{in} < V_{DDE4}$

[1] Higher V_{IH} thresholds can be used; however, the risks associated with less noise margin in the system must be evaluated and assumed by the customer.

4.14.6.2 Media Local Bus (MLB) AC electrical characteristics

Table 31 and Table 32 provide the AC electrical characteristics for the Media Local Bus interface.

Table 31. MLB timing for MLB speed 256 Fs or 512 Fs

Spec	Parameter	Symbol	Min	Typ	Max	Unit	Comments
1	MLBCLK Operating Frequency[1]	f_{mck}	11.264 — — —	— 12.288 24.576 —	— — — 24.6272 25.600	MHz	256 Fs at 44.0 kHz 256 Fs at 48.0 kHz 512 Fs at 48.0 kHz 512 Fs at 48.1 kHz 512 Fs PLL unlocked
2	MLBCLK rise time	t_{mckr}	—	—	3	ns	V_{IL} to V_{IH}
3	MLBCLK fall time	t_{mckf}	—	—	3	ns	V_{IH} to V_{IL}
4	MLBCLK cycle time	t_{mckc}	—	81 40	—	ns	256 Fs 512 Fs
5	MLBCLK low time	t_{mckl}	31.5 30	37 35.5	—	ns	256 Fs 256 Fs PLL unlocked
			14.5 14	17 16.5	—	ns	512 Fs 512 Fs PLL unlocked
6	MLBCLK high time	t_{mckh}	31.5 30	38 36.5	—	ns	256 Fs 256 Fs PLL unlocked
			14.5 14	17 16.5	—	ns	512 Fs 512 Fs PLL unlocked
7	MLBCLK pulse width variation[2]	t_{mpwv}	—	—	2	ns p-p	—
8	MLBSIG/MLBDAT input valid to MLBCLK falling	t_{dsmcf}	1	—	—	ns	—
9	MLBSIG/MLBDAT input hold from MLBCLK low	t_{dhmcf}	0	—	—	ns	—

Table 31. MLB timing for MLB speed 256 Fs or 512 Fs (continued)

Spec	Parameter	Symbol	Min	Typ	Max	Unit	Comments
10	MLBSIG/MLBDAT output high impedance from MLBCLK low	t_{mcfdz}	0	—	t_{mckl}	ns	—
11	Bus Hold time[3]	t_{mdzh}	4	—	—	ns	—
12	MLBSIG/MLBDAT output valid from MLBCLK rising	t_{mcrdv}	—	—	8	ns	—
• Ground = 0.0V • Load Capacitance = 60 pF, SIU_PCR144–SIU_PCR146[DSC] = 0b11. • MLB speed of 256 Fs or 512 Fs (Fs = 48 kHz) Unless otherwise noted, all timing parameters are specified from the valid voltage threshold in Table 30.							

1 The Controller can shut off MLBCLK to place MLB in a low-power state.

2 Pulse width variation is measured at 1.25 V by triggering on one edge of MLBCLK and measuring the spread on the other edge, measured in ns peak-to-peak (ns p-p).

3 The board must be designed to insure that the high-impedance bus does not leave the logic state of the final driven bit for this time period. Therefore, coupling must be minimized while meeting the maximum capacitive load listed.

Table 32. MLB timing for MLB speed 1024 Fs

Spec	Parameter	Symbol	Min	Typ	Max	Unit	Comments
1	MLBCLK Operating Frequency[1]	f_{mck}	45.056 — — —	— 49.152 — —	— — 49.2544 51.200	MHz	1024 Fs at 44.0 kHz 1024 Fs at 48.0 kHz 1024 Fs at 48.1 kHz 1024 Fs PLL unlocked
2	MLBCLK rise time	t_{mckr}	—	—	1	ns	V_{IL} to V_{IH}
3	MLBCLK fall time	t_{mckf}	—	—	1	ns	V_{IH} to V_{IL}
4	MLBCLK cycle time	t_{mckc}	—	20.3	—	ns	V_{IL} to V_{IH}
5	MLBCLK low time	t_{mckl}	6.5 6.1	7.7 7.3	—	ns	1024 Fs PLL unlocked
6	MLBCLK high time	t_{mckh}	9.7 9.3	10.6 10.2	—	ns	1024 Fs PLL unclocked
7	MLBCLK pulse width variation[2]	t_{mpwv}	—	—	0.7	ns p-p	
8	MLBSIG/MLBDAT input valid to MLBCLK falling	t_{dsmcf}	1	—	—	ns	
9	MLBSIG/MLBDAT input hold from MLBCLK low	t_{dhmcf}	0	—	—	ns	
10	MLBSIG/MLBDAT output high impedance from MLBCLK low	t_{mcfdz}	0	—	t_{mckl}	ns	
11	Bus Hold time[3]	t_{mdzh}	2	—	—	ns	
12	MLBSIG/MLBDAT output valid from MLBCLK rising	t_{mcrdv}	—	—	7	ns	
• Ground = 0.0V • Load Capacitance = 40 pF, SIU_PCR144–SIU_PCR146[DSC] = 0b00. • MLB speed = 1024Fs (Fs = 48 kHz) • Unless otherwise noted, timing parameters are specified from the valid voltage threshold in Table 30.							

1 The Controller can shut off MLBCLK to place MLB in a low-power state.

2 Pulse width variation is measured at 1.25 V by triggering on one edge of MLBCLK and measuring the spread on the other edge, measured in ns peak-to-peak (ns p-p).

3 The board must be designed to insure that the high-impedance bus does not leave the logic state of the final driven bit for this time period. Therefore, coupling must be minimized while meeting the maximum capacitive load listed.

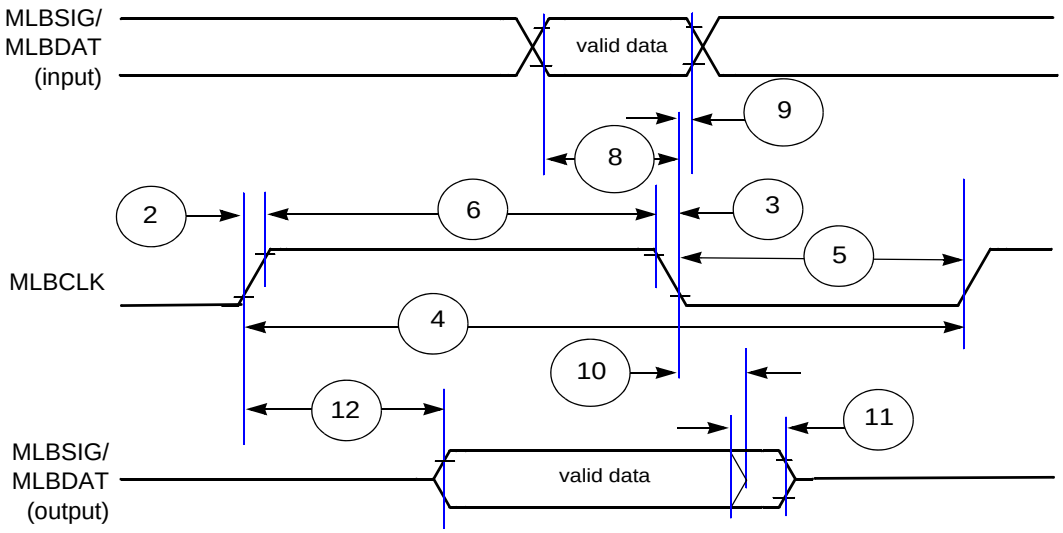


Figure 23. Media Local Bus (MLB) timing

4.14.7 Fast Ethernet Controller (FEC) interface

MII signals use CMOS signal levels compatible with devices operating at either 5.0 V or 3.3 V. Signals are not TTL compatible. They follow the CMOS electrical characteristics.

4.14.7.1 MII receive signal timing (RXD[3:0], RX_DV, RX_ER, and RX_CLK)

The receiver functions correctly up to a RX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the system clock frequency must exceed four times the RX_CLK frequency.

Table 33. MII receive signal timing

Spec	Characteristic	Min	Max	Unit
M1	RXD[3:0], RX_DV, RX_ER to RX_CLK setup	5	—	ns
M2	RX_CLK to RXD[3:0], RX_DV, RX_ER hold	5	—	ns
M3	RX_CLK pulse width high	35%	65%	RX_CLK period
M4	RX_CLK pulse width low	35%	65%	RX_CLK period

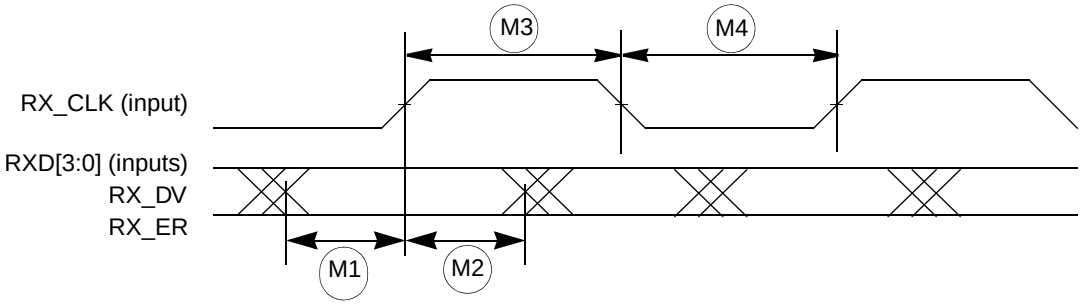


Figure 24. MII receive signal timing diagram

4.14.7.2 MII transmit signal timing (TXD[3:0], TX_EN, TX_ER, TX_CLK)

The transmitter functions correctly up to a TX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the system clock frequency must exceed four times the TX_CLK frequency.

The transmit outputs (TXD[3:0], TX_EN, TX_ER) can be programmed to transition from either the rising or falling edge of TX_CLK, and the timing is the same in either case. This options allows the use of non-compliant MII PHYs.

Refer to the Ethernet chapter for details of this option and how to enable it.

Table 34. MII transmit signal timing[1]

Spec	Characteristic	Min	Max	Unit
M5	TX_CLK to TXD[3:0], TX_EN, TX_ER invalid	5	—	ns
M6	TX_CLK to TXD[3:0], TX_EN, TX_ER valid	—	25	ns
M7	TX_CLK pulse width high	35%	65%	TX_CLK period
M8	TX_CLK pulse width low	35%	65%	TX_CLK period

1 Output pads configured with SRC = 0b11.

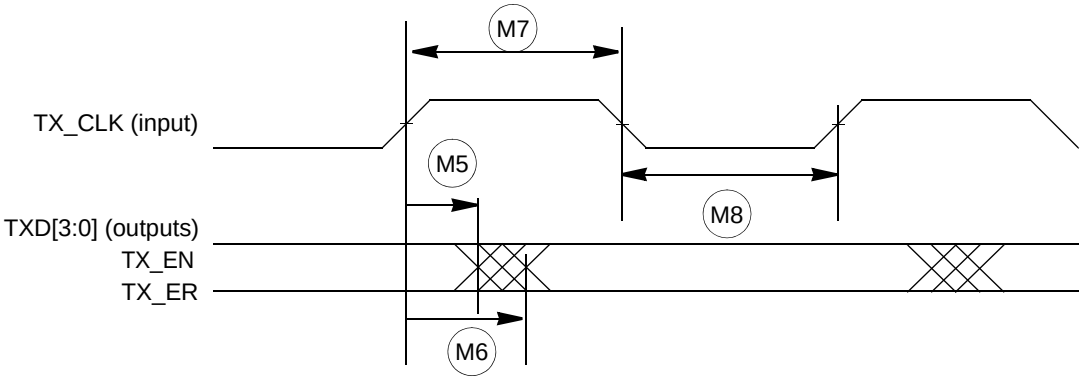


Figure 25. MII transmit signal timing diagram

4.14.7.3 MII async inputs signal timing (CRS and COL)

Table 35. MII Async Inputs Signal Timing[1]

Spec	Characteristic	Min	Max	Unit
M9	CRS, COL minimum pulse width	1.5	—	TX_CLK period

1 Output pads configured with SRC = 0b11.

Figure 26. MII async inputs timing diagram

4.14.7.4 MII serial management channel timing (MDIO and MDC)

The FEC functions correctly with a maximum MDC frequency of 2.5 MHz.

Table 36. MII serial management channel timing[1]

Spec	Characteristic	Min	Max	Unit
M10	MDC falling edge to MDIO output invalid (minimum propagation delay)	0	—	ns
M11	MDC falling edge to MDIO output valid (max prop delay)	—	25	ns
M12	MDIO (input) to MDC rising edge setup	10	—	ns
M13	MDIO (input) to MDC rising edge hold	0	—	ns
M14	MDC pulse width high	40%	60%	MDC period
M15	MDC pulse width low	40%	60%	MDC period

1 Output pads configured with SRC = 0b11.

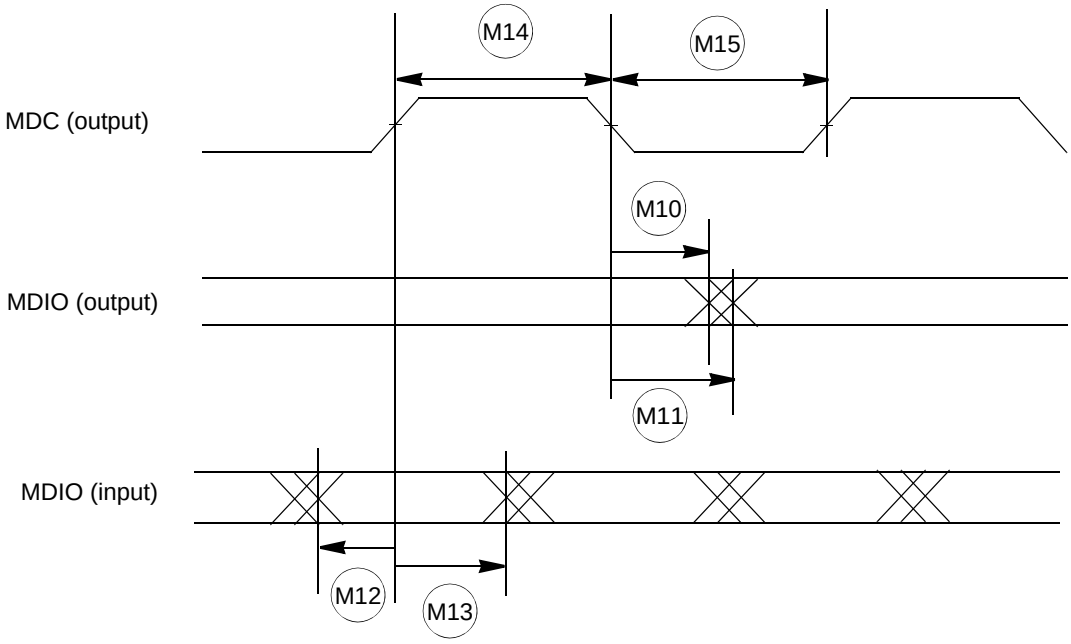


Figure 27. MII serial management channel timing diagram

5 Package characteristics

5.1 Package mechanical data

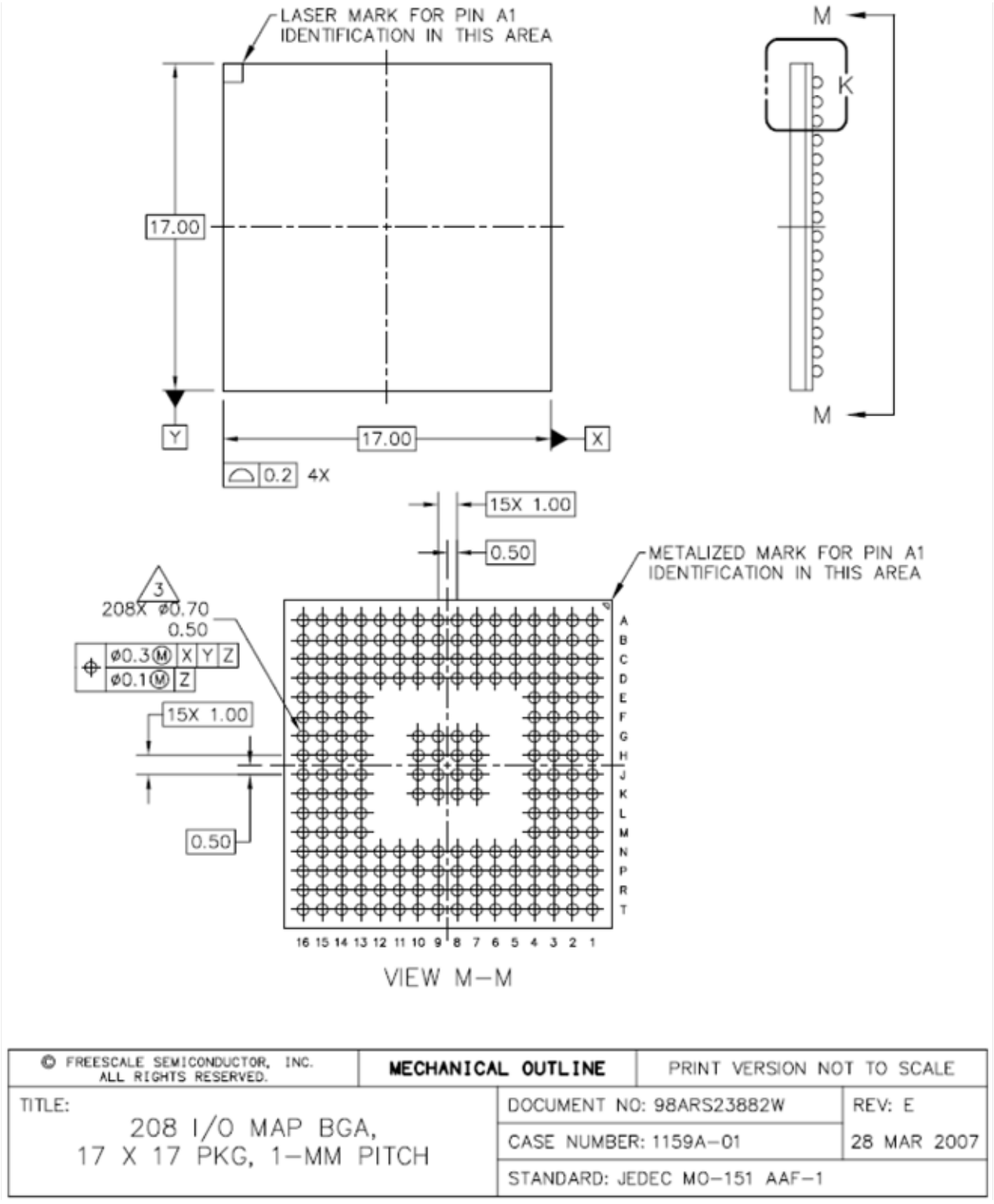
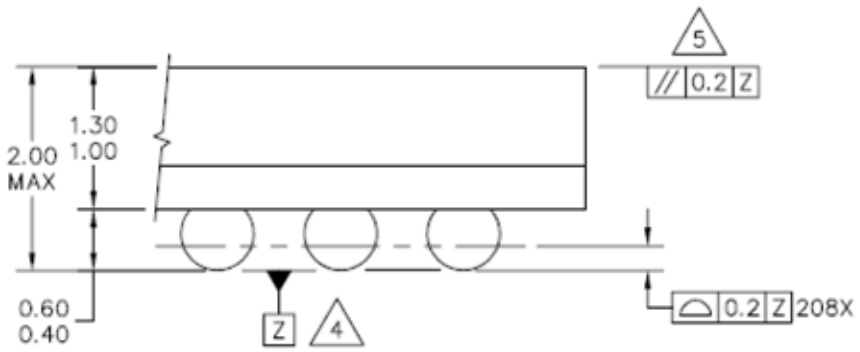


Figure 28. 208 MAPBGA package mechanical drawing



DETAIL K
(ROTATED 90° CLOCKWISE)

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.
6. PACKAGE CODE SUMMARY:
   MAP BGA: 5253
   MAP BGA PGE DIE: 5371

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 208 I/O MAP BGA, 17 X 17 PKG, 1–MM PITCH	DOCUMENT NO: 98ARS23882W	REV: E
	CASE NUMBER: 1159A–01	28 MAR 2007
	STANDARD: JEDEC MO–151 AAF–1	

Figure 29. 208 MAPBGA package detail

6 Revision history

Figure 37 describes the changes made to this document between revisions.

Table 37. Revision history

Revision	Date	Description of Changes
1	September 2011	Initial release: Technical Data

How to Reach Us:

Home Page:
www.freescale.com

Web Support:
http://www.freescale.com/support

USA/Europe or Locations Not Listed:
Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
1-800-521-6274 or +1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

Freescale Semiconductor Literature Distribution Center
1-800-441-2447 or +1-303-675-2140
Fax: +1-303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Document Number: PXN20
Rev. 1
2011

freescale™ semiconductor