# HEF4020B

## 14-stage binary counter

Rev. 8 — 18 November 2011 Product data sheet

## 1. General description

The HEF4020B is a 14-stage binary counter with a clock input ($\overline{CP}$), an overriding asynchronous master reset input (MR) and twelve fully buffered outputs (Q0, and Q3 to Q13). The counter advances on the HIGH to LOW transition of $\overline{CP}$. A HIGH on MR clears all counter stages and forces all outputs LOW, independent of the state of $\overline{CP}$. Each counter stage is a static toggle flip-flop. A feature of the device is its high speed (typ. 35 MHz at $V_{DD}$ = 15 V).

It operates over a recommended $V_{DD}$ power supply range of 3 V to 15 V referenced to $V_{SS}$ (usually ground). Unused inputs must be connected to $V_{DD}$, $V_{SS}$, or another input.

## 2. Features and benefits

- High speed operation
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Specified from −40 °C to +85 °C
- Complies with JEDEC standard JESD 13-B

## 3. Ordering information

**Table 1. Ordering information**

*All types operate from −40 °C to +85 °C.*

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| HEF4020BP | DIP16 | plastic dual in-line package; 16 leads (300 mil) | SOT38-4 |
| HEF4020BT | SO16 | plastic small outline package; 16 leads; body width 3.9 mm | SOT109-1 |

## 4. Functional diagram

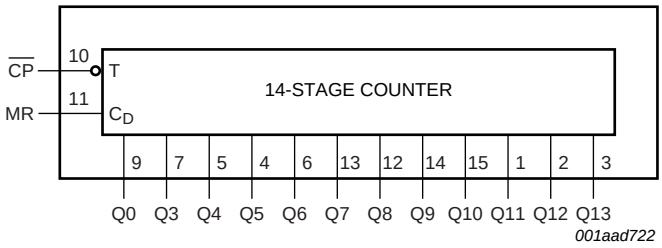


**Fig 1. Functional diagram**

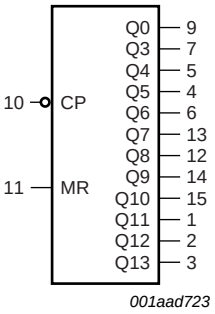


**Fig 2. Logic symbol**

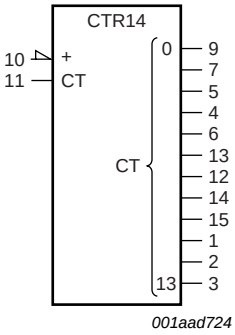


**Fig 3. IEC Logic symbol**

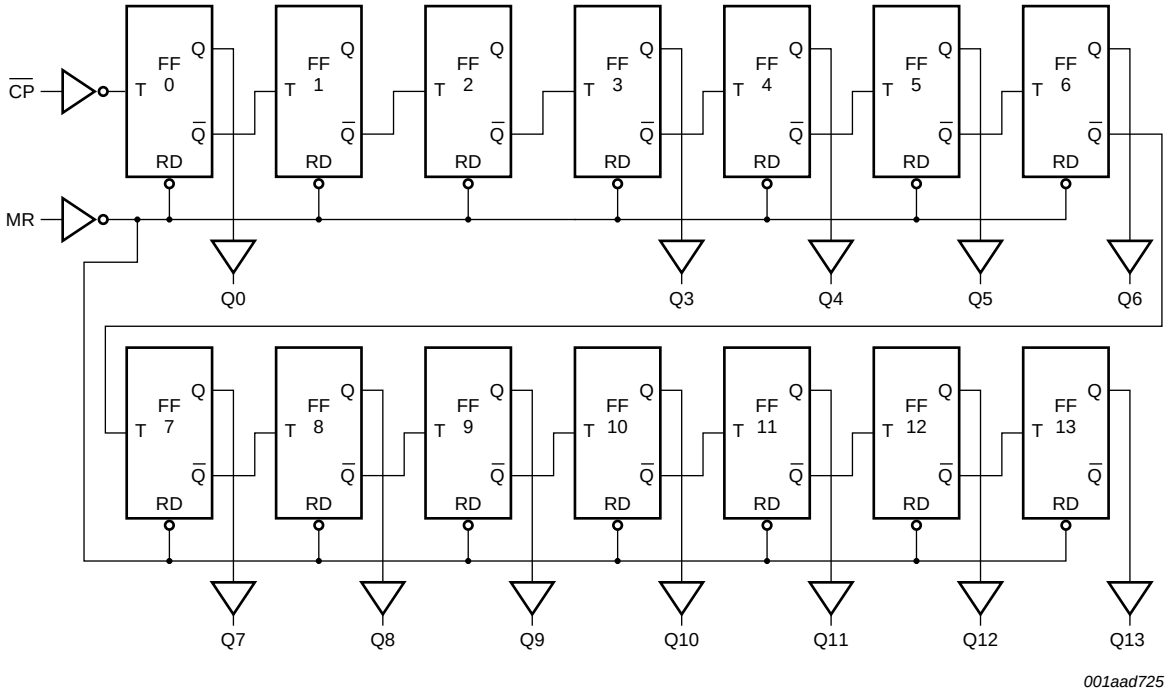


**Fig 4. Logic diagram**


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# 5. Pinning information

## 5.1 Pinning

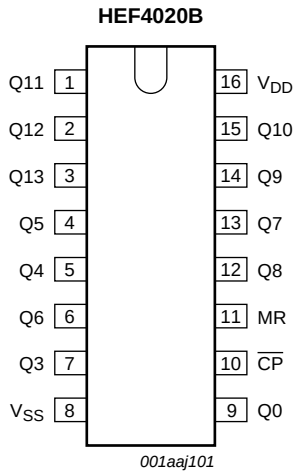


**Fig 5. Pin configuration**

## 5.2 Pin description

**Table 2. Pin description**

| Symbol | Pin | Description |
|---|---|---|
| Q3 to Q13 | 7, 5, 4, 6, 13, 12, 14, 15, 1, 2, 3 | parallel output (Q3 to Q13) |
| $V_{SS}$ | 8 | ground supply voltage |
| Q0 | 9 | parallel output |
| $\overline{CP}$ | 10 | clock input (HIGH-to-LOW edge triggered) |
| MR | 11 | master reset input (active HIGH) |
| $V_{DD}$ | 16 | supply voltage |

# 6. Functional description

**Table 3. Functional table[1]**

| Input | | Output |
|---|---|---|
| **CP** | **MR** | **Q0, Q3 to Q13** |
| ↑ | L | no change |
| ↓ | L | count |
| X | H | L |

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; ↑ = positive-going transition; ↓ = negative-going transition.


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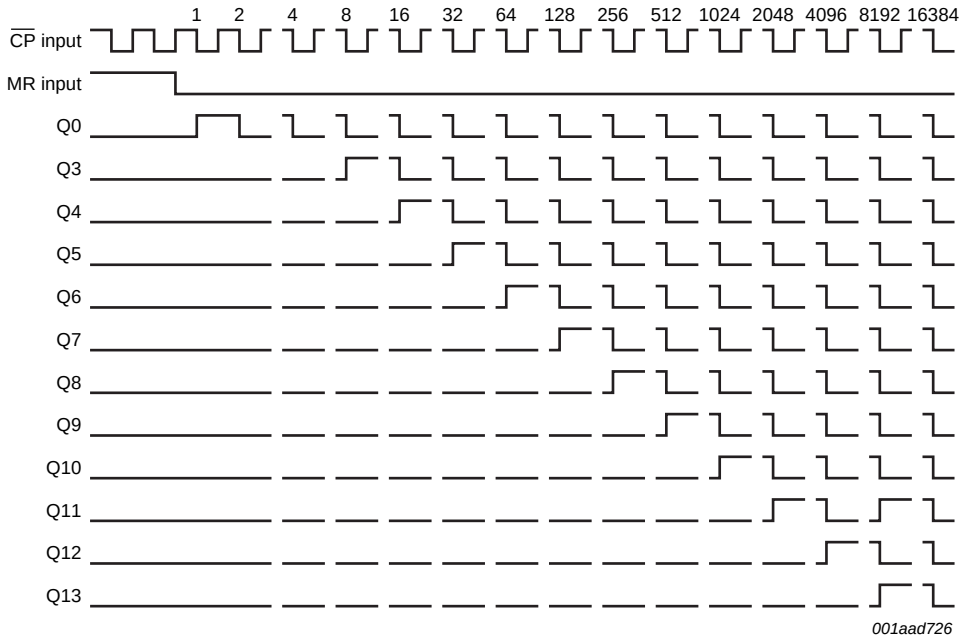


**Fig 6. Timing diagram**

## 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | supply voltage | | | –0.5 | +18 | V |
| $I_{IK}$ | input clamping current | $V_I < 0.–5$ V or $V_I > V_{DD} + 0.5$ V | | - | ±10 | mA |
| $V_I$ | input voltage | | | –0.5 | $V_{DD} + 0.5$ | V |
| $I_{OK}$ | output clamping current | $V_O < –0.5$ V or $V_O > V_{DD} + 0.5$ V | | - | ±10 | mA |
| $I_{I/O}$ | input/output current | | | - | ±10 | mA |
| $I_{DD}$ | supply current | | | - | 50 | mA |
| $T_{stg}$ | storage temperature | | | –65 | +150 | °C |
| $T_{amb}$ | ambient temperature | | | –40 | +85 | °C |
| $P_{tot}$ | total power dissipation | $T_{amb}$ –40 °C to +85 °C | | | | |
| | | DIP16 package | [1] | - | 750 | mW |
| | | SO16 package | [2] | - | 500 | mW |
| P | power dissipation | per output | | - | 100 | mW |

[1] For DIP16 package: $P_{tot}$ derates linearly with 12 mW/K above 70 °C.

[2] For SO16 package: $P_{tot}$ derates linearly with 8 mW/K above 70 °C.


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## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | supply voltage | | 3 | - | 15 | V |
| $V_I$ | input voltage | | 0 | - | $V_{DD}$ | V |
| $T_{amb}$ | ambient temperature | in free air | –40 | - | +85 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{DD}$ = 5 V | - | - | 3.75 | μs/V |
| | | $V_{DD}$ = 10 V | - | - | 0.5 | μs/V |
| | | $V_{DD}$ = 15 V | - | - | 0.08 | μs/V |

## 9. Static characteristics

**Table 6. Static characteristics**

*$V_{SS}$ = 0 V; $V_I$ = $V_{SS}$ or $V_{DD}$; unless otherwise specified.*

| Symbol | Parameter | Conditions | $V_{DD}$ | $T_{amb}$ = –40 °C | | $T_{amb}$ = 25 °C | | $T_{amb}$ = 85 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | Min | Max | |
| $V_{IH}$ | HIGH-level input voltage | $\|I_O\|$ < 1 μA | 5 V | 3.5 | - | 3.5 | - | 3.5 | - | V |
| | | | 10 V | 7.0 | - | 7.0 | - | 7.0 | - | V |
| | | | 15 V | 11.0 | - | 11.0 | - | 11.0 | - | V |
| $V_{IL}$ | LOW-level input voltage | $\|I_O\|$ < 1 μA | 5 V | - | 1.5 | - | 1.5 | - | 1.5 | V |
| | | | 10 V | - | 3.0 | - | 3.0 | - | 3.0 | V |
| | | | 15 V | - | 4.0 | - | 4.0 | - | 4.0 | V |
| $V_{OH}$ | HIGH-level output voltage | $\|I_O\|$ < 1 μA | 5 V | 4.95 | - | 4.95 | - | 4.95 | - | V |
| | | | 10 V | 9.95 | - | 9.95 | - | 9.95 | - | V |
| | | | 15 V | 14.95 | - | 14.95 | - | 14.95 | - | V |
| $V_{OL}$ | LOW-level output voltage | $\|I_O\|$ < 1 μA | 5 V | - | 0.05 | - | 0.05 | - | 0.05 | V |
| | | | 10 V | - | 0.05 | - | 0.05 | - | 0.05 | V |
| | | | 15 V | - | 0.05 | - | 0.05 | - | 0.05 | V |
| $I_{OH}$ | HIGH-level output current | $V_O$ = 2.5 V | 5 V | - | –1.7 | - | –1.4 | - | –1.1 | mA |
| | | $V_O$ = 4.6 V | 5 V | - | –0.52 | - | –0.44 | - | –0.36 | mA |
| | | $V_O$ = 9.5 V | 10 V | - | –1.3 | - | –1.1 | - | –0.9 | mA |
| | | $V_O$ = 13.5 V | 15 V | - | –3.6 | - | –3.0 | - | –2.4 | mA |
| $I_{OL}$ | LOW-level output current | $V_O$ = 0.4 V | 5 V | 0.52 | - | 0.44 | - | 0.36 | - | mA |
| | | $V_O$ = 0.5 V | 10 V | 1.3 | - | 1.1 | - | 0.9 | - | mA |
| | | $V_O$ = 1.5 V | 15 V | 3.6 | - | 3.0 | - | 2.4 | - | mA |
| $I_I$ | input leakage current | | 15 V | - | ±0.3 | - | ±0.3 | - | ±1.0 | μA |
| $I_{DD}$ | supply current | $I_O$ = 0 A | 5 V | - | 20 | - | 20 | - | 150 | μA |
| | | | 10 V | - | 40 | - | 40 | - | 300 | μA |
| | | | 15 V | - | 80 | - | 80 | - | 600 | μA |
| $C_I$ | input capacitance | | - | - | - | - | 7.5 | - | - | pF |


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## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

*$V_{SS}$ = 0 V; $T_{amb}$ = 25 °C; for test circuit see Figure 8.*

| Symbol | Parameter | Conditions | $V_{DD}$ | Extrapolation formula[1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| $t_{PHL}$ | HIGH to LOW propagation delay | CP to Q0; see Figure 7 | 5 V | 78 ns + (0.55 ns/pF)$C_L$ | - | 105 | 210 | ns |
| | | | 10 V | 34 ns + (0.23 ns/pF)$C_L$ | - | 45 | 90 | ns |
| | | | 15 V | 22 ns + (0.16 ns/pF)$C_L$ | - | 30 | 65 | ns |
| | | Qn to Qn + 1 | 5 V | 53 ns + (0.55 ns/pF)$C_L$ | - | 80 | 160 | ns |
| | | | 10 V | 19 ns + (0.23 ns/pF)$C_L$ | - | 30 | 60 | ns |
| | | | 15 V | 12 ns + (0.16 ns/pF)$C_L$ | - | 20 | 40 | ns |
| | | MR to Qn; see Figure 7 | 5 V | 153 ns + (0.55 ns/pF)$C_L$ | - | 180 | 360 | ns |
| | | | 10 V | 79 ns + (0.23 ns/pF)$C_L$ | - | 90 | 180 | ns |
| | | | 15 V | 62 ns + (0.16 ns/pF)$C_L$ | - | 70 | 140 | ns |
| $t_{PLH}$ | LOW to HIGH propagation delay | CP to Q0; see Figure 7 | 5 V | 78 ns + (0.55 ns/pF)$C_L$ | - | 105 | 210 | ns |
| | | | 10 V | 39 ns + (0.23 ns/pF)$C_L$ | - | 50 | 95 | ns |
| | | | 15 V | 27 ns + (0.16 ns/pF)$C_L$ | - | 35 | 70 | ns |
| | | Qn to Qn + 1 | 5 V | 43 ns + (0.55 ns/pF)$C_L$ | - | 70 | 140 | ns |
| | | | 10 V | 14 ns + (0.23 ns/pF)$C_L$ | - | 25 | 50 | ns |
| | | | 15 V | 12 ns + (0.16 ns/pF)$C_L$ | - | 20 | 40 | ns |
| $t_t$ | transition time | see Figure 7 | 5 V | 10 ns + (1.00 ns/pF)$C_L$ | - | 60 | 120 | ns |
| | | | 10 V | 9 ns + (0.42 ns/pF)$C_L$ | - | 30 | 60 | ns |
| | | | 15 V | 6 ns + (0.28 ns/pF)$C_L$ | - | 20 | 40 | ns |
| $t_W$ | pulse width | CP = HIGH; minimum width; see Figure 7 | 5 V | | 50 | 25 | - | ns |
| | | | 10 V | | 25 | 15 | - | ns |
| | | | 15 V | | 20 | 10 | - | ns |
| | | MR = HIGH; minimum width; see Figure 7 | 5 V | | 130 | 65 | - | ns |
| | | | 10 V | | 95 | 50 | - | ns |
| | | | 15 V | | 90 | 45 | - | ns |
| $t_{rec}$ | recovery time | MR input; see Figure 7 | 5 V | | 115 | 60 | - | ns |
| | | | 10 V | | 65 | 35 | - | ns |
| | | | 15 V | | 55 | 25 | - | ns |
| $f_{max}$ | maximum frequency | see Figure 7 | 5 V | | 5 | 10 | - | MHz |
| | | | 10 V | | 13 | 25 | - | MHz |
| | | | 15 V | | 18 | 35 | - | MHz |

[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown ($C_L$ in pF).


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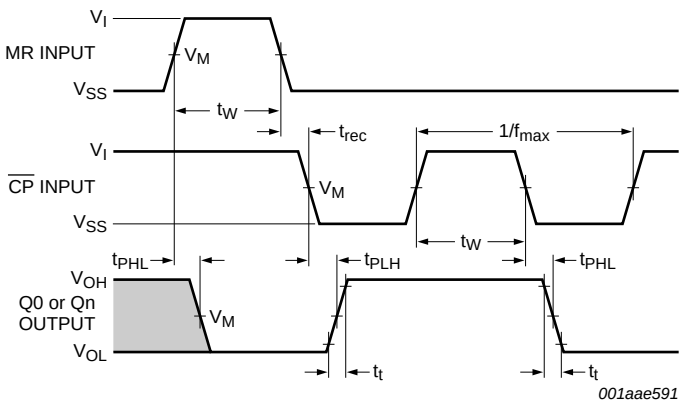
**Table 8. Dynamic power dissipation $P_D$**

*$P_D$ can be calculated from the formulas shown. $V_{SS}$ = 0 V; $t_r = t_f \leq 20$ ns; $T_{amb}$ = 25 °C.*

| Symbol | Parameter | $V_{DD}$ | Typical formula for $P_D$ (µW) | where: |
|---|---|---|---|---|
| $P_D$ | dynamic power dissipation | 5 V | $P_D = 600 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ | $f_i$ = input frequency in MHz, |
| | | 10 V | $P_D = 2800 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ | $f_o$ = output frequency in MHz, |
| | | 15 V | $P_D = 8200 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ | $C_L$ = output load capacitance in pF, |
| | | | | $V_{DD}$ = supply voltage in V, |
| | | | | $\Sigma(f_o \times C_L)$ = sum of the outputs. |

## 11. Waveforms




Measurement points are given in Table 9.

**Fig 7. Propagation delays, minimum pulse widths, transition and recovery times and maximum clock frequency**

**Table 9. Measurement points**

| Supply voltage | Input | Output |
|---|---|---|
| $V_{DD}$ | $V_M$ | $V_M$ |
| 5 V to 15 V | $0.5V_{DD}$ | $0.5V_{DD}$ |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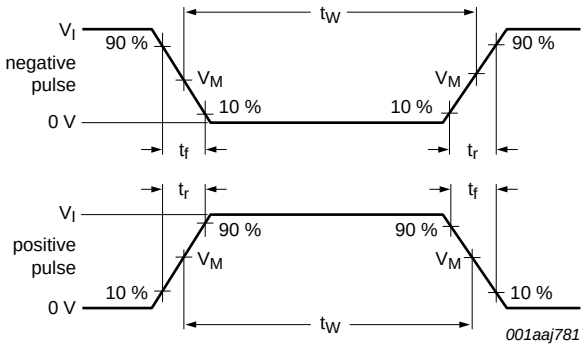
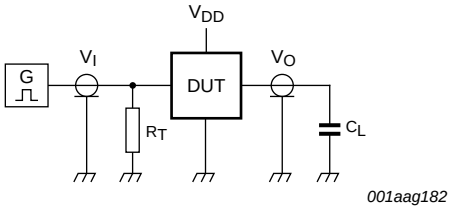



a. Input waveforms




b. Test circuit

Test data is given in Table 10.

Definitions for test circuit:

DUT = Device Under Test.

$C_L$ = load capacitance including jig and probe capacitance.

$R_T$ = termination resistance should be equal to the output impedance $Z_o$ of the pulse generator.

**Fig 8. Test circuit for measuring switching times**

**Table 10. Test data**

| Supply voltage | Input | | Load |
|---|---|---|---|
| $V_{DD}$ | $V_I$ | $t_r$, $t_f$ | $C_L$ |
| 5 V to 15 V | $V_{SS}$ or $V_{DD}$ | ≤ 20 ns | 50 pF |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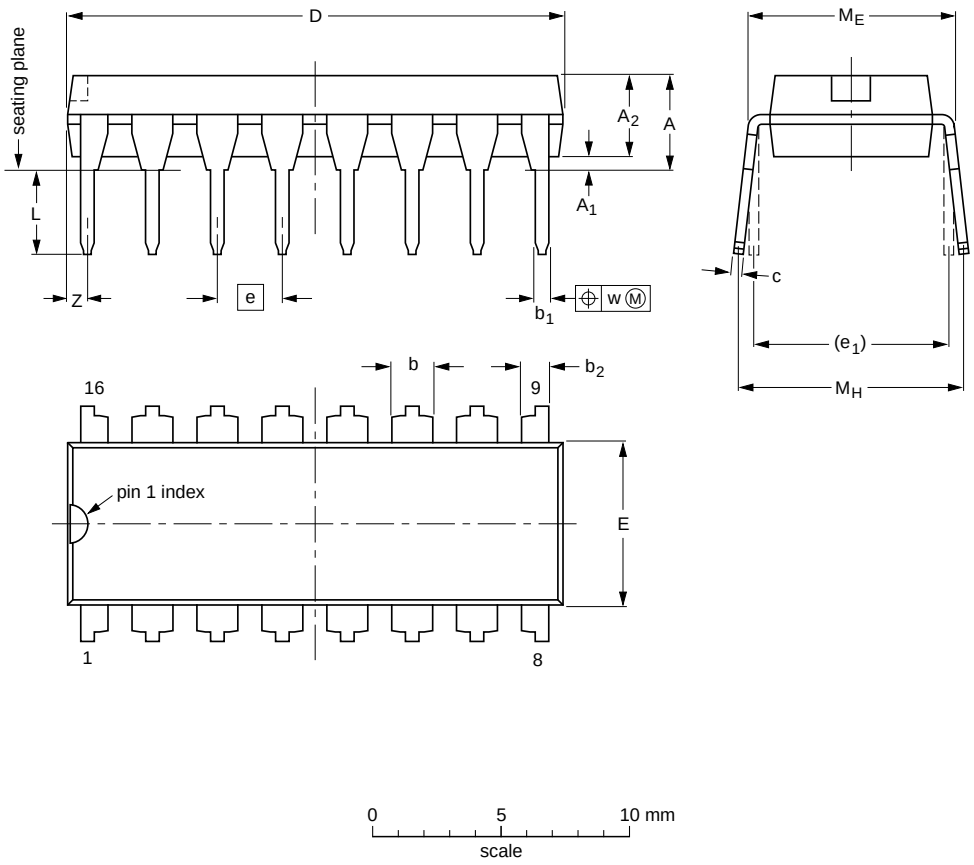
## 12. Package outline

**DIP16: plastic dual in-line package; 16 leads (300 mil)** **SOT38-4**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ min. | $A_2$ max. | b | $b_1$ | $b_2$ | c | D (1) | E (1) | e | $e_1$ | L | $M_E$ | $M_H$ | w | Z (1) max. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 4.2 | 0.51 | 3.2 | 1.73<br>1.30 | 0.53<br>0.38 | 1.25<br>0.85 | 0.36<br>0.23 | 19.50<br>18.55 | 6.48<br>6.20 | 2.54 | 7.62 | 3.60<br>3.05 | 8.25<br>7.80 | 10.0<br>8.3 | 0.254 | 0.76 |
| inches | 0.17 | 0.02 | 0.13 | 0.068<br>0.051 | 0.021<br>0.015 | 0.049<br>0.033 | 0.014<br>0.009 | 0.77<br>0.73 | 0.26<br>0.24 | 0.1 | 0.3 | 0.14<br>0.12 | 0.32<br>0.31 | 0.39<br>0.33 | 0.01 | 0.03 |

**Note**

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT38-4 | | | | | | ~~95-01-14~~<br>03-02-13 |

**Fig 9. Package outline SOT38-4 (DIP16)**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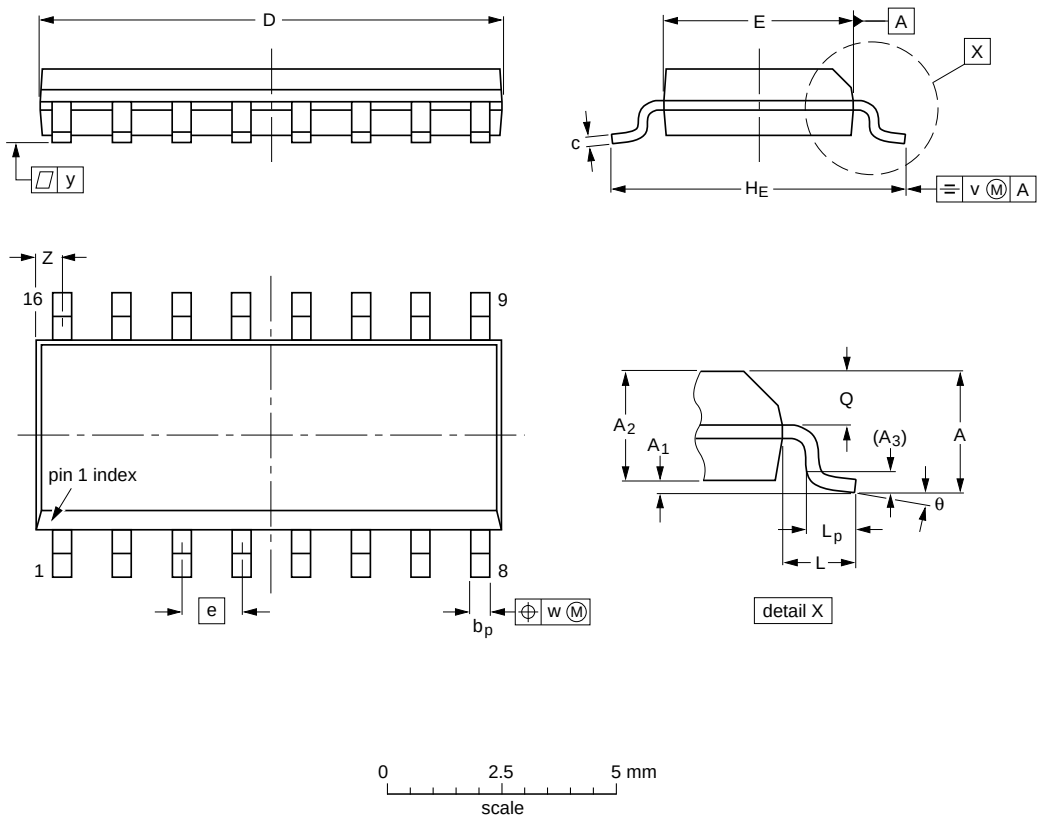
**SO16: plastic small outline package; 16 leads; body width 3.9 mm** **SOT109-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.75 | 0.25<br>0.10 | 1.45<br>1.25 | 0.25 | 0.49<br>0.36 | 0.25<br>0.19 | 10.0<br>9.8 | 4.0<br>3.8 | 1.27 | 6.2<br>5.8 | 1.05 | 1.0<br>0.4 | 0.7<br>0.6 | 0.25 | 0.25 | 0.1 | 0.7<br>0.3 | $8^o$<br>$0^o$ |
| inches | 0.069 | 0.010<br>0.004 | 0.057<br>0.049 | 0.01 | 0.019<br>0.014 | 0.0100<br>0.0075 | 0.39<br>0.38 | 0.16<br>0.15 | 0.05 | 0.244<br>0.228 | 0.041 | 0.039<br>0.016 | 0.028<br>0.020 | 0.01 | 0.01 | 0.004 | 0.028<br>0.012 | |

**Note**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT109-1 | 076E07 | MS-012 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig 10. Package outline SOT109-1 (SO16)**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## 13. Revision history

**Table 11. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| HEF4020B v.8 | 20111118 | Product data sheet | - | HEF4020B v.7 |
| Modifications: | • Legal pages updated.<br>• Changes in “General description” and “Features and benefits”.<br>• Section “Applications” removed. | | | |
| HEF4020B v.7 | 20111010 | Product data sheet | - | HEF4020B v.6 |
| HEF4020B v.6 | 20091127 | Product data sheet | - | HEF4020B v.5 |
| HEF4020B v.5 | 20090707 | Product data sheet | - | HEF4020B v.4 |
| HEF4020B v.4 | 20081204 | Product data sheet | - | HEF4020B_CNV v.3 |
| HEF4020B_CNV v.3 | 19950101 | Product specification | - | HEF4020B_CNV v.2 |
| HEF4020B_CNV v.2 | 19950101 | Product specification | - | - |


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# 14. Legal information

## 14.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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## 16. Contents



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