74HC299; 74HCT299

8-bit universal shift register; 3-state

Rev. 03 — 28 July 2008 Product data sheet

1. General description

The 74HC299; 74HCT299 are high-speed Si-gate CMOS devices which are pin-compatible with Low-power Schottky TTL (LSTTL) devices. They are specified in compliance with JEDEC standard no. 7A.

The 74HC299; 74HCT299 contain eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous shift-right, shift-left, parallel load and hold operations. An operation is determined by the mode select inputs S0 and S1, as shown in Table 3.

Pins I/O0 to I/O7 are flip-flop 3-state buffer outputs which allow them to operate as data inputs in parallel load mode. The serial outputs Q0 and Q7 are used for expansion in serial shifting of longer words.

A LOW signal on the asynchronous master reset input $\overline{MR}$ overrides the Sn and clock CP inputs and resets the flip-flops. All other state changes are initiated by the rising edge of the clock pulse. Inputs can change when the clock is in either state, provided that the recommended set-up and hold times are observed.

A HIGH signal on the 3-state output enable inputs $\overline{OE}1$ or $\overline{OE}2$ disables the 3-state buffers and the I/On outputs are set to the high-impedance OFF-state. In this condition, the shift, hold, load and reset operations still occur when preparing for a parallel load operation. The 3-state buffers are also disabled by HIGH signals on both S0 and S1.

2. Features

- Multiplexed inputs/outputs provide improved bit density
- Four operating modes:
  - Shift left
  - Shift right
  - Hold (store)
  - Load data
- Operates with output enable or at high-impedance OFF-state (Z)
- 3-state outputs drive bus lines directly
- Cascadable for n-bit word lengths
- ESD protection:
  - HBM JESD22-A114E exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Specified from –40 °C to +85 °C and from –40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC299				
74HC299D	–40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74HC299DB	–40 °C to +125 °C	SSOP20	plastic shrink small outline package; 20 leads; body width 5.3 mm	SOT339-1
74HC299N	–40 °C to +125 °C	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
74HC299PW	–40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74HCT299				
74HCT299D	–40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74HCT299DB	–40 °C to +125 °C	SSOP20	plastic shrink small outline package; 20 leads; body width 5.3 mm	SOT339-1
74HCT299N	–40 °C to +125 °C	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
74HCT299PW	–40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1

4. Functional diagram

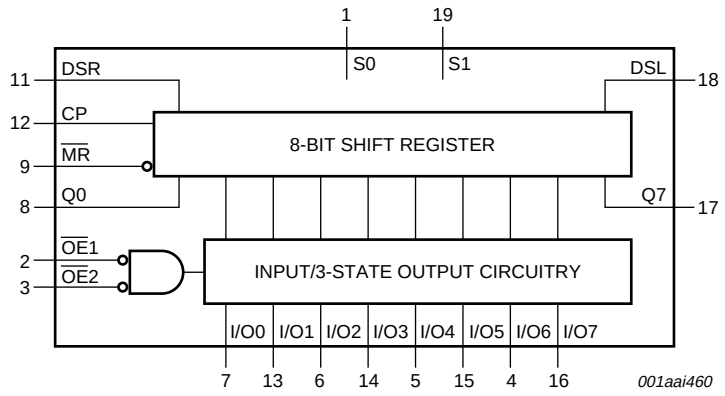


Fig 1. Functional diagram

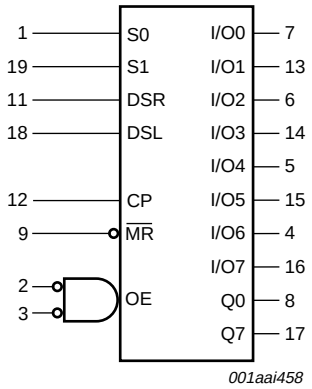


Fig 2. Logic symbol

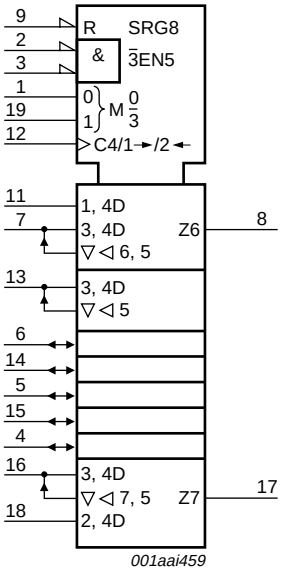


Fig 3. IEC logic symbol

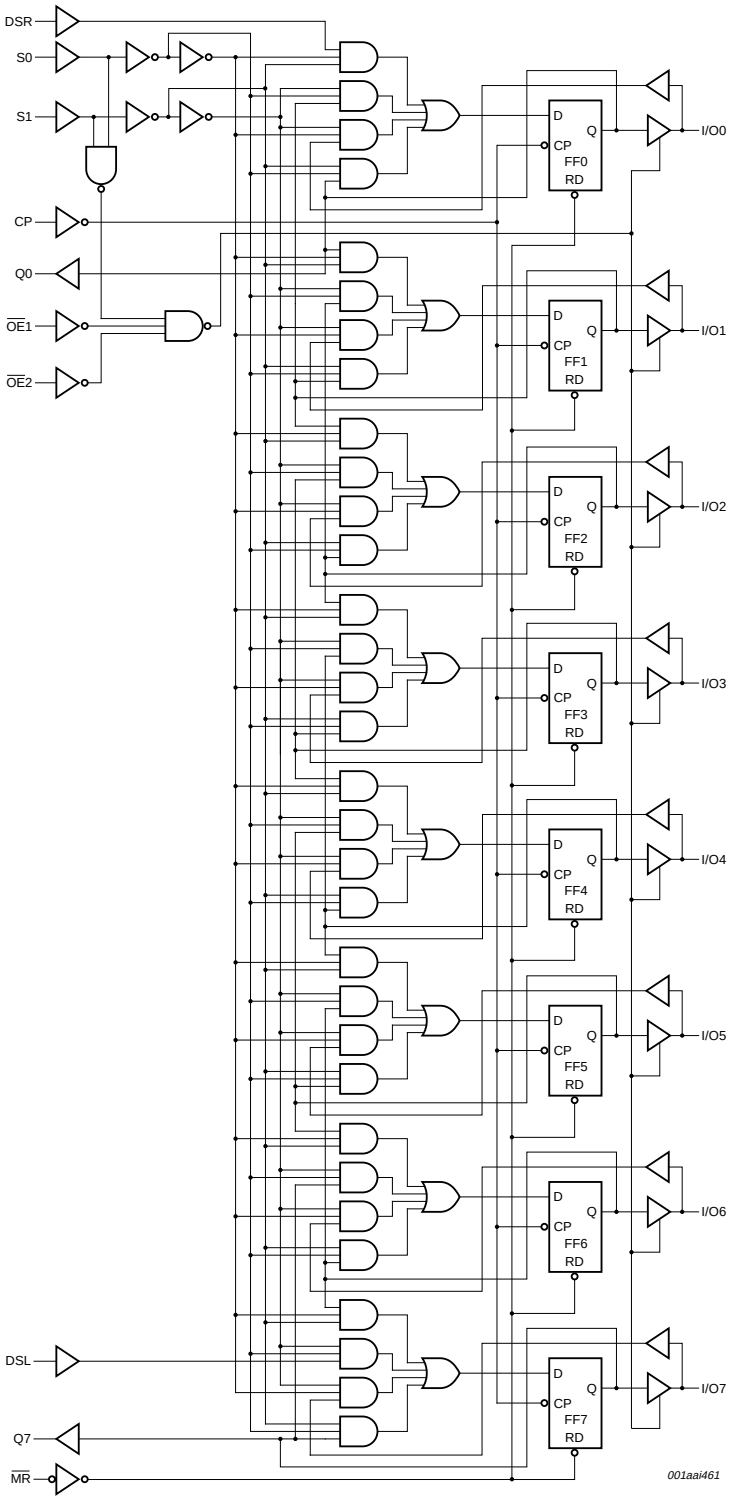


Fig 4. Logic diagram

5. Pinning information

5.1 Pinning

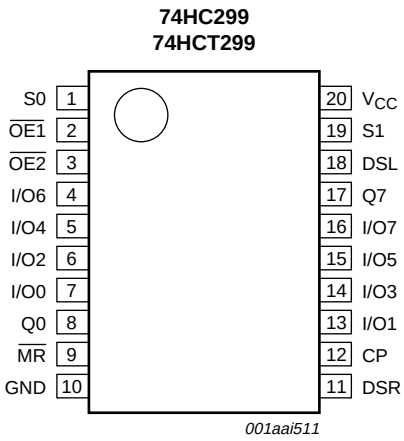


Fig 5. Pin configuration (SO20 and (T)SSOP20)

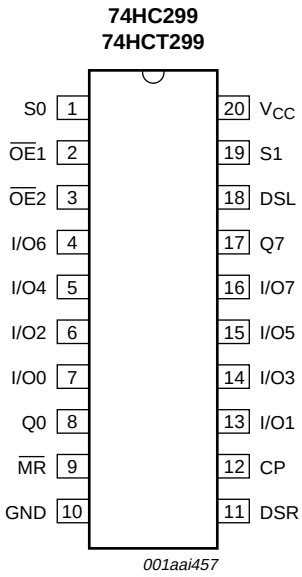


Fig 6. Pin configuration (DIP20)

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
S0	1	mode select input
$\overline{OE}$1	2	3-state output enable input (active LOW)
$\overline{OE}$2	3	3-state output enable input (active LOW)
I/O6	4	parallel data input or 3-state parallel output (bus driver)
I/O4	5	parallel data input or 3-state parallel output (bus driver)
I/O2	6	parallel data input or 3-state parallel output (bus driver)
I/O0	7	parallel data input or 3-state parallel output (bus driver)
Q0	8	serial output (standard output)
$\overline{MR}$	9	asynchronous master reset input (active LOW)
GND	10	ground (0 V)
DSR	11	serial data shift-right input
CP	12	clock input (LOW to HIGH, edge-triggered)
I/O1	13	parallel data input or 3-state parallel output (bus driver)
I/O3	14	parallel data input or 3-state parallel output (bus driver)
I/O5	15	parallel data input or 3-state parallel output (bus driver)
I/O7	16	parallel data input or 3-state parallel output (bus driver)
Q7	17	serial output (standard output)

Table 2. Pin description *...continued*

Symbol	Pin	Description
DSL	18	serial data shift-left input
S1	19	mode select input
V_{CC}	20	positive supply voltage

6. Functional description

Table 3. Function table[1]

Input				Response
$\overline{MR}$	S1	S0	CP	
L	X	X	X	asynchronous reset; Q0 to Q7 = LOW
H	H	H	↑	parallel load; I/On → Qn
H	L	H	↑	shift right; DSR → Q0, Q0 → Q1, etc.
H	H	L	↑	shift left; DSL → Q7, Q7 → Q6, etc.
H	L	L	X	hold

[1] H = HIGH voltage level;
L = LOW voltage level;
↑ = LOW to HIGH CP transition;
X = don't care.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7	V
I_{IK}	input clamping current	$V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_{OK}	output clamping current	$V_O < –0.5$ V or $V_O > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_O	output current	$–0.5 \text{ V} < V_O < V_{CC} + 0.5$ V				
	standard outputs			-	±25	mA
	bus driver outputs			-	±35	mA
I_{CC}	supply current					
	standard outputs			-	50	mA
	bus driver outputs			-	70	mA
I_{GND}	ground current					
	standard outputs			–50	-	mA
	bus driver outputs			–70	-	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = –40$ °C to +125 °C				
		DIP20 package	[2]	-	750	mW
		SO20 package	[3]	-	500	mW
		(T)SSOP20 package	[4]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] P_{tot} derates linearly at 12 mW/K above 70 °C.

[3] P_{tot} derates linearly at 8 mW/K above 70 °C.

[4] P_{tot} derates linearly at 5.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74HC299			74HCT299			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	-	+125	–40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate								
		V_{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V_{CC} = 4.5 V	-	1.67	139	-	1.67	1.39	ns/V
		V_{CC} = 6.0 V	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC299										
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V

Table 6. Static characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		all outputs								
		I_O = –20 µA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I_O = –20 µA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = –20 µA; V_{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		standard outputs								
		I_O = –4.0 mA; V_{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I_O = –5.2 mA; V_{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
		bus driver outputs								
		I_O = –6.0 mA; V_{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I_O = –7.8 mA; V_{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		all outputs								
		I_O = 20 µA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 µA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 µA; V_{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		standard outputs								
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
		bus driver outputs								
		I_O = 6.0 mA; V_{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I_O = 7.8 mA; V_{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	µA
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND; V_{CC} = 6.0 V	-	-	±0.5	-	±5.0	-	±10.0	µA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	8.0	-	80	-	160	µA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF
$C_{I/O}$	input/output capacitance		-	10	-	-	-	-	-	pF
C_{PD}	power dissipation capacitance	per package [1]	-	120	-	-	-	-	-	pF
74HCT299										
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V

Table 6. Static characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V								
		all outputs								
		I_O = –20 µA	4.4	4.5	-	4.4	-	4.4	-	V
		standard outputs								
		I_O = –4.0 mA	3.98	4.32	-	3.84	-	3.7	-	V
		bus driver outputs								
		I_O = –6.0 mA	3.98	4.32	-	3.84	-	3.7	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V								
		all outputs								
		I_O = 20 µA	-	0	0.1	-	0.1	-	0.1	V
		standard outputs								
		I_O = 4.0 mA	-	0.15	0.26	-	0.33	-	0.4	V
		bus driver outputs								
		I_O = 6.0 mA	-	0.16	0.26	-	0.33	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 5.5 V	-	-	±0.1	-	±1.0	-	±1.0	µA
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND per input pin; other inputs at V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	±0.5	-	±5.0	-	±10.0	µA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	8.0	-	80	-	160	µA
ΔI_{CC}	additional supply current	per input pin; $V_I = V_{CC}$ – 2.1 V; other inputs at V_{CC} or GND; I_O = 0 A; V_{CC} = 4.5 V to 5.5 V								
		I/On, DSR, DSL, $\overline{MR}$ and S1	-	25	90	-	112.5	-	122.5	µA
		CP, S0	-	60	216	-	270	-	294	µA
		$\overline{OE}$n	-	30	108	-	135	-	147	µA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF
$C_{I/O}$	input/output capacitance		-	10	-	-	-	-	-	pF
C_{PD}	power dissipation capacitance	per package [1]	-	125	-	-	-	-	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
V_I = GND to V_{CC} for 74HC299;
V_I = GND to (V_{CC} – 1.5 V) for 74HCT299.

10. Dynamic characteristics

Table 7. Dynamic characteristics

GND (ground = 0 V); for test circuit, see Figure 11.

Symbol	Parameter	Conditions		25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
74HC299											
t_{pd}	propagation delay	CP to Q0, Q7; see Figure 7	[1]								
		V_{CC} = 2.0 V		-	66	200	-	250	-	300	ns
		V_{CC} = 4.5 V		-	24	40	-	50	-	60	ns
		V_{CC} = 5.0 V; C_L = 15 pF		-	20	-	-	-	-	-	ns
		V_{CC} = 6.0 V		-	19	34	-	43	-	51	ns
		CP to I/On; see Figure 7									
		V_{CC} = 2.0 V		-	66	200	-	250	-	300	ns
		V_{CC} = 4.5 V		-	24	40	-	50	-	60	ns
		V_{CC} = 5.0 V; C_L = 15 pF		-	20	-	-	-	-	-	ns
		V_{CC} = 6.0 V		-	19	34	-	43	-	51	ns
		$\overline{MR}$ to Q0, Q7 or I/On; see Figure 8	[2]								
		V_{CC} = 2.0 V		-	66	200	-	250	-	300	ns
		V_{CC} = 4.5 V		-	24	40	-	50	-	60	ns
		V_{CC} = 5.0 V; C_L = 15 pF		-	20	-	-	-	-	-	ns
		V_{CC} = 6.0 V		-	19	34	-	43	-	51	ns
t_t	transition time	bus driver (I/On); see Figure 7	[3]								
		V_{CC} = 2.0 V		-	14	60	-	75	-	90	ns
		V_{CC} = 4.5 V		-	5	12	-	15	-	18	ns
		V_{CC} = 6.0 V		-	4	10	-	13	-	15	ns
		standard (Q0, Q7); see Figure 7									
		V_{CC} = 2.0 V		-	19	75	-	95	-	110	ns
		V_{CC} = 4.5 V		-	7	15	-	19	-	22	ns
		V_{CC} = 6.0 V		-	6	13	-	16	-	19	ns

Table 7. Dynamic characteristics *…continued*

GND (ground = 0 V); for test circuit, see Figure 11.

Symbol	Parameter	Conditions		25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
t_W	pulse width	CP HIGH or LOW; see Figure 7									
		V_{CC} = 2.0 V		80	17	-	100	-	120	-	ns
		V_{CC} = 4.5 V		16	6	-	20	-	24	-	ns
		V_{CC} = 6.0 V		14	5	-	17	-	20	-	ns
		$\overline{MR}$ LOW; see Figure 8									
		V_{CC} = 2.0 V		80	19	-	100	-	120	-	ns
		V_{CC} = 4.5 V		16	7	-	20	-	24	-	ns
		V_{CC} = 6.0 V		14	6	-	17	-	20	-	ns
t_{PZH}	OFF-state to HIGH propagation delay	$\overline{OE}$n to I/On; see Figure 10	[4]								
		V_{CC} = 2.0 V		-	50	155	-	195	-	235	ns
		V_{CC} = 4.5 V		-	18	31	-	39	-	47	ns
		V_{CC} = 6.0 V		-	14	26	-	33	-	40	ns
t_{PZL}	OFF-state to LOW propagation delay	$\overline{OE}$n to I/On; see Figure 10									
		V_{CC} = 2.0 V		-	41	130	-	165	-	195	ns
		V_{CC} = 4.5 V		-	15	26	-	33	-	39	ns
		V_{CC} = 6.0 V		-	12	22	-	28	-	33	ns
t_{PHZ}	HIGH to OFF-state propagation delay	$\overline{OE}$n to I/On; see Figure 10	[5]								
		V_{CC} = 2.0 V		-	66	185	-	230	-	280	ns
		V_{CC} = 4.5 V		-	24	37	-	46	-	56	ns
		V_{CC} = 6.0 V		-	19	31	-	39	-	48	ns
t_{PLZ}	LOW to OFF-state propagation delay	$\overline{OE}$n to I/On; see Figure 10									
		V_{CC} = 2.0 V		-	55	155	-	195	-	235	ns
		V_{CC} = 4.5 V		-	20	31	-	39	-	47	ns
		V_{CC} = 6.0 V		-	16	26	-	33	-	40	ns
t_{rec}	recovery time	$\overline{MR}$ to CP; see Figure 8									
		V_{CC} = 2.0 V		5	–14	-	5	-	5	-	ns
		V_{CC} = 4.5 V		5	–5	-	5	-	5	-	ns
		V_{CC} = 6.0 V		5	–4	-	5	-	5	-	ns

Table 7. Dynamic characteristics *…continued*

GND (ground = 0 V); for test circuit, see Figure 11.

Symbol	Parameter	Conditions		25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
t_{su}	set-up time	DSR, DSL to CP; see Figure 7									
		V_{CC} = 2.0 V		100	33	-	125	-	150	-	ns
		V_{CC} = 4.5 V		20	12	-	25	-	30	-	ns
		V_{CC} = 6.0 V		17	10	-	21	-	26	-	ns
		S0, S1 to CP; see Figure 9									
		V_{CC} = 2.0 V		100	33	-	125	-	150	-	ns
		V_{CC} = 4.5 V		20	12	-	25	-	30	-	ns
		V_{CC} = 6.0 V		17	10	-	21	-	26	-	ns
		I/On to CP; see Figure 7									
		V_{CC} = 2.0 V		125	39	-	155	-	190	-	ns
		V_{CC} = 4.5 V		25	14	-	31	-	38	-	ns
		V_{CC} = 6.0 V		21	11	-	26	-	32	-	ns
t_h	hold time	I/On, DSR, DSL to CP; see Figure 7									
		V_{CC} = 2.0 V		0	–14	-	0	-	0	-	ns
		V_{CC} = 4.5 V		0	–5	-	0	-	0	-	ns
		V_{CC} = 6.0 V		0	–4	-	0	-	0	-	ns
		S0, S1 to CP; see Figure 9									
		V_{CC} = 2.0 V		0	–28	-	0	-	0	-	ns
		V_{CC} = 4.5 V		0	–10	-	0	-	0	-	ns
		V_{CC} = 6.0 V		0	–8	-	0	-	0	-	ns
f_{max}	maximum frequency	CP input; see Figure 7									
		V_{CC} = 2.0 V		5.0	15	-	4.0	-	3.4	-	MHz
		V_{CC} = 4.5 V		25	45	-	20	-	17	-	MHz
		V_{CC} = 5.0 V; C_L = 15 pF		-	50	-	-	-	-	-	MHz
		V_{CC} = 6.0 V		29	54	-	24	-	20	-	MHz
74HCT299											
t_{pd}	propagation delay	CP to Q0, Q7; see Figure 7	[1]								
		V_{CC} = 4.5 V		-	22	37	-	46	-	56	ns
		V_{CC} = 5.0 V; C_L = 15 pF		-	19	-	-	-	-	-	ns
		CP to I/On; see Figure 7									
		V_{CC} = 4.5 V		-	22	37	-	46	-	56	ns
		V_{CC} = 5.0 V; C_L = 15 pF		-	19	-	-	-	-	-	ns
		$\overline{MR}$ to Q0, Q7 or I/On; see Figure 8	[2]								
		V_{CC} = 4.5 V		-	27	46	-	58	-	69	ns
		V_{CC} = 5.0 V; C_L = 15 pF		-	23	-	-	-	-	-	ns

Table 7. Dynamic characteristics *…continued*

GND (ground = 0 V); for test circuit, see Figure 11.

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_t	transition time	bus driver (I/On); see Figure 7 [3]								
		V_{CC} = 4.5 V	-	5	12	-	15	-	18	ns
		standard (Q0, Q7); see Figure 7								
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns
t_W	pulse width	clock HIGH or LOW; see Figure 7								
		V_{CC} = 4.5 V	20	10	-	25	-	30	-	ns
		master reset LOW; see Figure 8								
		V_{CC} = 4.5 V	20	11	-	25	-	30	-	ns
t_{en}	enable time	$\overline{OE}$n to I/On; see Figure 10 [4]								
		V_{CC} = 4.5 V	-	19	30	-	38	-	45	ns
t_{PHZ}	HIGH to OFF-state propagation delay	$\overline{OE}$n to I/On; see Figure 10 [5]								
		V_{CC} = 4.5 V	-	24	37	-	46	-	56	ns
t_{PLZ}	LOW to OFF-state propagation delay	$\overline{OE}$n to I/On; see Figure 10								
		V_{CC} = 4.5 V	-	20	32	-	40	-	48	ns
t_{rec}	recovery time	$\overline{MR}$ to CP; see Figure 8								
		V_{CC} = 4.5 V	10	2	-	9	-	11	-	ns
t_{su}	set-up time	I/On, DSR, DSL to CP; see Figure 7								
		V_{CC} = 4.5 V	25	14	-	31	-	38	-	ns
		S0, S1 to CP; see Figure 9								
		V_{CC} = 4.5 V	32	18	-	40	-	48	-	ns
t_h	hold time	I/On, DSR, DSL to CP; see Figure 7								
		V_{CC} = 4.5 V	0	–11	-	0	-	0	-	ns
		S0, S1 to CP; see Figure 9								
		V_{CC} = 4.5 V	0	–17	-	0	-	0	-	ns
f_{max}	maximum frequency	CP input; see Figure 7								
		V_{CC} = 4.5 V	25	42	-	20	-	17	-	MHz
		V_{CC} = 5.0 V; C_L = 15 pF	-	46	-	-	-	-	-	MHz

[1] t_{pd} is the same as t_{PHL} and t_{PLH}.

[2] t_{pd} is the same as t_{PHL}.

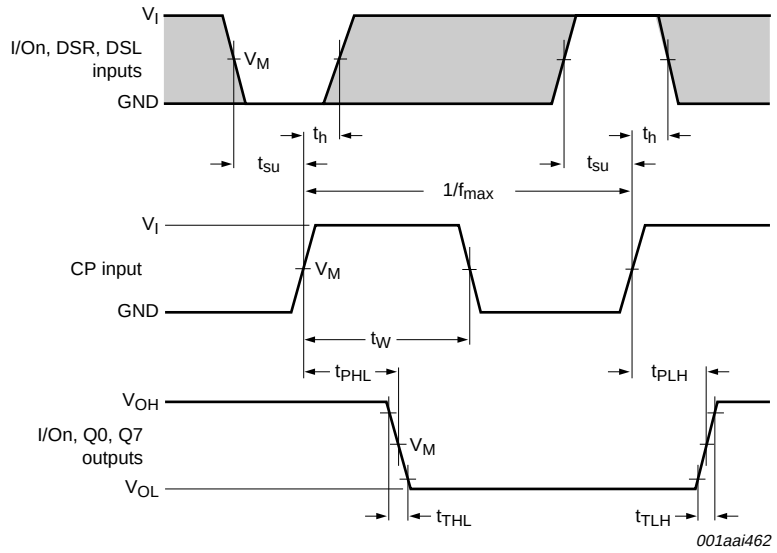
[3] t_t is the same as t_{THL} and t_{TLH}.

[4] t_{en} is the same as t_{PZH} and t_{PZL}.

[5] t_{dis} is the same as t_{PHZ} and t_{PLZ}.

[6] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching.

11. Waveforms

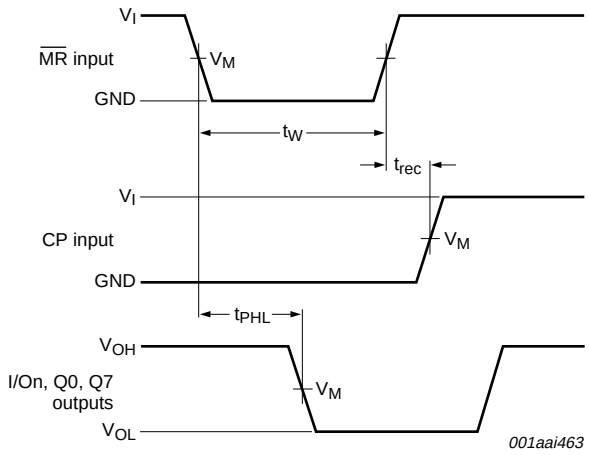


The shaded areas indicate when the input is permitted to change for predictable output performance.

Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

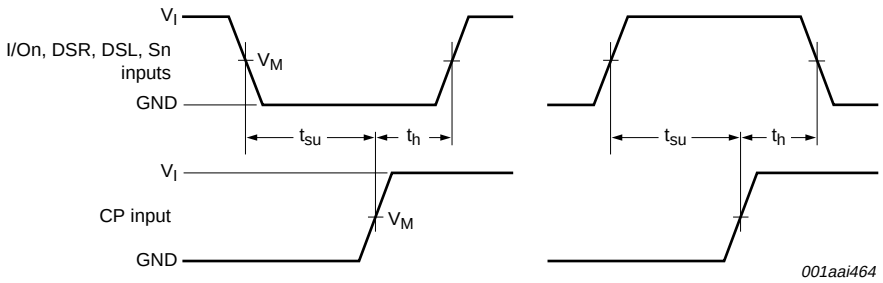
Fig 7. Clock pulse to outputs I/On, Q0, Q7 propagation delays, the clock pulse width, the I/On, DSR and DSL to clock pulse set-up and hold times, the output transition times and the maximum clock frequency



Measurement points are given in Table 8.

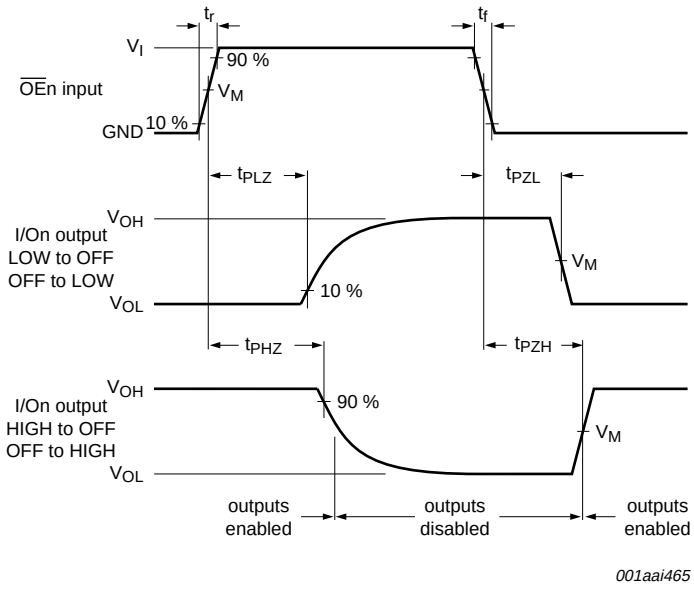
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 8. The master reset pulse width (LOW), the master reset to outputs I/On, Q0, Q7 propagation delays and the master reset to clock pulse removal time



Measurement points are given in Table 8.

Fig 9. Set-up and hold times from the mode control inputs S0, S1 to the clock pulse



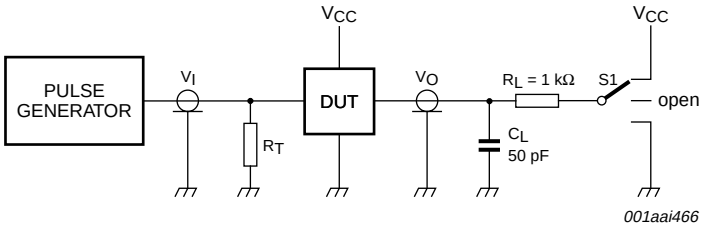
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 10. 3-state enable and disable times for $\overline{OE}$n inputs

Table 8. Measurement points

Type	Input		Output
	V_I	V_M	V_M
74HC299	V_{CC}	$0.5V_{CC}$	$0.5V_{CC}$
74HCT299	3 V	1.3 V	1.3 V



Test data is given in Table 9.

Definitions for test circuit:

DUT = Device Under Test.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

S1 = Test selection switch

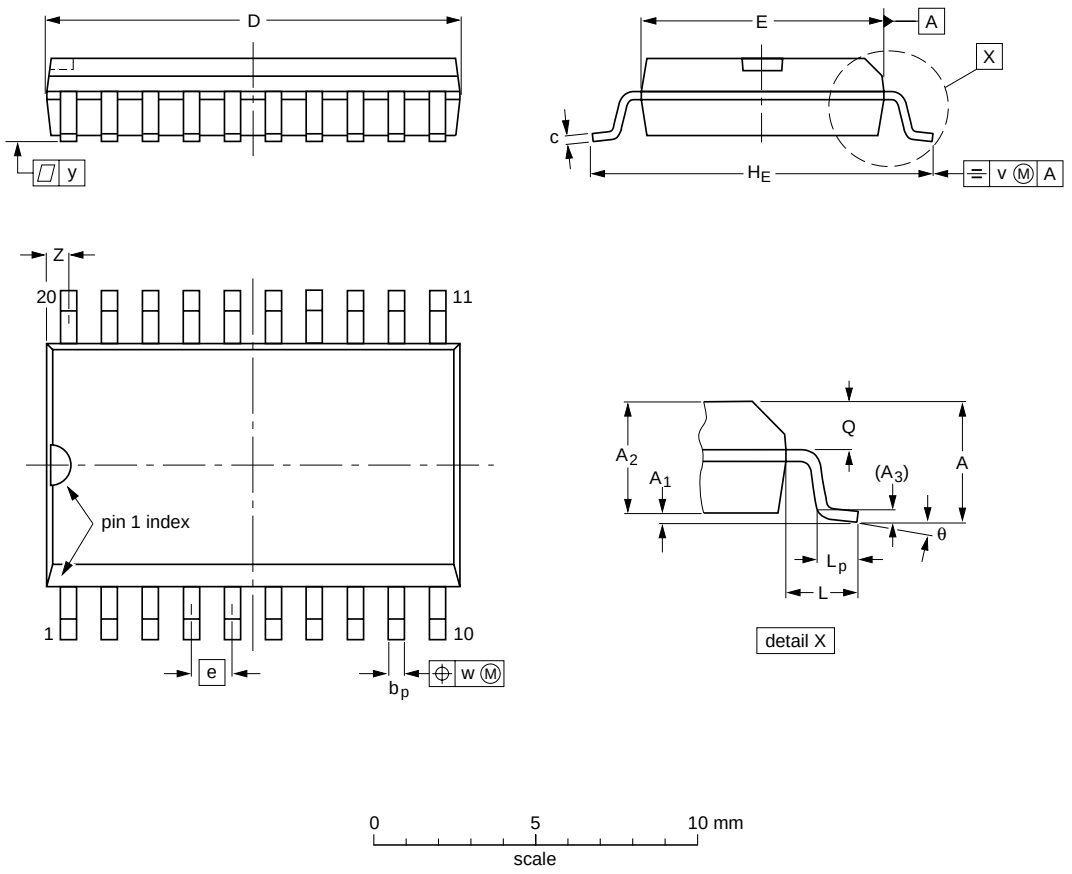
Fig 11. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load		S1 position
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}
74HC299	V_{CC}	6 ns	15 pF, 50 pF	1 kΩ	open
74HCT299	3 V	6 ns	15 pF, 50 pF	1 kΩ	open

12. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

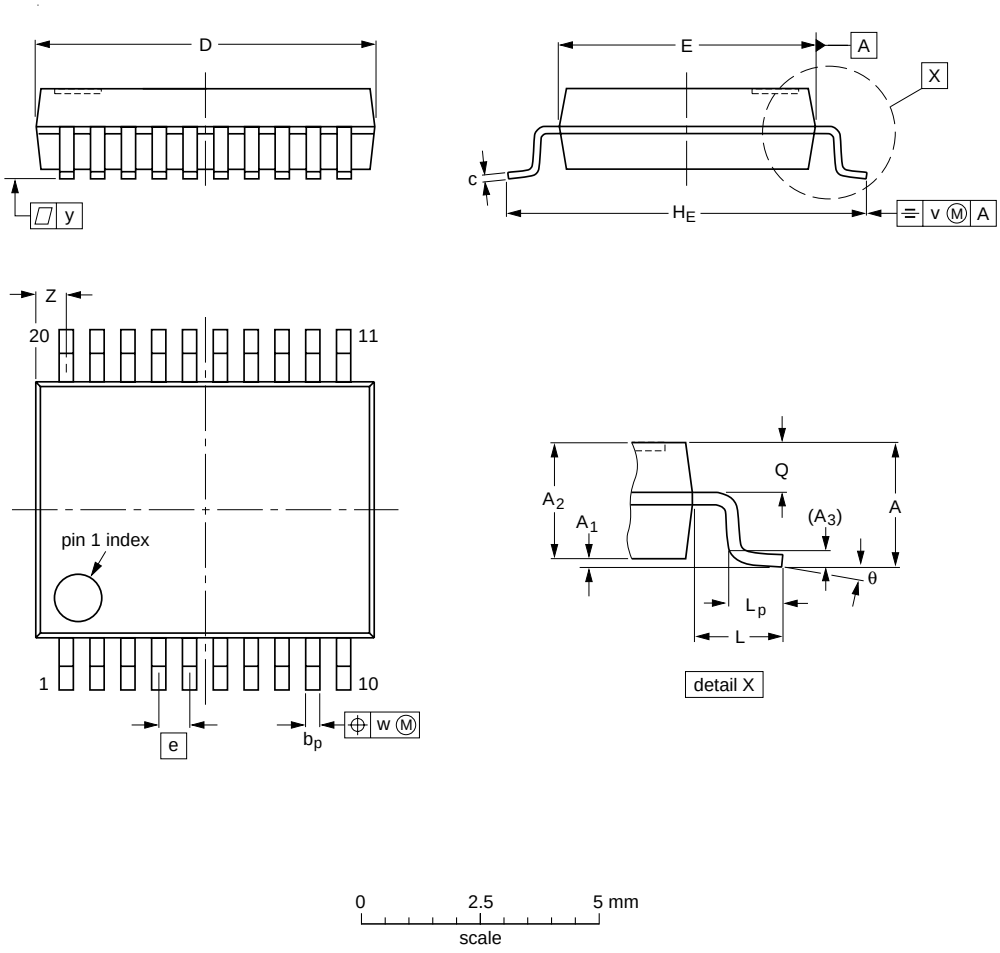
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				~~99-12-27~~ 03-02-19

Fig 12. Package outline SOT163-1 (SO20)

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm **SOT339-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8^o 0^o

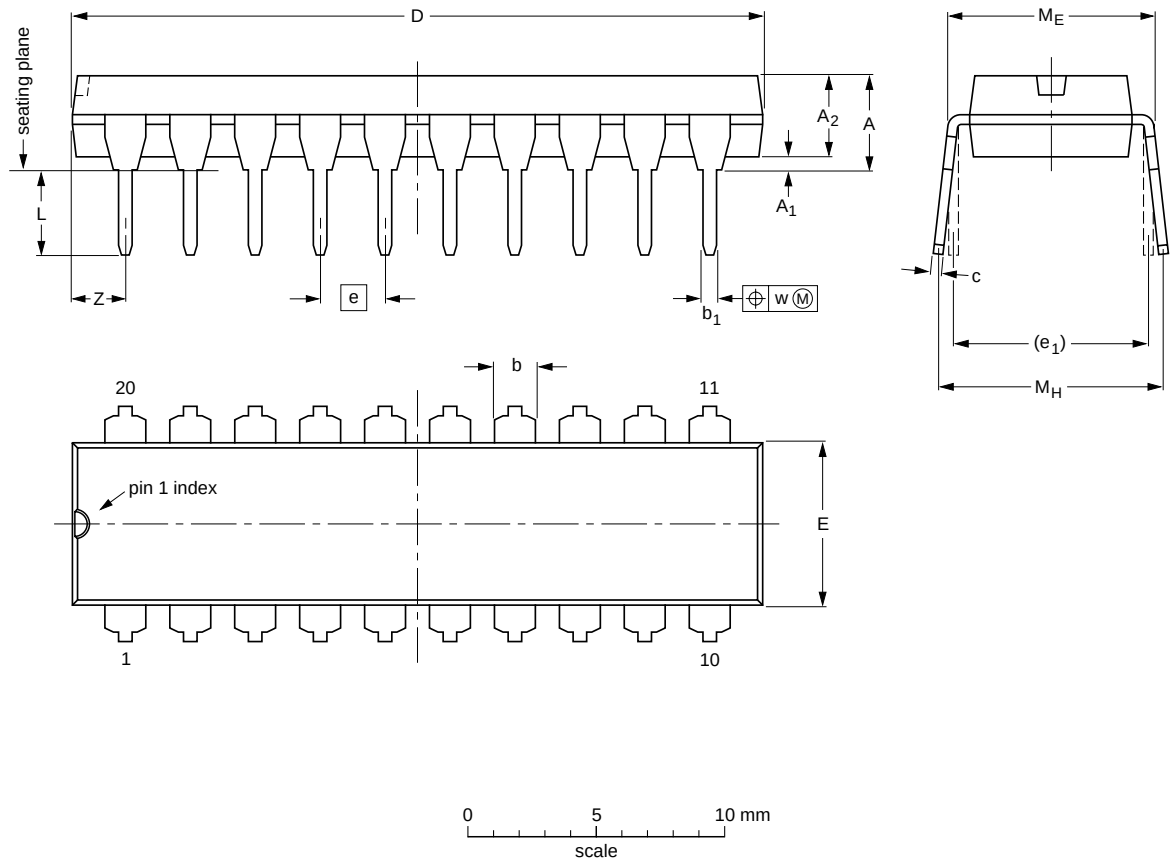
Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT339-1		MO-150				~~99-12-27~~ 03-02-19

Fig 13. Package outline SOT339-1 (SSOP20)

DIP20: plastic dual in-line package; 20 leads (300 mil) **SOT146-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

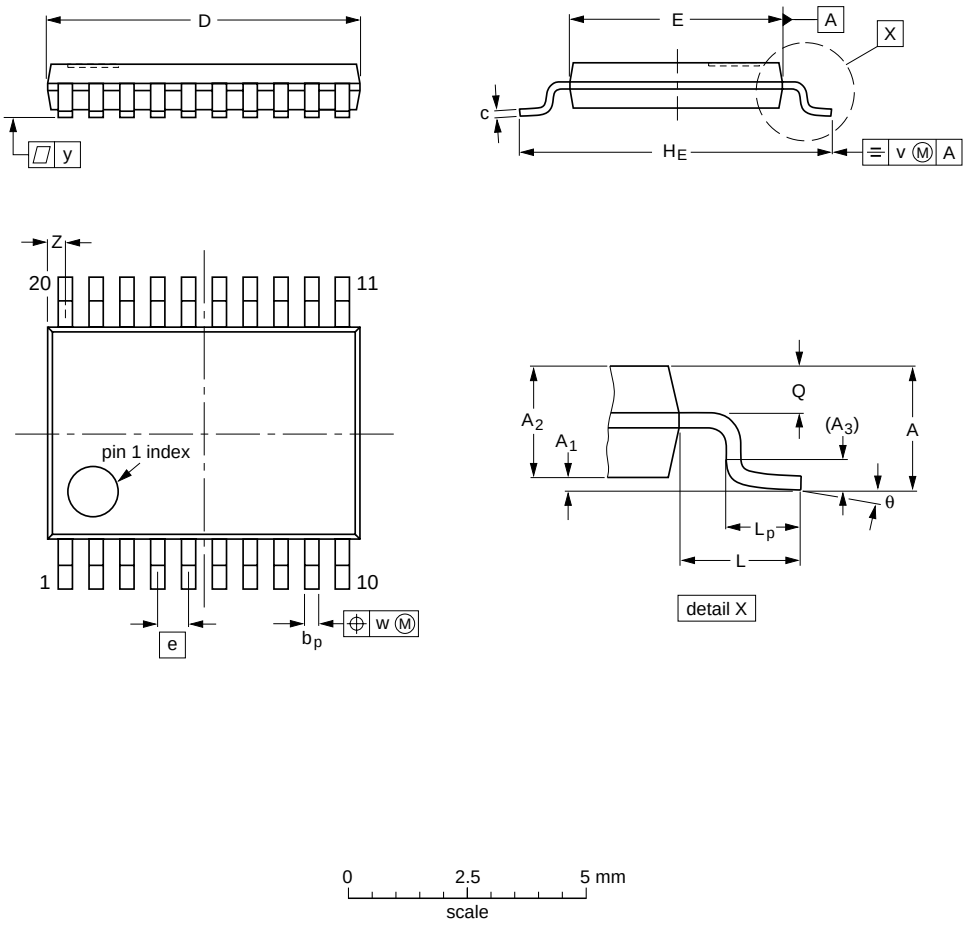
Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT146-1		MS-001	SC-603			~~99-12-27~~ 03-02-13

Fig 14. Package outline SOT146-1 (DIP20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				~~99-12-27~~ 03-02-19

Fig 15. Package outline SOT360-1 (TSSOP20)

13. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT299_3	20080728	Product data sheet	-	74HC_HCT299_CNV_2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Section 3: Ordering information added • Section 12: Package outline drawings added • Section 9 “Static characteristics”: Family data added • Section 11 “Waveforms”: Test circuit added			
74HC_HCT299_CNV_2	19970828	Product specification	-	-

14. Legal information

14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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