

74HC373; 74HCT373

Octal D-type transparent latch; 3-state

Rev. 5 — 13 December 2011

Product data sheet

1. General description

The 74HC373; 74HCT373 is a high-speed Si-gate CMOS device and is pin compatible with Low-power Schottky TTL. It is specified in compliance with JEDEC standard no. 7A.

The 74HC373; 74HCT373 is an octal D-type transparent latch featuring separate D-type inputs for each latch and 3-state outputs for bus oriented applications. A latch enable (LE) input and an output enable (\overline{OE}) input are common to all latches.

The 74HC373; 74HCT373 consists of eight D-type transparent latches with 3-state true outputs. When LE is HIGH, data at the D_n inputs enters the latches. In this condition the latches are transparent, i.e. a latch output will change state each time its corresponding D input changes.

When LE is LOW the latches store the information that was present at the D inputs a set-up time preceding the HIGH-to-LOW transition of LE. When \overline{OE} is LOW, the contents of the 8 latches are available at the outputs. When \overline{OE} is HIGH, the outputs go to the high-impedance OFF-state. Operation of the \overline{OE} input does not affect the state of the latches.

The 74HC373; 74HCT373 is functionally identical to:

- 74HC563; 74HCT563: but inverted outputs and different pin arrangement
- 74HC573; 74HCT573: but different pin arrangement

2. Features and benefits

- 3-state non-inverting outputs for bus oriented applications
- Common 3-state output enable input
- Functionally identical to the 74HC563; 74HCT563 and 74HC573; 74HCT573
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2 000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C



3. Ordering information

Table 1. Ordering information

| Type number | Package | | | |
|-------------------------|-------------------|----------|--|----------|
| | Temperature range | Name | Description | Version |
| 74HC373N 74HCT373N | -40 °C to +125 °C | DIP20 | plastic dual in-line package; 20 leads (300 mil) | SOT146-1 |
| 74HC373D 74HCT373D | -40 °C to +125 °C | SO20 | plastic small outline package; 20 leads; body width 7.5 mm | SOT163-1 |
| 74HC373DB 74HCT373DB | -40 °C to +125 °C | SSOP20 | plastic shrink small outline package; 20 leads; body width 5.3 mm | SOT339-1 |
| 74HC373PW 74HCT373PW | -40 °C to +125 °C | TSSOP20 | plastic thin shrink small outline package; 20 leads; body width 4.4 mm | SOT360-1 |
| 74HC373BQ 74HCT373BQ | -40 °C to +125 °C | DHVQFN20 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm | SOT764-1 |

4. Functional diagram

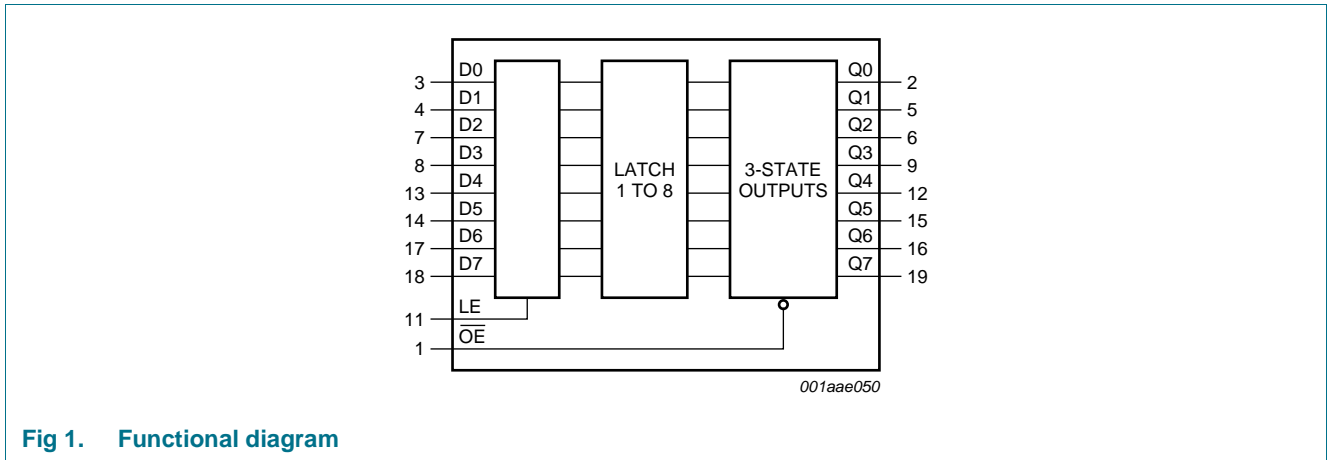


Fig 1. Functional diagram

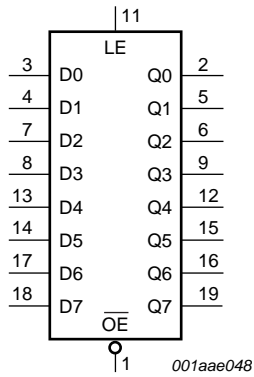


Fig 2. Logic symbol

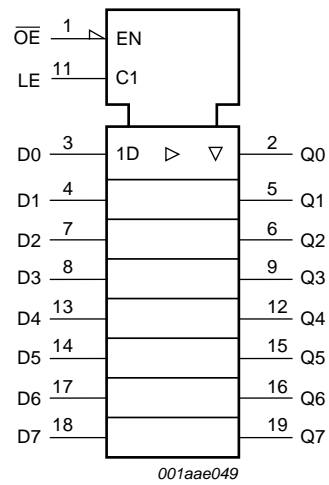


Fig 3. IEC logic symbol

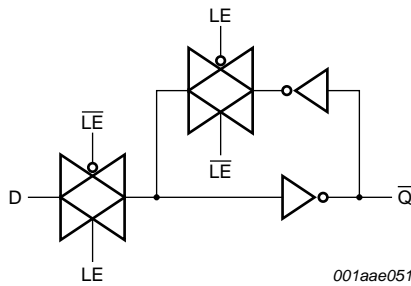


Fig 4. Logic diagram (one latch)

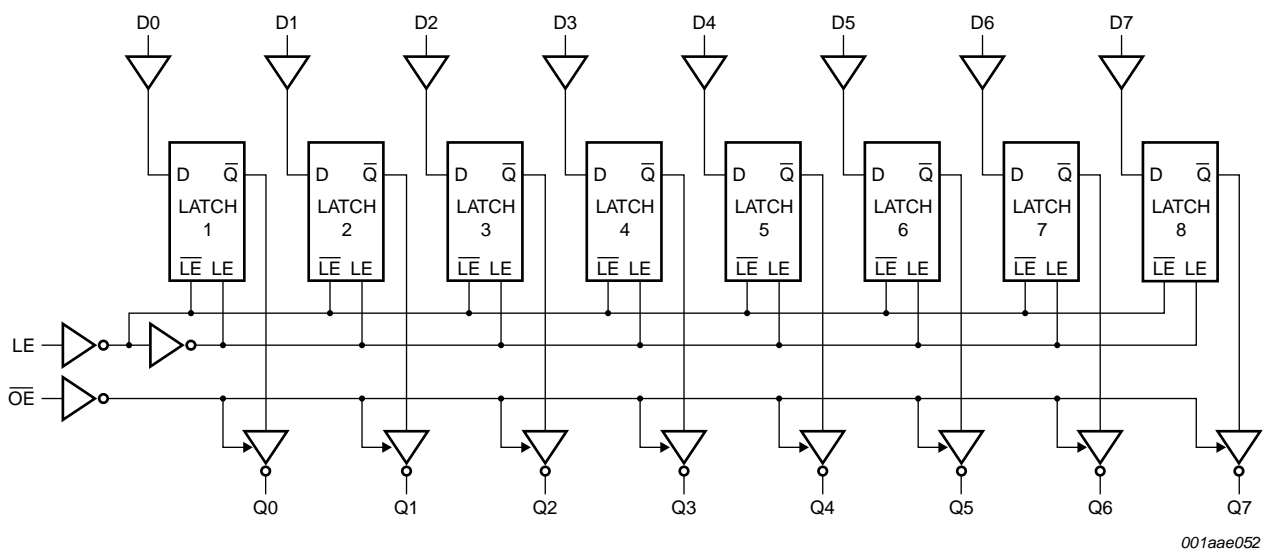
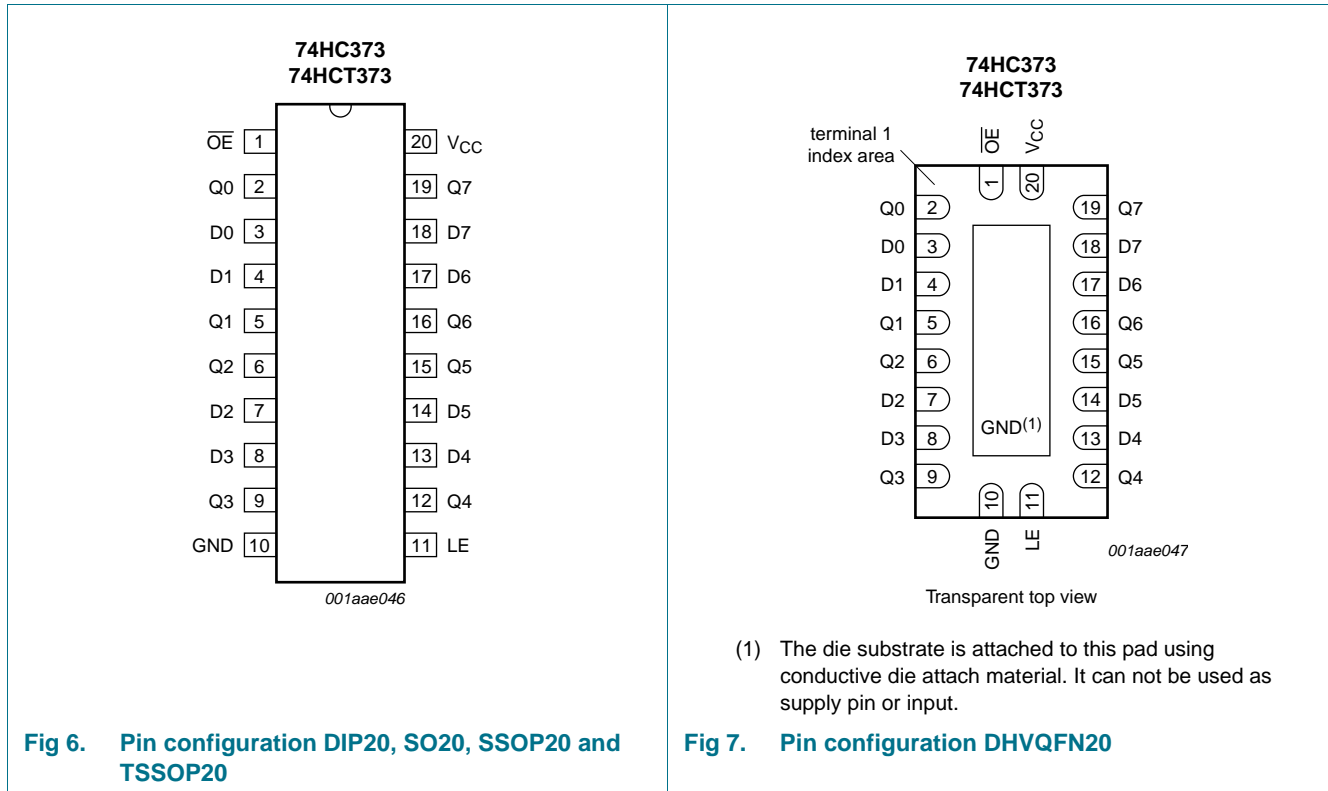


Fig 5. Logic diagram

5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|--------------------------------|----------------------------|--|
| OE | 1 | 3-state output enable input (active LOW) |
| Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7 | 2, 5, 6, 9, 12, 15, 16, 19 | 3-state latch output |
| D0, D1, D2, D3, D4, D5, D6, D7 | 3, 4, 7, 8, 13, 14, 17, 18 | data input |
| GND | 10 | ground (0 V) |
| LE | 11 | latch enable input (active HIGH) |
| V _{CC} | 20 | supply voltage |

6. Functional description

6.1 Function table

Table 3. Function table^[1]

| Operating mode | Control | | Input | Internal latches | Output |
|---|---------|----|-------|------------------|--------|
| | OE | LE | Dn | | Qn |
| Enable and read register (transparent mode) | L | H | L | L | L |
| | | | H | H | H |
| Latch and read register | L | L | l | L | L |
| | | | h | H | H |
| Latch register and disable outputs | H | X | X | X | Z |

- [1] H = HIGH voltage level;
 h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition;
 L = LOW voltage level;
 l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition;
 X = don't care;
 Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit | |
|------------------|-------------------------|---|------|------|------|----|
| V _{CC} | supply voltage | | -0.5 | +7 | V | |
| I _{IK} | input clamping current | V _I < -0.5 V or V _I > V _{CC} + 0.5 V | - | ±20 | mA | |
| I _{OK} | output clamping current | V _O < -0.5 V or V _O > V _{CC} + 0.5 V | - | ±20 | mA | |
| I _O | output current | V _O = -0.5 V to (V _{CC} + 0.5 V) | - | ±35 | mA | |
| I _{CC} | supply current | | - | +70 | mA | |
| I _{GND} | ground current | | - | -70 | mA | |
| T _{stg} | storage temperature | | -65 | +150 | °C | |
| P _{tot} | total power dissipation | DIP20 package | [1] | - | 750 | mW |
| | | SO20 package | [2] | - | 500 | mW |
| | | SSOP20 package | [3] | - | 500 | mW |
| | | TSSOP20 package | [3] | - | 500 | mW |
| | | DHVQFN20 package | [4] | - | 500 | mW |

- [1] For DIP20 package: P_{tot} derates linearly with 12 mW/K above 70 °C.
 [2] For SO20: P_{tot} derates linearly with 8 mW/K above 70 °C.
 [3] For SSOP20 and TSSOP20 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.
 [4] For DHVQFN20 package: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

| Symbol | Parameter | Conditions | 74HC373 | | | 74HCT373 | | | Unit |
|------------------|-------------------------------------|-------------------------|---------|------|-----------------|----------|------|-----------------|------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| V _{CC} | supply voltage | | 2.0 | 5.0 | 6.0 | 4.5 | 5.0 | 5.5 | V |
| V _I | input voltage | | 0 | - | V _{CC} | 0 | - | V _{CC} | V |
| V _O | output voltage | | 0 | - | V _{CC} | 0 | - | V _{CC} | V |
| T _{amb} | ambient temperature | | -40 | +25 | +125 | -40 | +25 | +125 | °C |
| Δt/ΔV | input transition rise and fall rate | V _{CC} = 2.0 V | - | - | 625 | - | - | - | ns/V |
| | | V _{CC} = 4.5 V | - | 1.67 | 139 | - | 1.67 | 139 | ns/V |
| | | V _{CC} = 6.0 V | - | - | 83 | - | - | - | ns/V |

9. Static characteristics

Table 6. Static characteristics 74HC373

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|---------------------------|---|------|------|------|------|
| T_{amb} = 25 °C | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 2.0 V | 1.5 | 1.2 | - | V |
| | | V _{CC} = 4.5 V | 3.15 | 2.4 | - | V |
| | | V _{CC} = 6.0 V | 4.2 | 3.2 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 2.0 V | - | 0.8 | 0.5 | V |
| | | V _{CC} = 4.5 V | - | 2.1 | 1.35 | V |
| | | V _{CC} = 6.0 V | - | 2.8 | 1.8 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} | - | - | - | |
| | | I _O = -20 μA; V _{CC} = 2.0 V | 1.9 | 2.0 | - | V |
| | | I _O = -20 μA; V _{CC} = 4.5 V | 4.4 | 4.5 | - | V |
| | | I _O = -20 μA; V _{CC} = 6.0 V | 5.9 | 6.0 | - | V |
| | | I _O = -6.0 mA; V _{CC} = 4.5 V | 3.98 | 4.32 | - | V |
| | | I _O = -7.8 mA; V _{CC} = 6.0 V | 5.48 | 5.81 | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | - | - | - | |
| | | I _O = 20 μA; V _{CC} = 2.0 V | - | 0 | 0.1 | V |
| | | I _O = 20 μA; V _{CC} = 4.5 V | - | 0 | 0.1 | V |
| | | I _O = 20 μA; V _{CC} = 6.0 V | - | 0 | 0.1 | V |
| | | I _O = 6.0 mA; V _{CC} = 4.5 V | - | 0.15 | 0.26 | V |
| | | I _O = 7.8 mA; V _{CC} = 6.0 V | - | 0.16 | 0.26 | V |
| I _I | input leakage current | V _I = V _{CC} or GND; V _{CC} = 6.0 V | - | - | ±0.1 | μA |
| I _{OZ} | OFF-state output current | V _I = V _{IH} or V _{IL} ; V _{CC} = 6.0 V; V _O = V _{CC} or GND | - | - | ±0.5 | μA |
| I _{CC} | supply current | V _{CC} = 6.0 V; I _O = 0 A; V _I = V _{CC} or GND | - | - | 8.0 | μA |
| C _I | input capacitance | | - | 3.5 | - | pF |

Table 6. Static characteristics 74HC373 ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|---------------------------|---|------|-----|------|------|
| T_{amb} = -40 °C to +85 °C | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 2.0 V | 1.5 | - | - | V |
| | | V _{CC} = 4.5 V | 3.15 | - | - | V |
| | | V _{CC} = 6.0 V | 4.2 | - | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 2.0 V | - | - | 0.5 | V |
| | | V _{CC} = 4.5 V | - | - | 1.35 | V |
| | | V _{CC} = 6.0 V | - | - | 1.8 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} | | | | |
| | | I _O = -20 μA; V _{CC} = 2.0 V | 1.9 | - | - | V |
| | | I _O = -20 μA; V _{CC} = 4.5 V | 4.4 | - | - | V |
| | | I _O = -20 μA; V _{CC} = 6.0 V | 5.9 | - | - | V |
| | | I _O = -6.0 mA; V _{CC} = 4.5 V | 3.84 | - | - | V |
| | | I _O = -7.8 mA; V _{CC} = 6.0 V | 5.34 | - | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | | | | |
| | | I _O = 20 μA; V _{CC} = 2.0 V | - | - | 0.1 | V |
| | | I _O = 20 μA; V _{CC} = 4.5 V | - | - | 0.1 | V |
| | | I _O = 20 μA; V _{CC} = 6.0 V | - | - | 0.1 | V |
| | | I _O = 6.0 mA; V _{CC} = 4.5 V | - | - | 0.33 | V |
| | | I _O = 7.8 mA; V _{CC} = 6.0 V | - | - | 0.33 | V |
| I _I | input leakage current | V _I = V _{CC} or GND; V _{CC} = 6.0 V | - | - | ±1.0 | μA |
| I _{OZ} | OFF-state output current | V _I = V _{IH} or V _{IL} ; V _{CC} = 6.0 V; V _O = V _{CC} or GND | - | - | ±5.0 | μA |
| I _{CC} | supply current | V _{CC} = 6.0 V; I _O = 0 A; V _I = V _{CC} or GND | | - | 80 | μA |
| T_{amb} = -40 °C to +125 °C | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 2.0 V | 1.5 | - | - | V |
| | | V _{CC} = 4.5 V | 3.15 | - | - | V |
| | | V _{CC} = 6.0 V | 4.2 | - | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 2.0 V | - | - | 0.5 | V |
| | | V _{CC} = 4.5 V | - | - | 1.35 | V |
| | | V _{CC} = 6.0 V | - | - | 1.8 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} | | | | |
| | | I _O = -20 μA; V _{CC} = 2.0 V | 1.9 | - | - | V |
| | | I _O = -20 μA; V _{CC} = 4.5 V | 4.4 | - | - | V |
| | | I _O = -20 μA; V _{CC} = 6.0 V | 5.9 | - | - | V |
| | | I _O = -6.0 mA; V _{CC} = 4.5 V | 3.7 | - | - | V |
| | | I _O = -7.8 mA; V _{CC} = 6.0 V | 5.2 | - | - | V |

Table 6. Static characteristics 74HC373 ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------|--------------------------|---|-----|-----|-------|------|
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | | | | |
| | | I _O = 20 μA; V _{CC} = 2.0 V | - | - | 0.1 | V |
| | | I _O = 20 μA; V _{CC} = 4.5 V | - | - | 0.1 | V |
| | | I _O = 20 μA; V _{CC} = 6.0 V | - | - | 0.1 | V |
| | | I _O = 6.0 mA; V _{CC} = 4.5 V | - | - | 0.4 | V |
| | | I _O = 7.8 mA; V _{CC} = 6.0 V | - | - | 0.4 | V |
| I _I | input leakage current | V _I = V _{CC} or GND; V _{CC} = 6.0 V | - | - | ±1.0 | μA |
| I _{OZ} | OFF-state output current | V _I = V _{IH} or V _{IL} ; V _{CC} = 6.0 V; V _O = V _{CC} or GND | - | - | ±10.0 | μA |
| I _{CC} | supply current | V _{CC} = 6.0 V; I _O = 0 A; V _I = V _{CC} or GND | - | - | 160 | μA |

Table 7. Static characteristics 74HCT373

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---------------------------|--|------|------|------|------|
| T_{amb} = 25 °C | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 4.5 V to 5.5 V | 2.0 | 1.6 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 4.5 V to 5.5 V | - | 1.2 | 0.8 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} | | | | |
| | | I _O = -20 μA; V _{CC} = 4.5 V | 4.4 | 4.5 | - | V |
| | | I _O = -6.0 mA; V _{CC} = 4.5 V | 3.98 | 4.32 | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | | | | |
| | | I _O = 20 μA; V _{CC} = 4.5 V | - | 0.0 | 0.1 | V |
| | | I _O = 6.0 mA; V _{CC} = 4.5 V | - | 0.16 | 0.26 | V |
| I _I | input leakage current | V _I = V _{CC} or GND; V _{CC} = 5.5 V | - | - | ±0.1 | μA |
| I _{OZ} | OFF-state output current | V _I = V _{IH} or V _{IL} ; V _{CC} = 5.5 V; V _O = V _{CC} or GND per input pin; other inputs at V _{CC} or GND; I _O = 0 A | - | - | ±0.5 | μA |
| I _{CC} | supply current | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V | - | - | 8.0 | μA |
| ΔI _{CC} | additional supply current | V _I = V _{CC} - 2.1 V; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V; I _O = 0 A | | | | |
| | | Dn | - | 30 | 108 | μA |
| | | LE | - | 150 | 540 | μA |
| | | $\overline{\text{OE}}$ | - | 100 | 360 | μA |
| C _I | input capacitance | | - | 3.5 | - | pF |
| T_{amb} = -40 °C to +85 °C | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 4.5 V to 5.5 V | 2.0 | - | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 4.5 V to 5.5 V | - | - | 0.8 | V |

Table 7. Static characteristics 74HCT373 ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|---------------------------|--|------|-----|------|------|
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} | | | | |
| | | I _O = -20 μA; V _{CC} = 4.5 V | 4.4 | - | - | V |
| | | I _O = -6.0 μA; V _{CC} = 4.5 V | 3.84 | - | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | | | | |
| | | I _O = 20 μA; V _{CC} = 4.5 V | - | - | 0.1 | V |
| | | I _O = 6.0 mA; V _{CC} = 4.5 V | - | - | 0.33 | V |
| I _I | input leakage current | V _I = V _{CC} or GND; V _{CC} = 5.5 V | - | - | ±1.0 | μA |
| I _{OZ} | OFF-state output current | V _I = V _{IH} or V _{IL} ; V _{CC} = 5.5 V; V _O = V _{CC} or GND per input pin; other inputs at V _{CC} or GND; I _O = 0 A | - | - | ±5.0 | μA |
| I _{CC} | supply current | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V | - | - | 80 | μA |
| ΔI _{CC} | additional supply current | V _I = V _{CC} - 2.1 V; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V; I _O = 0 A | | | | |
| | | Dn | - | - | 135 | μA |
| | | LE | - | - | 675 | μA |
| | | $\overline{\text{OE}}$ | - | - | 450 | μA |
| T_{amb} = -40 °C to +125 °C | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 4.5 V to 5.5 V | 2.0 | - | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 4.5 V to 5.5 V | - | - | 0.8 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} | | | | |
| | | I _O = -20 μA; V _{CC} = 4.5 V | 4.4 | - | - | V |
| | | I _O = -6.0 mA; V _{CC} = 4.5 V | 3.7 | - | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | | | | |
| | | I _O = 20 μA; V _{CC} = 4.5 V | - | - | 0.1 | V |
| | | I _O = 6.0 mA; V _{CC} = 4.5 V | - | - | 0.4 | V |
| I _I | input leakage current | V _I = V _{CC} or GND; V _{CC} = 5.5 V | - | - | ±1.0 | μA |
| I _{OZ} | OFF-state output current | V _I = V _{IH} or V _{IL} ; V _{CC} = 5.5 V; V _O = V _{CC} or GND per input pin; other inputs at V _{CC} or GND; I _O = 0 A | - | - | ±10 | μA |
| I _{CC} | supply current | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V | - | - | 160 | μA |
| ΔI _{CC} | additional supply current | V _I = V _{CC} - 2.1 V; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V; I _O = 0 A | | | | |
| | | Dn | - | - | 147 | μA |
| | | LE | - | - | 735 | μA |
| | | $\overline{\text{OE}}$ | - | - | 490 | μA |

10. Dynamic characteristics

Table 8. Dynamic characteristics 74HC373

Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit see [Figure 12](#).

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit | |
|-------------------------------------|-------------------------------|---|-----|-----|-----|------|----|
| $T_{amb} = 25$ °C | | | | | | | |
| t_{pd} | propagation delay | Dn to Qn; see Figure 8 | [1] | | | | |
| | | $V_{CC} = 2.0$ V | - | 41 | 150 | ns | |
| | | $V_{CC} = 4.5$ V | - | 15 | 30 | ns | |
| | | $V_{CC} = 5$ V; $C_L = 15$ pF | - | 12 | - | ns | |
| | | $V_{CC} = 6.0$ V | - | 12 | 26 | ns | |
| | | LE to Qn; see Figure 9 | | | | | |
| | | $V_{CC} = 2.0$ V | - | 50 | 175 | ns | |
| | | $V_{CC} = 4.5$ V | - | 18 | 35 | ns | |
| | | $V_{CC} = 5$ V; $C_L = 15$ pF | - | 15 | - | ns | |
| $V_{CC} = 6.0$ V | - | 14 | 30 | ns | | | |
| t_{en} | enable time | \overline{OE} to Qn; see Figure 10 | [2] | | | | |
| | | $V_{CC} = 2.0$ V | - | 44 | 150 | ns | |
| | | $V_{CC} = 4.5$ V | - | 16 | 30 | ns | |
| | | $V_{CC} = 6.0$ V | - | 13 | 26 | ns | |
| t_{dis} | disable time | \overline{OE} to Qn; see Figure 10 | [3] | | | | |
| | | $V_{CC} = 2.0$ V | - | 47 | 150 | ns | |
| | | $V_{CC} = 4.5$ V | - | 17 | 30 | ns | |
| | | $V_{CC} = 6.0$ V | - | 14 | 26 | ns | |
| t_t | transition time | Qn; see Figure 8 and Figure 9 | [4] | | | | |
| | | $V_{CC} = 2.0$ V | - | 14 | 60 | ns | |
| | | $V_{CC} = 4.5$ V | - | 5 | 12 | ns | |
| | | $V_{CC} = 6.0$ V | - | 4 | 10 | ns | |
| t_W | pulse width | LE HIGH; see Figure 9 | | | | | |
| | | $V_{CC} = 2.0$ V | 80 | 17 | - | ns | |
| | | $V_{CC} = 4.5$ V | 16 | 6 | - | ns | |
| | | $V_{CC} = 6.0$ V | 14 | 5 | - | ns | |
| t_{su} | set-up time | Dn to LE; see Figure 11 | | | | | |
| | | $V_{CC} = 2.0$ V | 50 | 14 | - | ns | |
| | | $V_{CC} = 4.5$ V | 10 | 5 | - | ns | |
| | | $V_{CC} = 6.0$ V | 9 | 4 | - | ns | |
| t_h | hold time | Dn to LE; see Figure 11 | | | | | |
| | | $V_{CC} = 2.0$ V | +5 | -8 | - | ns | |
| | | $V_{CC} = 4.5$ V | +5 | -3 | - | ns | |
| | | $V_{CC} = 6.0$ V | +5 | -2 | - | ns | |
| C_{PD} | power dissipation capacitance | per latch; $V_I = GND$ to V_{CC} | [5] | - | 45 | - | pF |

Table 8. Dynamic characteristics 74HC373 ...continued

Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit see [Figure 12](#).

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|-------------------|---|---------------------|--|---------------------|------|
| $T_{amb} = -40$ °C to $+85$ °C | | | | | | |
| t_{pd} | propagation delay | Dn to Qn; see Figure 8 | [1] | | | |
| | | $V_{CC} = 2.0$ V | - | - | 190 | ns |
| | | $V_{CC} = 4.5$ V | - | - | 38 | ns |
| | | $V_{CC} = 6.0$ V | - | - | 33 | ns |
| | | LE to Qn; see Figure 9 | | | | |
| | | $V_{CC} = 2.0$ V | - | - | 220 | ns |
| | | $V_{CC} = 4.5$ V | - | - | 44 | ns |
| | | $V_{CC} = 6.0$ V | - | - | 37 | ns |
| | | t_{en} | enable time | \overline{OE} to Qn; see Figure 10 | [2] | |
| $V_{CC} = 2.0$ V | - | | | - | 190 | ns |
| $V_{CC} = 4.5$ V | - | | | - | 38 | ns |
| $V_{CC} = 6.0$ V | - | | | - | 33 | ns |
| t_{dis} | disable time | \overline{OE} to Qn; see Figure 10 | [3] | | | |
| | | $V_{CC} = 2.0$ V | - | - | 190 | ns |
| | | $V_{CC} = 4.5$ V | - | - | 38 | ns |
| | | $V_{CC} = 6.0$ V | - | - | 33 | ns |
| t_t | transition time | Qn; see Figure 8 and Figure 9 | [4] | | | |
| | | $V_{CC} = 2.0$ V | - | - | 75 | ns |
| | | $V_{CC} = 4.5$ V | - | - | 15 | ns |
| | | $V_{CC} = 6.0$ V | - | - | 13 | ns |
| t_W | pulse width | LE HIGH; see Figure 9 | | | | |
| | | $V_{CC} = 2.0$ V | 100 | - | - | ns |
| | | $V_{CC} = 4.5$ V | 20 | - | - | ns |
| | | $V_{CC} = 6.0$ V | 17 | - | - | ns |
| t_{su} | set-up time | Dn to LE; see Figure 11 | | | | |
| | | $V_{CC} = 2.0$ V | 65 | - | - | ns |
| | | $V_{CC} = 4.5$ V | 13 | - | - | ns |
| | | $V_{CC} = 6.0$ V | 11 | - | - | ns |
| t_h | hold time | Dn to LE; see Figure 11 | | | | |
| | | $V_{CC} = 2.0$ V | 5 | - | - | ns |
| | | $V_{CC} = 4.5$ V | 5 | - | - | ns |
| | | $V_{CC} = 6.0$ V | 5 | - | - | ns |

Table 8. Dynamic characteristics 74HC373 ...continued

Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit see [Figure 12](#).

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|-------------------|---|-------------|--|-----|------|
| $T_{amb} = -40$ °C to $+125$ °C | | | | | | |
| t_{pd} | propagation delay | Dn to Qn; see Figure 8 | | [1] | | |
| | | $V_{CC} = 2.0$ V | - | - | 225 | ns |
| | | $V_{CC} = 4.5$ V | - | - | 45 | ns |
| | | $V_{CC} = 6.0$ V | - | - | 38 | ns |
| | | LE to Qn; see Figure 9 | | | | |
| | | $V_{CC} = 2.0$ V | - | - | 265 | ns |
| | | $V_{CC} = 4.5$ V | - | - | 53 | ns |
| | | $V_{CC} = 6.0$ V | - | - | 45 | ns |
| | | t_{en} | enable time | \overline{OE} to Qn; see Figure 10 | | [2] |
| $V_{CC} = 2.0$ V | - | | | - | 225 | ns |
| $V_{CC} = 4.5$ V | - | | | - | 45 | ns |
| $V_{CC} = 6.0$ V | - | | | - | 38 | ns |
| t_{dis} | disable time | \overline{OE} to Qn; see Figure 10 | | [3] | | |
| | | $V_{CC} = 2.0$ V | - | - | 225 | ns |
| | | $V_{CC} = 4.5$ V | - | - | 45 | ns |
| | | $V_{CC} = 6.0$ V | - | - | 38 | ns |
| t_t | transition time | Qn; see Figure 8 and Figure 9 | | [4] | | |
| | | $V_{CC} = 2.0$ V | - | - | 90 | ns |
| | | $V_{CC} = 4.5$ V | - | - | 18 | ns |
| | | $V_{CC} = 6.0$ V | - | - | 15 | ns |
| t_W | pulse width | LE HIGH; see Figure 9 | | | | |
| | | $V_{CC} = 2.0$ V | 120 | - | - | ns |
| | | $V_{CC} = 4.5$ V | 24 | - | - | ns |
| | | $V_{CC} = 6.0$ V | 20 | - | - | ns |
| t_{su} | set-up time | Dn to LE; see Figure 11 | | | | |
| | | $V_{CC} = 2.0$ V | 75 | - | - | ns |
| | | $V_{CC} = 4.5$ V | 15 | - | - | ns |
| | | $V_{CC} = 6.0$ V | 13 | - | - | ns |

Table 8. Dynamic characteristics 74HC373 ...continued

Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit see [Figure 12](#).

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|-----------|---|-----|-----|-----|------|
| t_h | hold time | Dn to LE; see Figure 11 | | | | |
| | | $V_{CC} = 2.0$ V | 5 | - | - | ns |
| | | $V_{CC} = 4.5$ V | 5 | - | - | ns |
| | | $V_{CC} = 6.0$ V | 5 | - | - | ns |

- [1] t_{pd} is the same as t_{PLH} and t_{PHL} .
- [2] t_{en} is the same as t_{PZH} and t_{PZL} .
- [3] t_{dis} is the same as t_{PLZ} and t_{PHZ} .
- [4] t_t is the same as t_{THL} and t_{TLH} .
- [5] C_{PD} is used to determine the dynamic power dissipation (P_D in μ W).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in V;
 N = number of inputs switching;
 $\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

Table 9. Dynamic characteristics 74HCT373

Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit see [Figure 12](#).

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit | |
|-------------------------------------|-------------------------------|---|-----|-----|-----|------|----|
| $T_{amb} = 25$ °C | | | | | | | |
| t_{pd} | propagation delay | Dn to Qn; see Figure 8 | | [1] | | | |
| | | $V_{CC} = 4.5$ V | - | 17 | 30 | ns | |
| | | $V_{CC} = 5$ V; $C_L = 15$ pF | - | 14 | - | ns | |
| | | LE to Qn; see Figure 9 | | | | | |
| | | $V_{CC} = 4.5$ V | - | 16 | 32 | ns | |
| | | $V_{CC} = 5$ V; $C_L = 15$ pF | - | 13 | - | ns | |
| t_{en} | enable time | \overline{OE} to Qn; see Figure 10 | | [2] | | | |
| | | $V_{CC} = 4.5$ V | - | 19 | 32 | ns | |
| t_{dis} | disable time | \overline{OE} to Qn; see Figure 10 | | [3] | | | |
| | | $V_{CC} = 4.5$ V | - | 18 | 30 | ns | |
| t_t | transition time | Qn; see Figure 8 and Figure 9 | | [4] | | | |
| | | $V_{CC} = 4.5$ V | - | 5 | 12 | ns | |
| t_W | pulse width | LE HIGH; see Figure 9 | | | | | |
| | | $V_{CC} = 4.5$ V | 16 | 4 | - | ns | |
| t_{su} | set-up time | Dn to LE; see Figure 11 | | | | | |
| | | $V_{CC} = 4.5$ V | 12 | 6 | - | ns | |
| t_h | hold time | Dn to LE; see Figure 11 | | | | | |
| | | $V_{CC} = 4.5$ V | 4 | -1 | - | ns | |
| C_{PD} | power dissipation capacitance | per latch; $V_1 = GND$ to $(V_{CC} - 1.5$ V) | [5] | - | 41 | - | pF |

Table 9. Dynamic characteristics 74HCT373 ...continued

Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit see [Figure 12](#).

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|----------------------|---|-----|-----|-----|------|
| $T_{amb} = -40$ °C to $+85$ °C | | | | | | |
| t_{pd} | propagation delay | Dn to Qn; see Figure 8 | [1] | | | |
| | | $V_{CC} = 4.5$ V | - | - | 38 | ns |
| | | LE to Qn; see Figure 9 | | | | |
| | | $V_{CC} = 4.5$ V | - | - | 40 | ns |
| t_{en} | enable time | \overline{OE} to Qn; see Figure 10 | [2] | | | |
| | | $V_{CC} = 4.5$ V | - | - | 40 | ns |
| t_{dis} | disable time | \overline{OE} to Qn; see Figure 10 | [3] | | | |
| | | $V_{CC} = 4.5$ V | - | - | 38 | ns |
| t_t | transition time | Qn; see Figure 8 and Figure 9 | [4] | | | |
| | | $V_{CC} = 4.5$ V | - | - | 15 | ns |
| t_W | pulse width | LE HIGH; see Figure 9 | | | | |
| | | $V_{CC} = 4.5$ V | 20 | - | - | ns |
| t_{su} | set-up time | Dn to LE; see Figure 11 | | | | |
| | | $V_{CC} = 4.5$ V | 15 | - | - | ns |
| t_h | hold time | Dn to LE; see Figure 11 | | | | |
| | | $V_{CC} = 4.5$ V | 4 | - | - | ns |
| $T_{amb} = -40$ °C to $+125$ °C | | | | | | |
| t_{pd} | propagation delay | Dn to Qn; see Figure 8 | [1] | | | |
| | | $V_{CC} = 4.5$ V | - | - | 45 | ns |
| | | LE to Qn; see Figure 9 | | | | |
| | | $V_{CC} = 4.5$ V | - | - | 48 | ns |
| t_{en} | enable time | \overline{OE} to Qn; see Figure 10 | [2] | | | |
| | | $V_{CC} = 4.5$ V | - | - | 48 | ns |
| t_{dis} | disable time | \overline{OE} to Qn; see Figure 10 | [3] | | | |
| | | $V_{CC} = 4.5$ V | - | - | 45 | ns |
| t_t | transition time | Qn; see Figure 8 and Figure 9 | [4] | | | |
| | | $V_{CC} = 4.5$ V | - | - | 18 | ns |
| t_W | pulse width | LE HIGH; see Figure 9 | | | | |
| | | $V_{CC} = 4.5$ V | 24 | - | - | ns |
| t_{su} | set-up time Dn to LE | Dn to LE; see Figure 11 | | | | |
| | | $V_{CC} = 4.5$ V | 18 | - | - | ns |

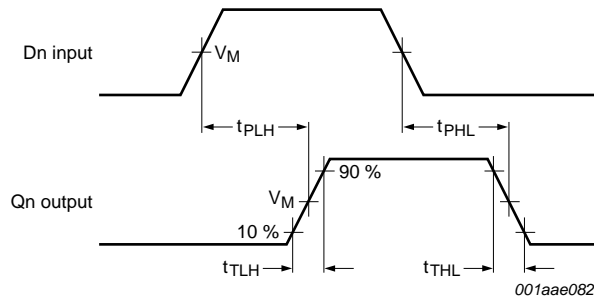
Table 9. Dynamic characteristics 74HCT373 ...continued

Voltages are referenced to GND (ground = 0 V); $C_L = 50 \text{ pF}$ unless otherwise specified; for test circuit see [Figure 12](#).

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|--------------------|---|-----|-----|-----|------|
| t_h | hold time Dn to LE | Dn to LE; see Figure 11 $V_{CC} = 4.5 \text{ V}$ | 4 | - | - | ns |

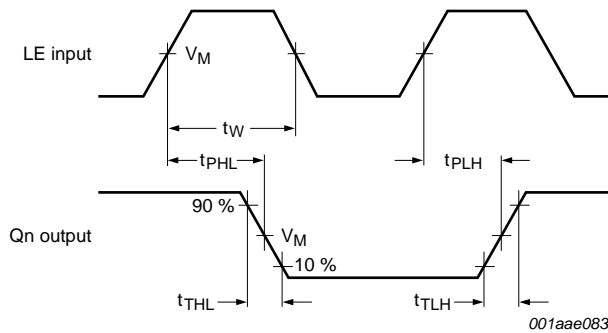
- [1] t_{pd} is the same as t_{PLH} and t_{PHL} .
- [2] t_{en} is the same as t_{PZH} and t_{PZL} .
- [3] t_{dis} is the same as t_{PLZ} and t_{PHZ} .
- [4] t_i is the same as t_{THL} and t_{TLH} .
- [5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in V;
 N = number of inputs switching;
 $\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

11. Waveforms



Measurement points are given in [Table 10](#).

Fig 8. Propagation delay input (Dn) to output (Qn) and transition time output (Qn)



Measurement points are given in [Table 10](#).

Fig 9. Pulse width latch enable input (LE), propagation delay (LE) to output (Qn) and transition time output (Qn)

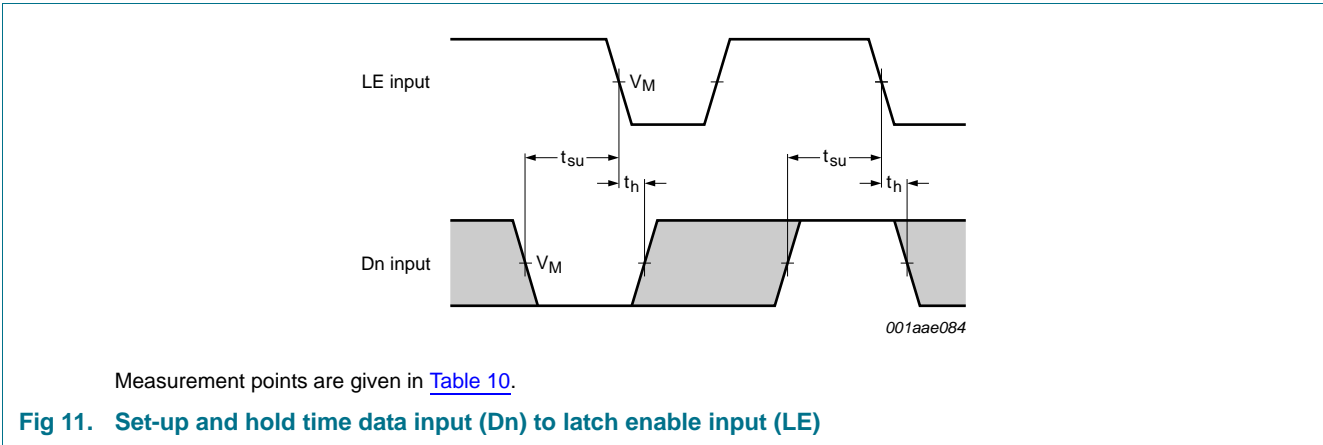
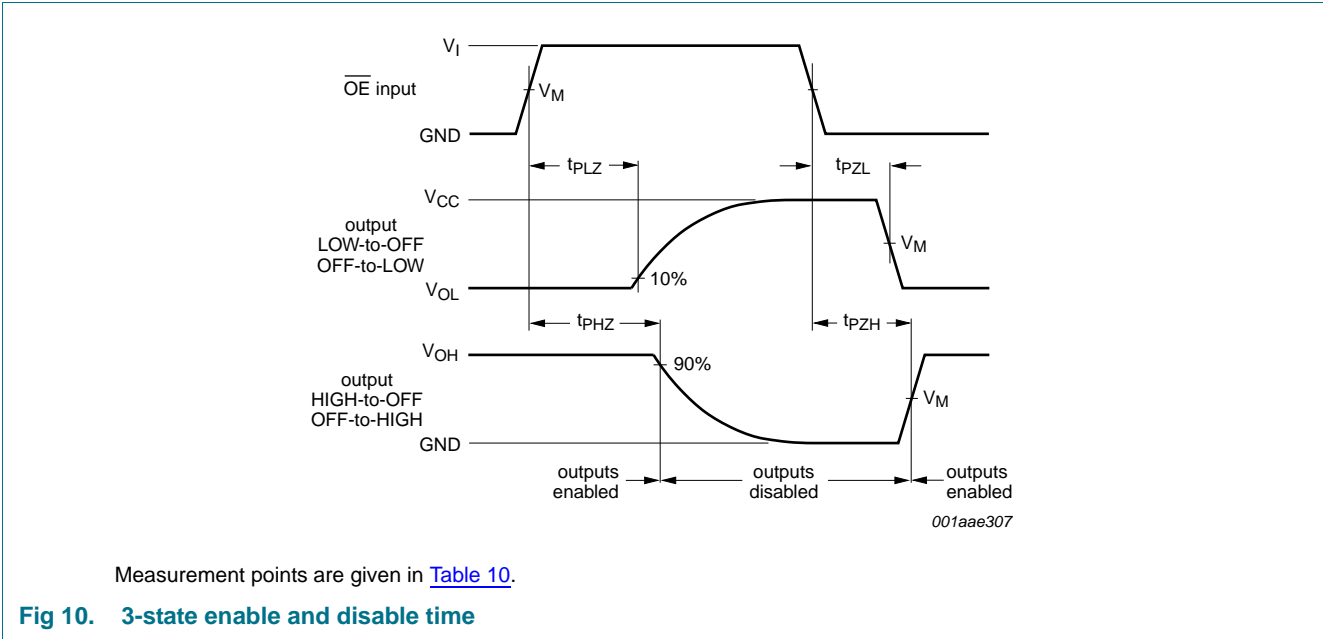


Table 10. Measurement points

| Type | Input | Output |
|----------|-------------|-------------|
| | V_M | V_M |
| 74HC373 | $0.5V_{CC}$ | $0.5V_{CC}$ |
| 74HCT373 | 1.3 V | 1.3 V |

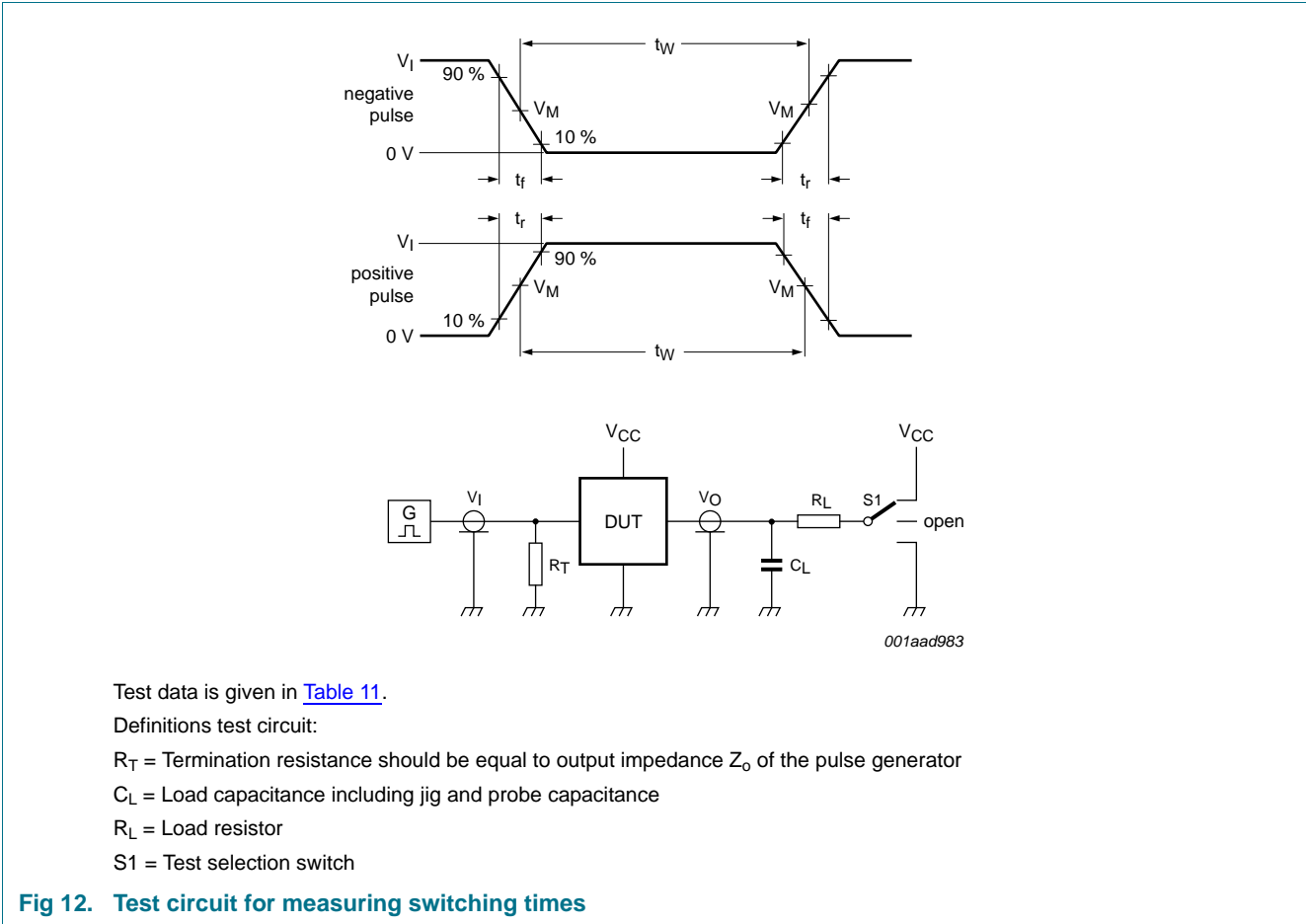


Fig 12. Test circuit for measuring switching times

Table 11. Test data

| Type | Input | | Load | | S1 position | | |
|----------|----------|------------|--------------|--------------|--------------------|--------------------|--------------------|
| | V_I | t_r, t_f | C_L | R_L | t_{PHL}, t_{PLH} | t_{PZH}, t_{PHZ} | t_{PZL}, t_{PLZ} |
| 74HC373 | V_{CC} | 6 ns | 15 pF, 50 pF | 1 k Ω | open | GND | V_{CC} |
| 74HCT373 | 3 V | 6 ns | 15 pF, 50 pF | 1 k Ω | open | GND | V_{CC} |

12. Package outline

DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1

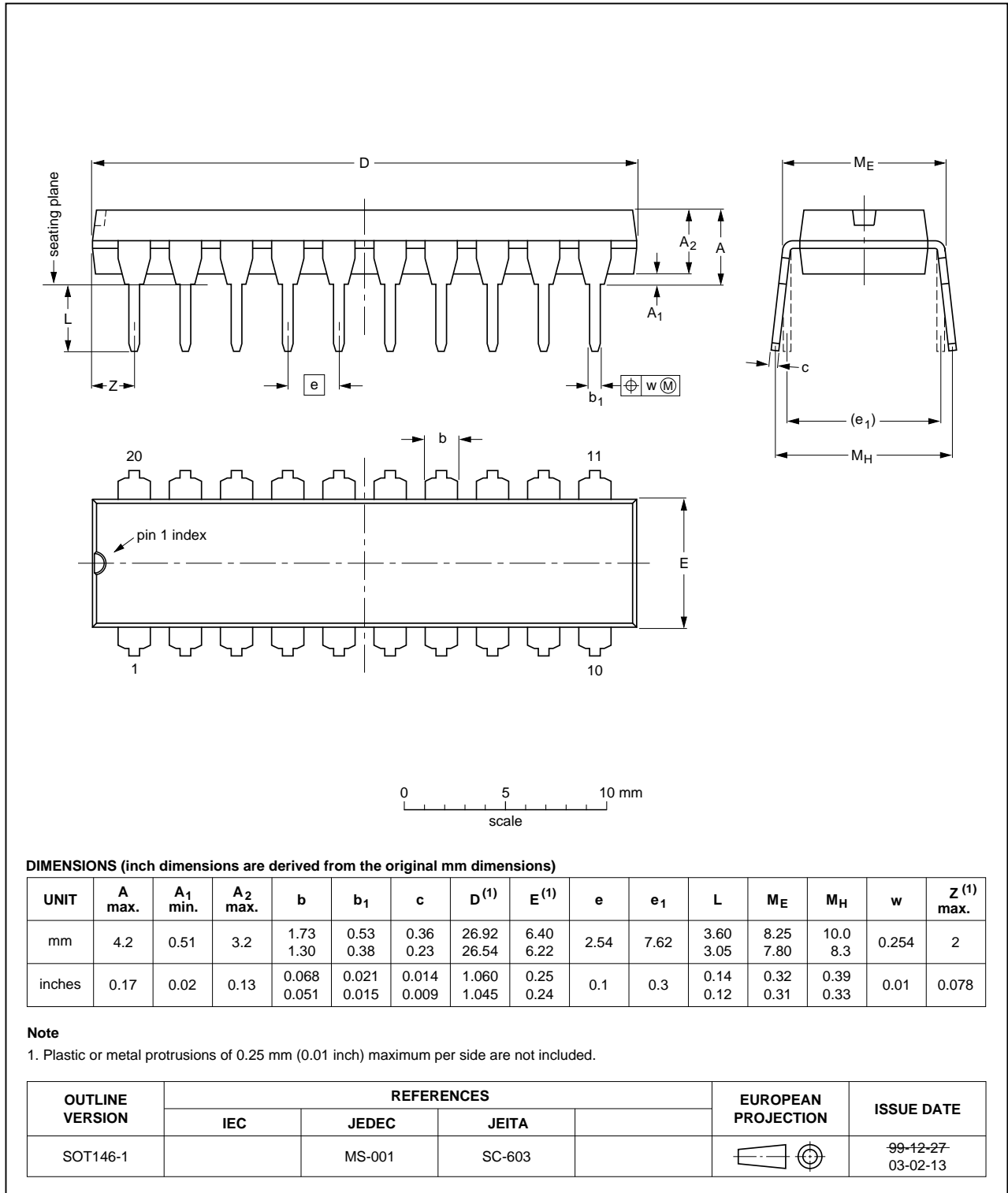


Fig 13. Package outline SOT146-1 (DIP20)

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

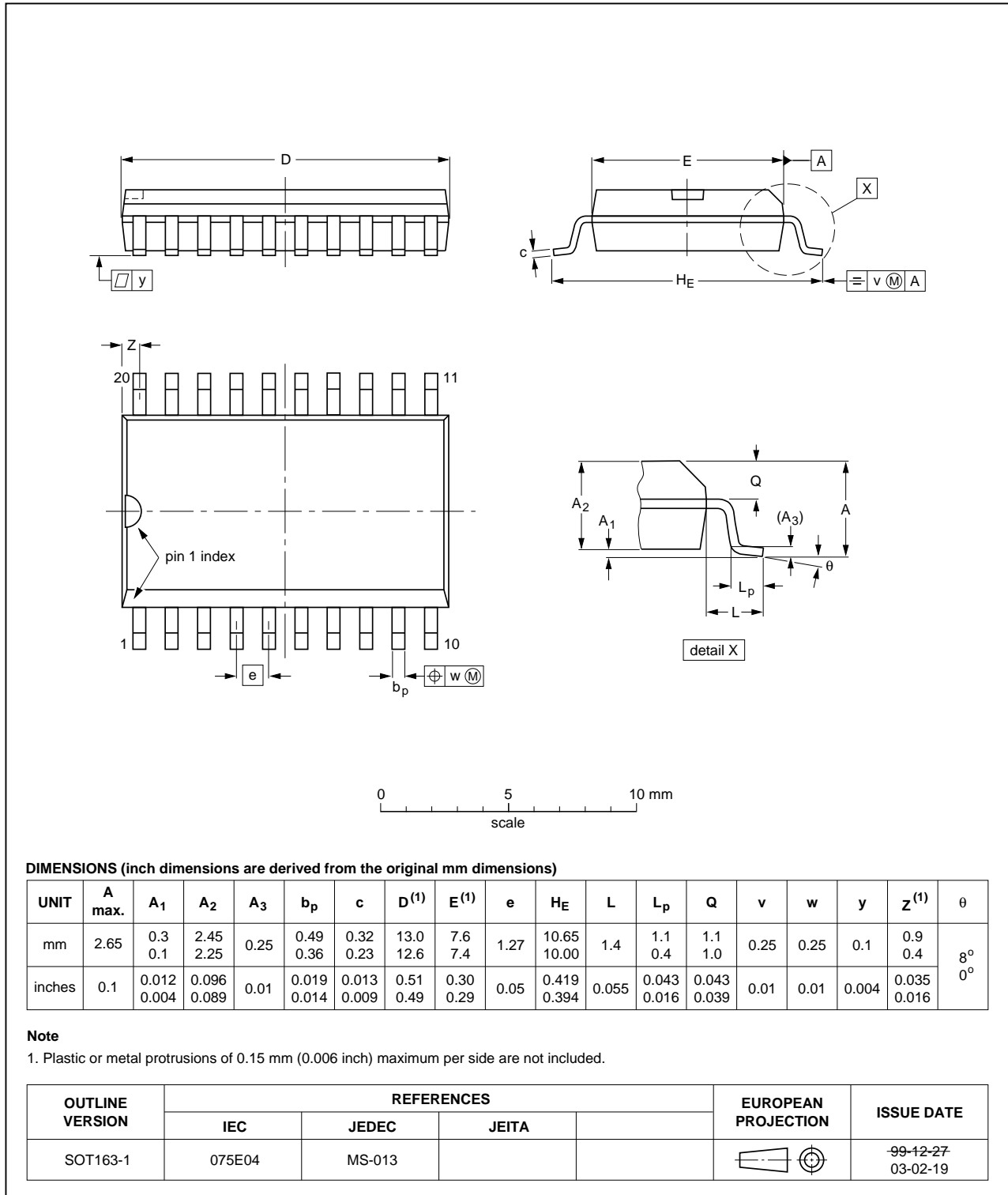


Fig 14. Package outline SOT163-1 (SO20)

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1

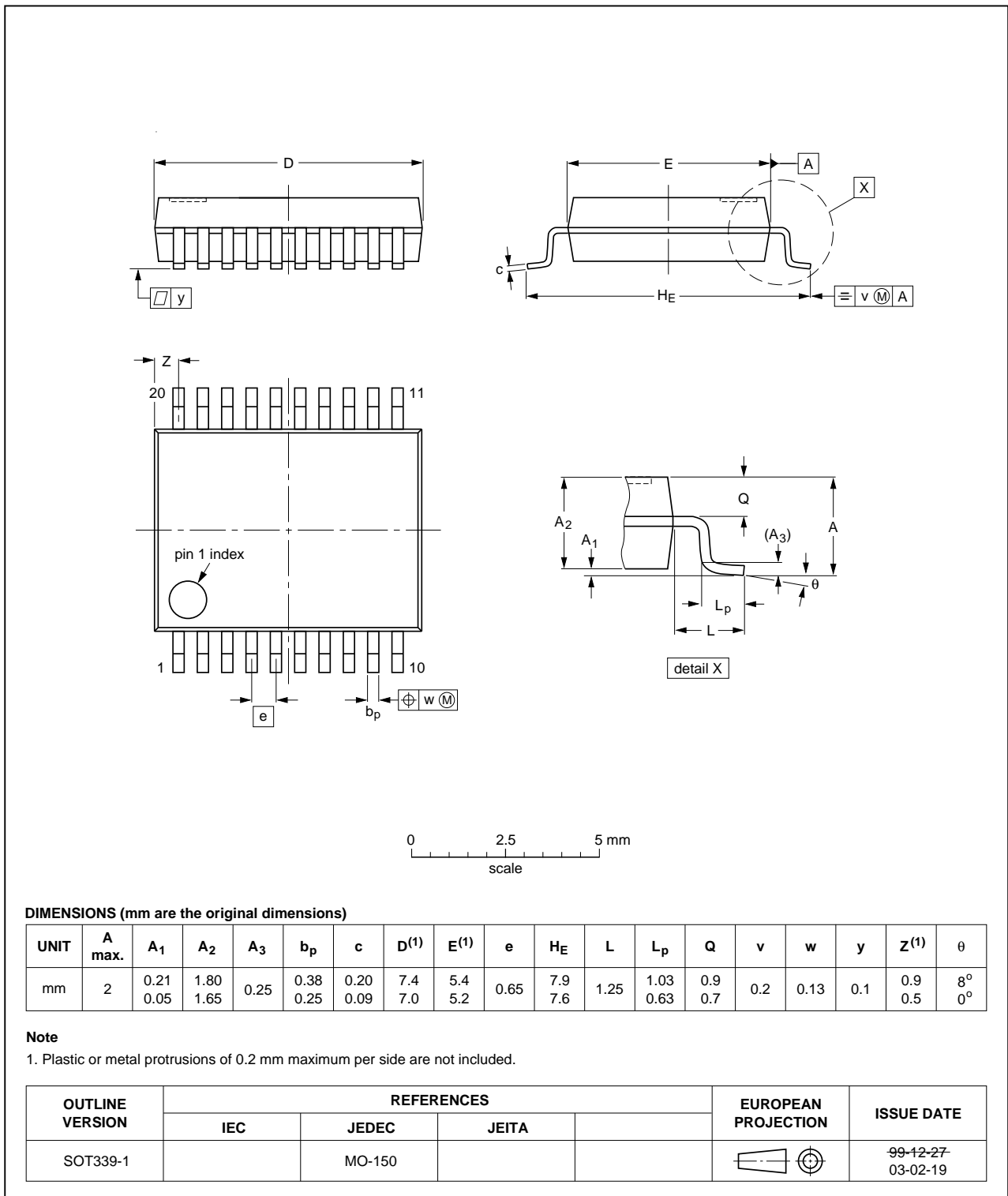


Fig 15. Package outline SOT339-1 (SSOP20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

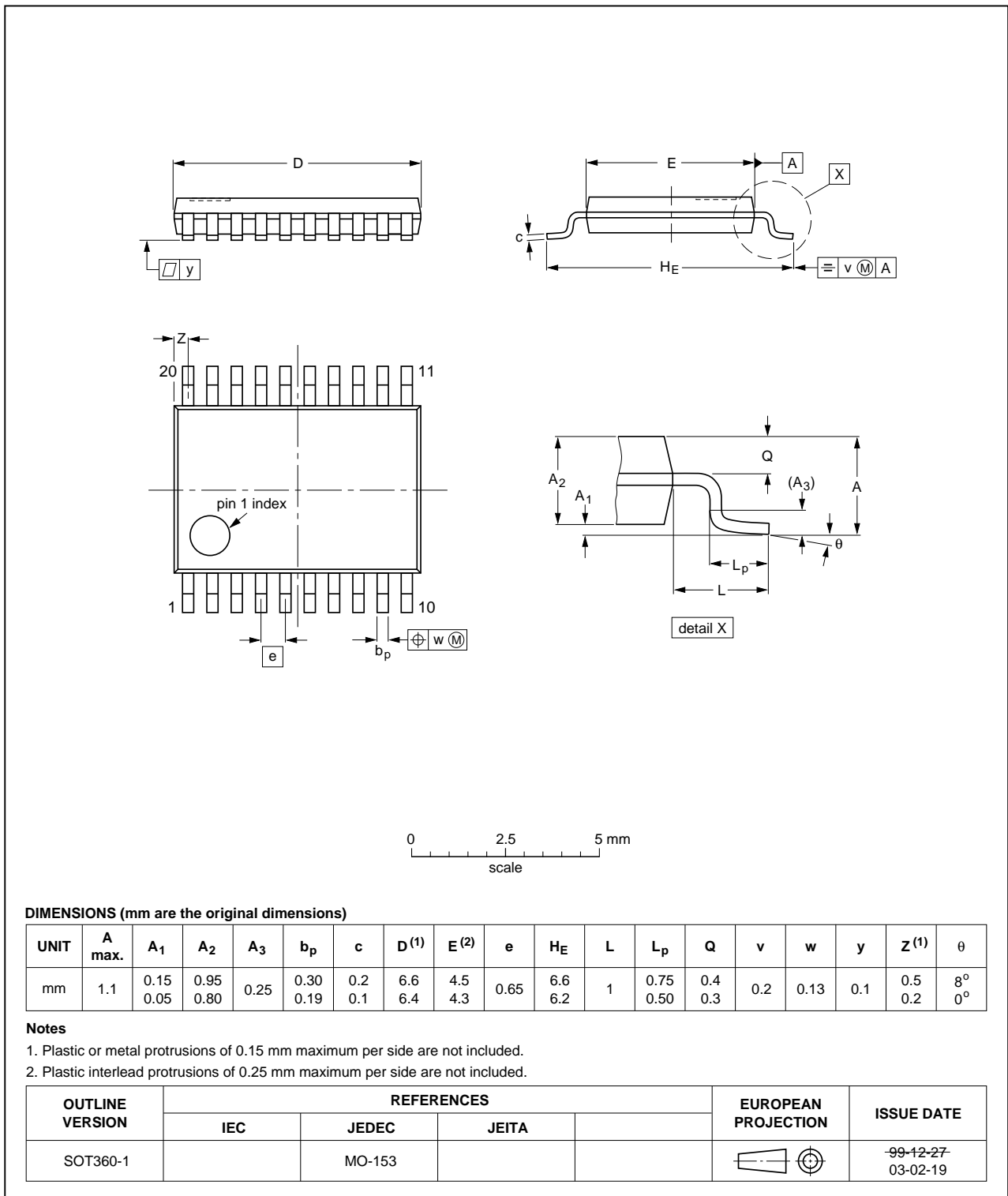


Fig 16. Package outline SOT360-1 (TSSOP20)

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm

SOT764-1

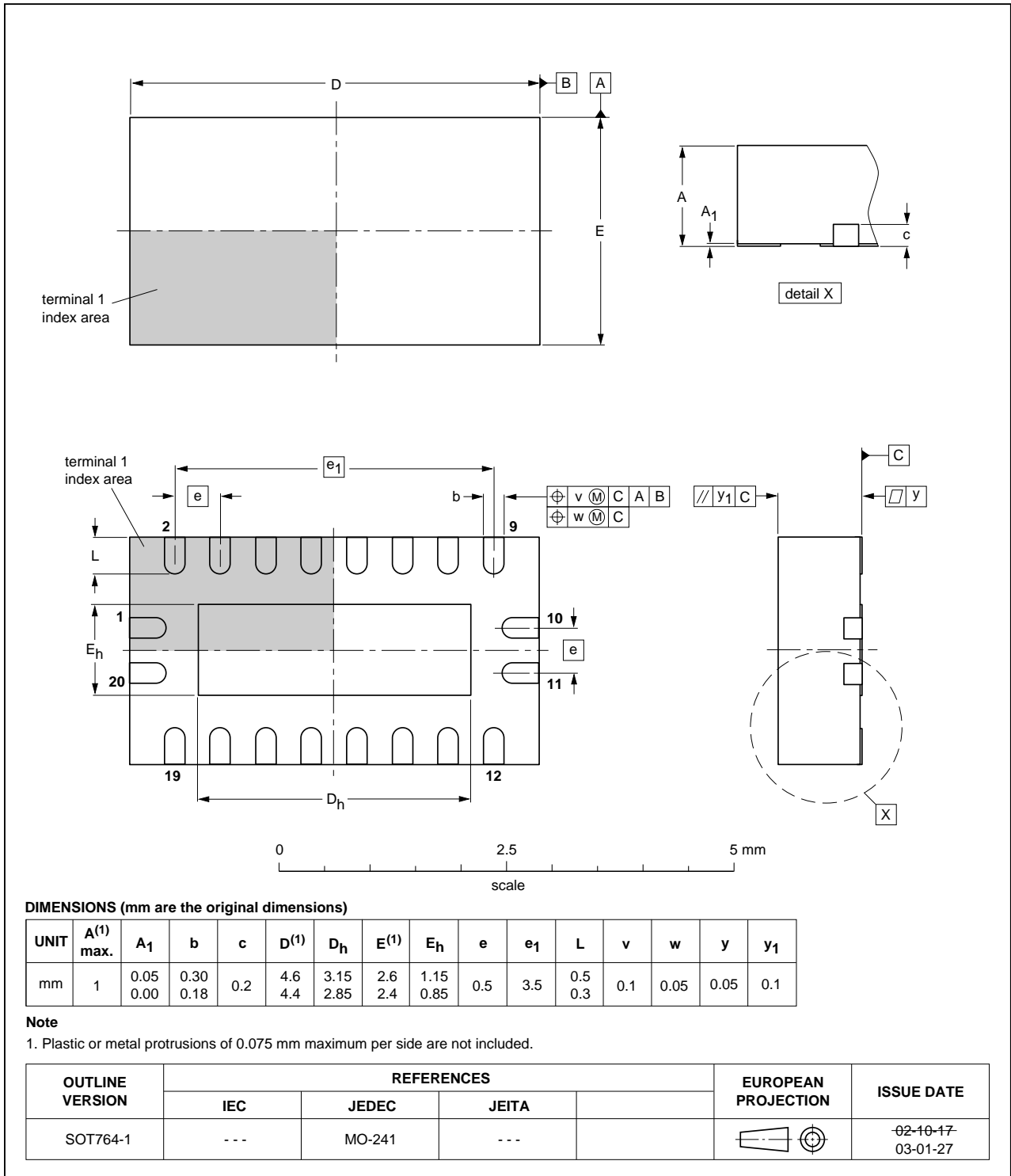


Fig 17. Package outline SOT764-1 (DHVQFN20)

13. Abbreviations

Table 12. Abbreviations

| Acronym | Description |
|---------|---|
| CMOS | Complementary Metal Oxide Semiconductor |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

14. Revision history

Table 13. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---------------------|--|-----------------------|---------------|---------------------|
| 74HC_HCT373 v.5 | 20111213 | Product data sheet | - | 74HC_HCT373 v.4 |
| Modifications: | <ul style="list-style-type: none"> Legal pages updated. | | | |
| 74HC_HCT373 v.4 | 20100903 | Product data sheet | - | 74HC_HCT373 v.3 |
| 74HC_HCT373 v.3 | 20060120 | Product data sheet | - | 74HC_HCT373_CNV v.2 |
| 74HC_HCT373_CNV v.2 | 19970827 | Product specification | - | - |

15. Legal information

15.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

15.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

15.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or

malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond

NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

15.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

16. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

17. Contents

| | | |
|-----------|---|-----------|
| 1 | General description | 1 |
| 2 | Features and benefits | 1 |
| 3 | Ordering information | 2 |
| 4 | Functional diagram | 2 |
| 5 | Pinning information | 4 |
| 5.1 | Pinning | 4 |
| 5.2 | Pin description | 4 |
| 6 | Functional description | 5 |
| 6.1 | Function table | 5 |
| 7 | Limiting values | 5 |
| 8 | Recommended operating conditions | 6 |
| 9 | Static characteristics | 6 |
| 10 | Dynamic characteristics | 10 |
| 11 | Waveforms | 15 |
| 12 | Package outline | 18 |
| 13 | Abbreviations | 23 |
| 14 | Revision history | 23 |
| 15 | Legal information | 24 |
| 15.1 | Data sheet status | 24 |
| 15.2 | Definitions | 24 |
| 15.3 | Disclaimers | 24 |
| 15.4 | Trademarks | 25 |
| 16 | Contact information | 25 |
| 17 | Contents | 26 |

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2011.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 13 December 2011

Document identifier: 74HC_HCT373