74HC540-Q100; 74HCT540-Q100

Octal buffer/line driver; 3-state; inverting

Rev. 2 — 1 March 2016

Product data sheet

1. General description

The 74HC540-Q100; 74HCT540-Q100 is an 8-bit inverting buffer/line driver with 3-state outputs. The device features two output enables ($\overline{\text{OE}}1$ and $\overline{\text{OE}}2$). A HIGH on $\overline{\text{OE}}n$ causes the outputs to assume a high-impedance OFF-state. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - ◆ Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Inverting outputs
- Complies with JEDEC standard no. 7A
- Input levels:
 - ◆ For 74HC540-Q100: CMOS level
 - ◆ For 74HCT540-Q100: TTL level
- ESD protection:
 - MIL-STD-883, method 3015 exceeds 2000 V
 - ♦ HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0 Ω)

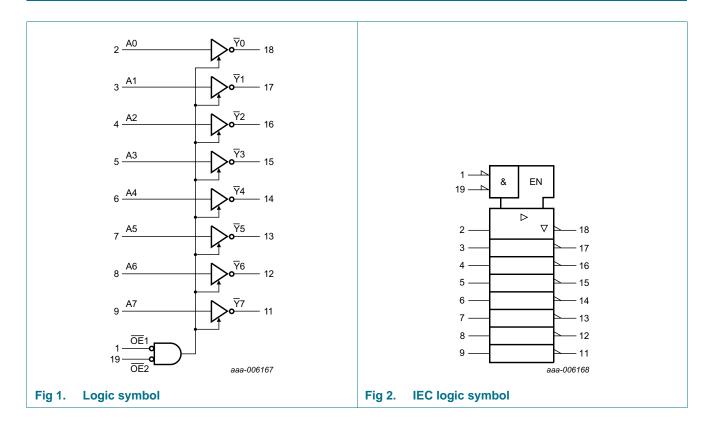
3. Ordering information

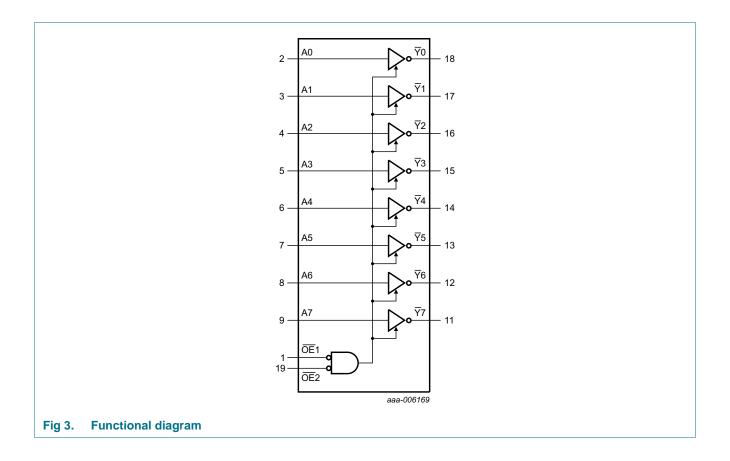
Table 1. Ordering information

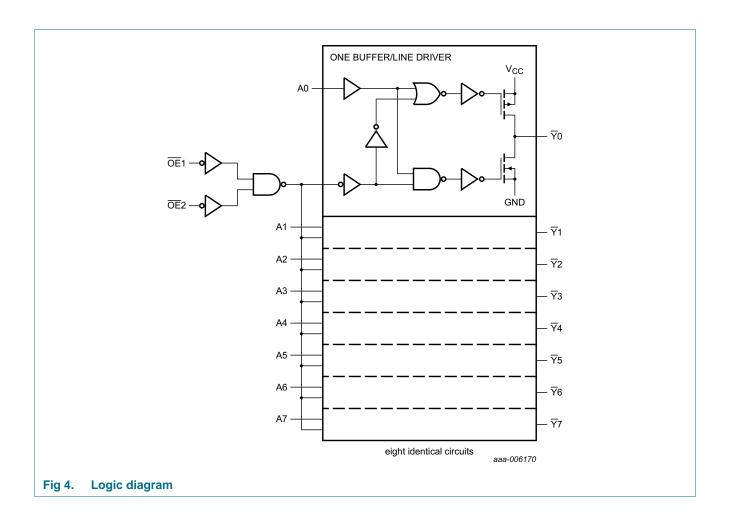
Type number	Package	Package									
	Temperature range	Name	Description	Version							
74HC540D-Q100	-40 °C to +125 °C	SO20	plastic small outline package; 20 leads;	SOT163-1							
74HCT540D-Q100			body width 7.5 mm								



4. Functional diagram

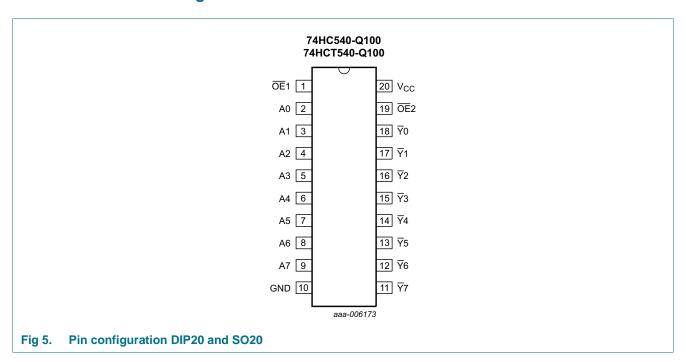






5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Pin	Description
1	output enable input (active LOW)
2, 3, 4, 5, 6, 7, 8, 9	data input
10	ground (0 V)
18, 17, 16, 15, 14, 13, 12, 11	data output
19	output enable input (active LOW)
20	supply voltage
	1 2, 3, 4, 5, 6, 7, 8, 9 10 18, 17, 16, 15, 14, 13, 12, 11 19

6. Functional description

Table 3. Functional table[1]

Control		Input	Output
OE1	OE2	An	Ϋ́n
L	L	L	Н
L	L	Н	L
X	Н	X	Z
Н	X	X	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

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7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{CC}	supply voltage			-0.5	+7	V
I _{IK}	input clamping current	$V_I < -0.5 \text{ V or } V_I > V_{CC} + 0.5 \text{ V}$	<u>[1]</u>	-	±20	mA
I _{OK}	output clamping current	$V_O < -0.5 \text{ V or } V_O > V_{CC} + 0.5 \text{ V}$	<u>[1]</u>	-	±20	mA
Io	output current	$-0.5 \text{ V} < \text{V}_{\text{O}} < \text{V}_{\text{CC}} + 0.5 \text{ V}$		-	±35	mA
I _{CC}	supply current			-	70	mA
I _{GND}	ground current			-70	-	mA
T _{stg}	storage temperature			-65	+150	°C
P _{tot}	total power dissipation	SO20	[2]	-	500	mW

^[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74H	74HC540-Q100		74HCT540-Q100			Unit
			Min	Тур	Max	Min	Тур	Max	
V _{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
VI	input voltage		0	-	V _{CC}	0	-	V _{CC}	V
Vo	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V _{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V _{CC} = 6.0 V	-	-	83	-	-	-	ns/V

^[2] For SO20 packages: above 70 °C the value of Ptot derates linearly with 8 mW/K.

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Tar	_{nb} = 25	°C		: –40 °C 85 °C		= –40 °C 125 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	
74HC54	0-Q100									
V _{IH}	HIGH-level	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
	input voltage	V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V _{IL}	LOW-level	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
	input voltage	V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V _{OH}	HIGH-level	$V_I = V_{IH}$ or V_{IL}								
	output voltage	$I_{O} = -20 \mu A; V_{CC} = 2.0 V$	1.9	2.0	-	1.9	-	1.9	-	V
		$I_{O} = -20 \mu A; V_{CC} = 4.5 V$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_{O} = -20 \mu A; V_{CC} = 6.0 V$	5.9	6.0	-	5.9	-	5.9	-	V
		$I_{O} = -6.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	3.98	4.32	-	3.84	-	3.7	-	V
		$I_{O} = -7.8 \text{ mA}; V_{CC} = 6.0 \text{ V}$	5.48	5.81	-	5.34	-	5.2	-	V
V _{OL} LOW-level		$V_I = V_{IH}$ or V_{IL}								
	output voltage	$I_O = 20 \mu A; V_{CC} = 2.0 \text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 20 \mu A; V_{CC} = 4.5 V$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 20 \mu A; V_{CC} = 6.0 \text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_{O} = 6.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	0.15	0.26	-	0.33	-	0.4	V
		$I_O = 7.8 \text{ mA}; V_{CC} = 6.0 \text{ V}$	-	0.16	0.26	-	0.33	-	0.4	V
l _l	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0 \text{ V}$	-	-	±0.1	-	±1.0	-	±1.0	μА
l _{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 6.0$ V; $V_O = V_{CC}$ or GND	-	±0.5	-	±5.0	-	±10	-	μА
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0 \text{ V}$	-	-	8.0	-	80	-	160	μА
C _I	input capacitance		-	3.5	-	-	-	-	-	pF
74HCT5	40-Q100									
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 \text{ V}$								
	output voltage	I _O = -20 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -6.0 mA	3.98	4.32	-	3.84	-	3.7	-	V
V _{OL}	LOW-level	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 \text{ V}$								
	output voltage	I _O = 20 μA;	-	0	0.1	-	0.1	-	0.1	V
		I _O = 6.0 mA;	-	0.16	0.26	-	0.33	-	0.4	V

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 Table 6.
 Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T _{an}	_{nb} = 25	°C		-40 °C 85 °C		-40 °C 125 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	
I ₁	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$	-	-	±0.1	-	±1.0	-	±1.0	μΑ
l _{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 5.5$ V; $V_O = V_{CC}$ or GND	-	-	±0.5	-	±5.0	-	±10	μА
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5 \text{ V}$	-	-	8.0	-	80	-	160	μΑ
Δl _{CC}	additional supply current	per input pin; $I_O = 0$ A; $V_I = V_{CC} - 2.1$ V; other inputs at V_{CC} or GND; $V_{CC} = 4.5$ V to 5.5 V								
		An input	-	140	504	-	630	-	686	μΑ
		OE1 input	-	150	540	-	675	-	735	μΑ
		OE2 input	-	100	360	-	450	-	490	μΑ
C _I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

 $GND = 0 \ V; \ C_L = 50 \ pF;$ for test circuit see <u>Figure 8</u>.

Symbol	Parameter	Conditions		Tan	_{nb} = 25	°C	T _{amb} = -40 °	C to +125 °C	Unit
				Min	Тур	Max	Max (85 °C)	Max (125 °C)	
74HC540)-Q100								1
t _{pd}	propagation delay	An to Yn; see Figure 6	[1]						
		V _{CC} = 2.0 V		-	30	100	125	150	ns
		V _{CC} = 4.5 V		-	11	20	25	30	ns
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$		-	9	-	-	-	ns
		V _{CC} = 6.0 V		-	9	17	21	26	ns
t _{en}	enable time	OEn to Yn; see Figure 7	[1]						
		V _{CC} = 2.0 V		-	52	160	200	240	ns
		V _{CC} = 4.5 V		-	19	32	40	48	ns
		V _{CC} = 6.0 V		-	15	27	34	41	ns
t _{dis}	disable time	OEn to Yn; see Figure 7	[1]						
		V _{CC} = 2.0 V		-	61	160	200	240	ns
		V _{CC} = 4.5 V		-	22	32	40	48	ns
		V _{CC} = 6.0 V		-	18	27	34	41	ns
t _t	transition time	see Figure 6	[2]						
		V _{CC} = 2.0 V		-	14	60	75	90	ns
		V _{CC} = 4.5 V		-	5	12	15	18	ns
		V _{CC} = 6.0 V		-	4	10	13	15	ns

Table 7. Dynamic characteristics

 $GND = 0 \ V; \ C_L = 50 \ pF;$ for test circuit see <u>Figure 8</u>.

Symbol	Parameter	Conditions		Tan	_{nb} = 25	°C	T _{amb} = -40 °	C to +125 °C	Unit
				Min	Тур	Max	Max (85 °C)	Max (125 °C)	
C _{PD}	power dissipation capacitance	per package; V _I = GND to V _{CC}	[3]	-	39	-	-	-	pF
74HCT54	40-Q100								
t _{pd}	propagation delay	An to Yn; see Figure 6	[1]						
		V _{CC} = 4.5 V		-	13	24	30	36	ns
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$		-	11	-	-	-	ns
t _{en}	enable time	OEn to Yn; see Figure 7	<u>[1]</u>						
		V _{CC} = 4.5 V		-	22	35	44	53	ns
t _{dis}	disable time	OEn to Yn; see Figure 7	<u>[1]</u>						
		V _{CC} = 4.5 V		-	23	35	44	53	ns
t _t	transition time	V _{CC} = 4.5 V; see <u>Figure 6</u>	[2]	-	5	12	15	18	ns
C _{PD}	power dissipation capacitance	per package; V _I = GND to V _{CC} – 1.5 V	[3]	-	44	-	-	-	pF

[1] t_{pd} is the same as t_{PLH} and t_{PHL} .

 t_{en} is the same as t_{PZL} and $t_{\text{PZH}}.$

 t_{dis} is the same as t_{PLZ} and t_{PHZ} .

[2] t_t is the same as t_{THL} and t_{TLH} .

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$

 f_i = input frequency in MHz;

 f_o = output frequency in MHz;

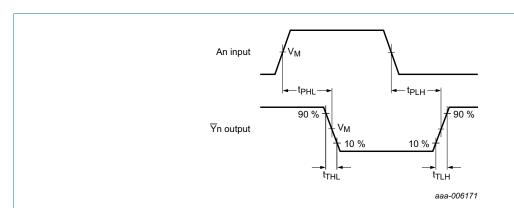
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

11. Waveforms



Measurement points are given in Table 8.

 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 6. Input to output propagation delays

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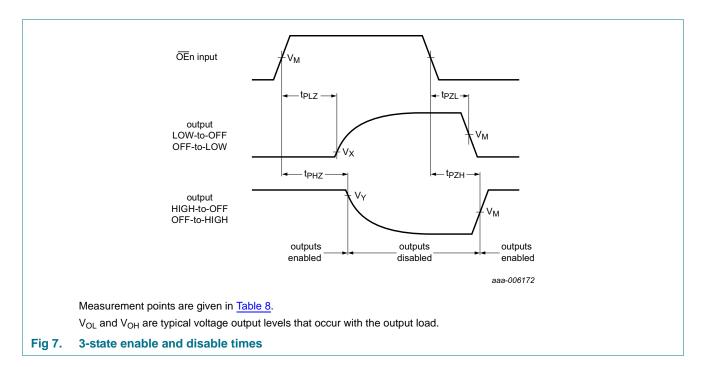
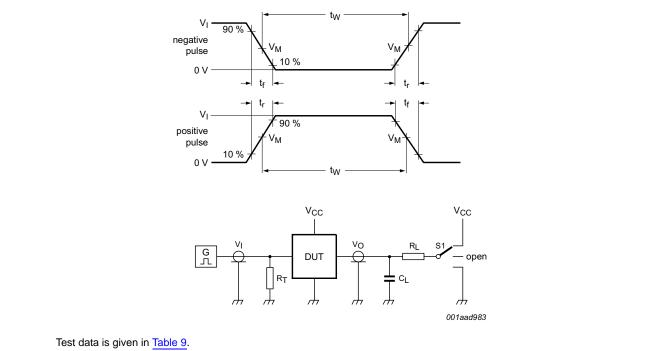


Table 8. Measurement points

Туре	Input	Output					
	V _M	V _M	V _X	V _Y			
74HC540-Q100	0.5V _{CC}	0.5V _{CC}	0.1V _{CC}	0.9V _{CC}			
74HCT540-Q100	1.3 V	1.3 V	0.1V _{CC}	0.9V _{CC}			

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Tost data is given in table s

Definitions test circuit:

 R_T = Termination resistance should be equal to output impedance Z_0 of the pulse generator

 $\ensuremath{C_L}$ = Load capacitance including jig and probe capacitance

R_L = Load resistance

S1 = Test selection switch

Fig 8. Test circuit for measuring switching times

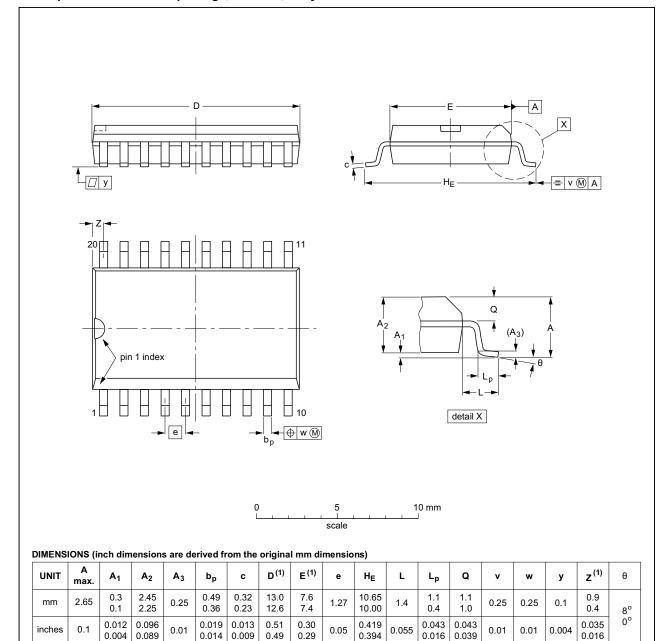
Table 9. Test data

Туре	Input		Load		S1 position		
	VI	t _r , t _f	CL	R _L	t _{PHL} , t _{PLH}	t _{PZH} , t _{PHZ}	t _{PZL} , t _{PLZ}
74HC540-Q100	V _{CC}	6 ns	15 pF, 50 pF	1 kΩ	open	GND	V _{CC}
74HCT540-Q100	3 V	6 ns	15 pF, 50 pF	1 kΩ	open	GND	V _{CC}

12. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE	
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE
SOT163-1	075E04	MS-013			99-12-27 03-02-19

Fig 9. Package outline SOT163-1 (SO20)

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13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic
MIL	Military
MM	Machine Model

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT540_Q100 v.2	20160301	Product data sheet	-	74HC_HCT540_Q100 v.1
Modifications:	 Type numbers 74HC540N-Q100 and 74HCT540N-Q100 (SOT146-1) removed. 			
74HC_HCT540_Q100 v.1	20130121	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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74HC540-Q100; 74HCT540-Q100

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Octal buffer/line driver; 3-state; inverting

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