

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## **74HC/HCT640**

Octal bus transceiver; 3-state;  
inverting

Product specification  
File under Integrated Circuits, IC06

March 1988

## Octal bus transceiver; 3-state; inverting

## 74HC/HCT640

## FEATURES

- Octal bidirectional bus interface
- Inverting 3-state outputs
- Output capability: bus driver
- I<sub>CC</sub> category: MSI

## GENERAL DESCRIPTION

The 74HC/HCT640 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT640 are octal transceivers featuring inverting 3-state bus compatible outputs in both send and receive directions.

The "640" features an output enable ( $\overline{OE}$ ) input for easy cascading and a send/receive (DIR) for direction control.  $\overline{OE}$  controls the outputs so that the buses are effectively isolated. The "640" is similar to the "245" but has inverting outputs.

## QUICK REFERENCE DATA

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay A <sub>n</sub> to B <sub>n</sub> ; B <sub>n</sub> to A <sub>n</sub>	C <sub>L</sub> = 15 pF; V <sub>CC</sub> = 5 V	9	9	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>I/O</sub>	input/output capacitance		10	10	pF
C <sub>PD</sub>	power dissipation capacitance per transceiver	notes 1 and 2	35	35	pF

## Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz

f<sub>o</sub> = output frequency in MHz

∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in V

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> – 1.5 V

## ORDERING INFORMATION

See "74HC/HCT/HCU/HCMOS Logic Package Information".

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## PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	DIR	direction control
2, 3, 4, 5, 6, 7, 8, 9	A <sub>0</sub> to A <sub>7</sub>	data inputs/outputs
10	GND	ground (0 V)
18, 17, 16, 15, 14, 13, 12, 11	B <sub>0</sub> to B <sub>7</sub>	data inputs/outputs
19	$\overline{OE}$	output enable input (active LOW)
20	V <sub>CC</sub>	positive supply voltage

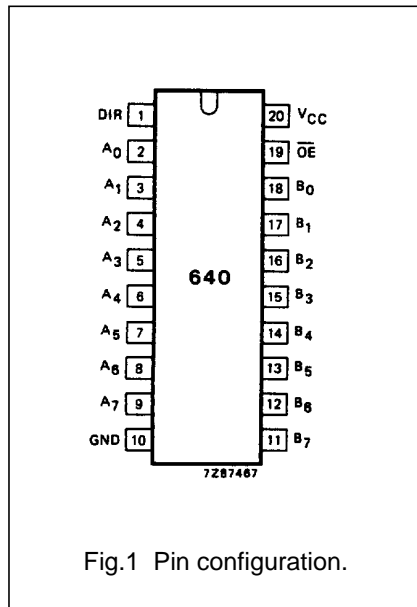


Fig.1 Pin configuration.

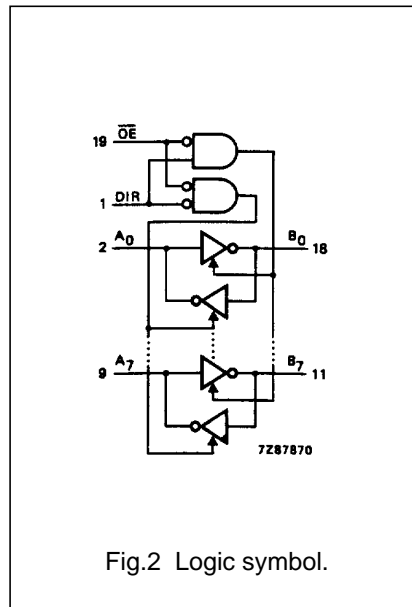


Fig.2 Logic symbol.

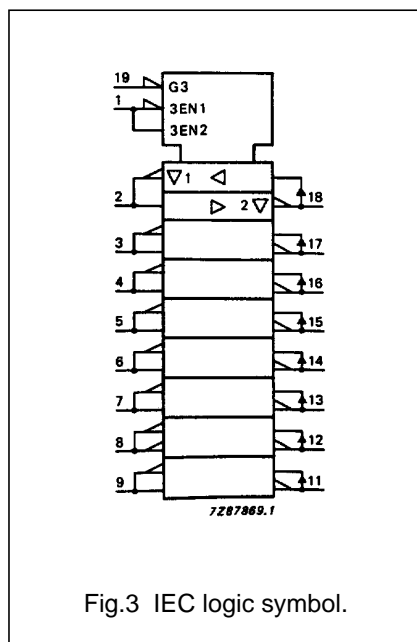


Fig.3 IEC logic symbol.

## FUNCTION TABLE

inputs		inputs/outputs	
$\overline{OE}$	DIR	A <sub>n</sub>	B <sub>n</sub>
L	L	A= $\overline{B}$	inputs
L	H	inputs	B= $\overline{A}$
H	X	Z	Z

### Note

- H = HIGH voltage level  
L = LOW voltage level  
X = don't care  
Z = high impedance OFF-state

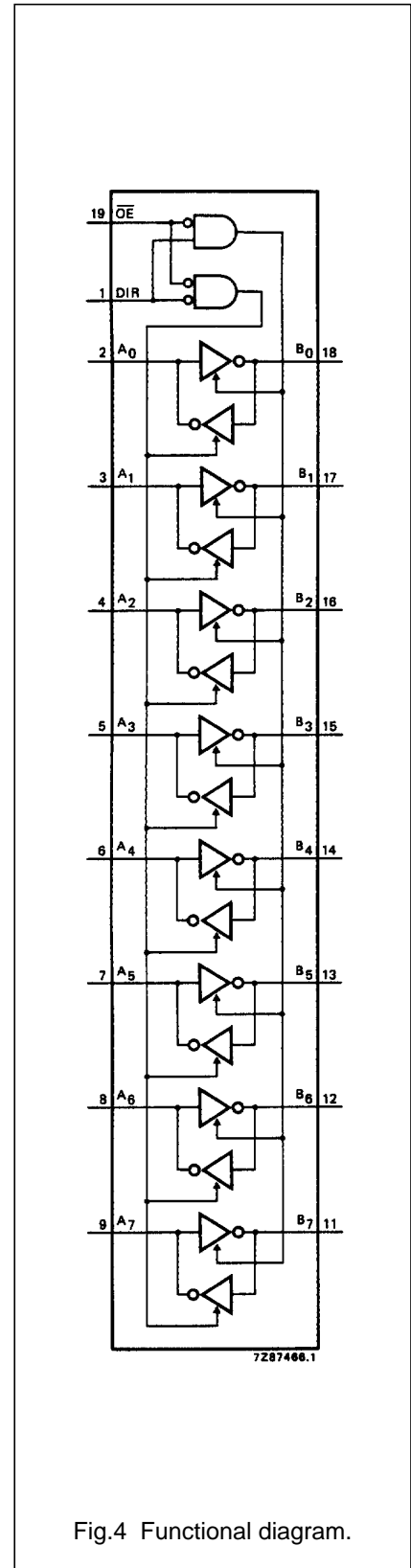


Fig.4 Functional diagram.

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**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> to B <sub>n</sub> ; B <sub>n</sub> to A <sub>n</sub>		30 11 9	90 18 15		115 23 20		135 27 23	ns	2.0 4.5 6.0	Fig.5
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time $\overline{OE}$ , DIR to A <sub>n</sub> ; $\overline{OE}$ , DIR to B <sub>n</sub>		44 16 13	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.6
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time $\overline{OE}$ , DIR to A <sub>n</sub> ; $\overline{OE}$ , DIR to B <sub>n</sub>		50 18 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig.5

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## 74HC/HCT640

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
A <sub>n</sub>	1.50
B <sub>n</sub>	1.50
$\overline{OE}$	1.50
DIR	0.90

**AC CHARACTERISTICS FOR 74HCT**

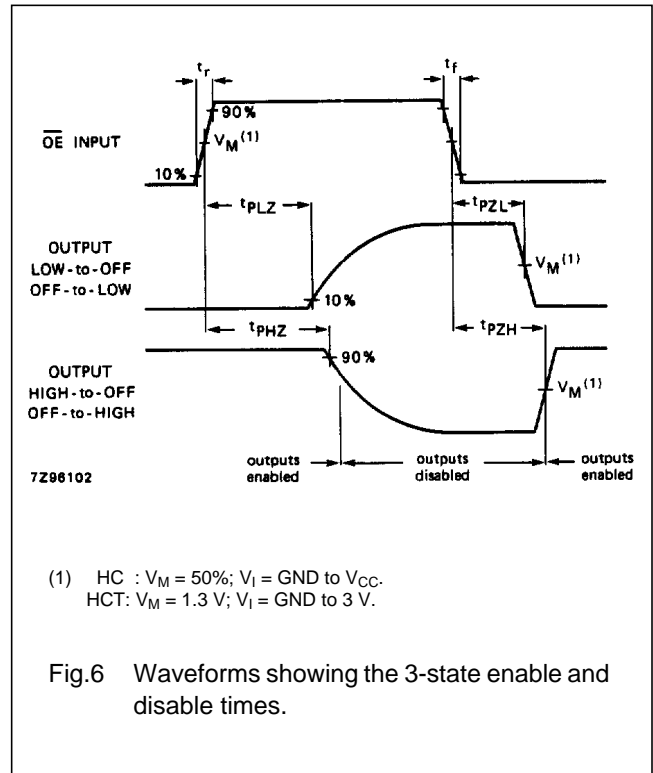
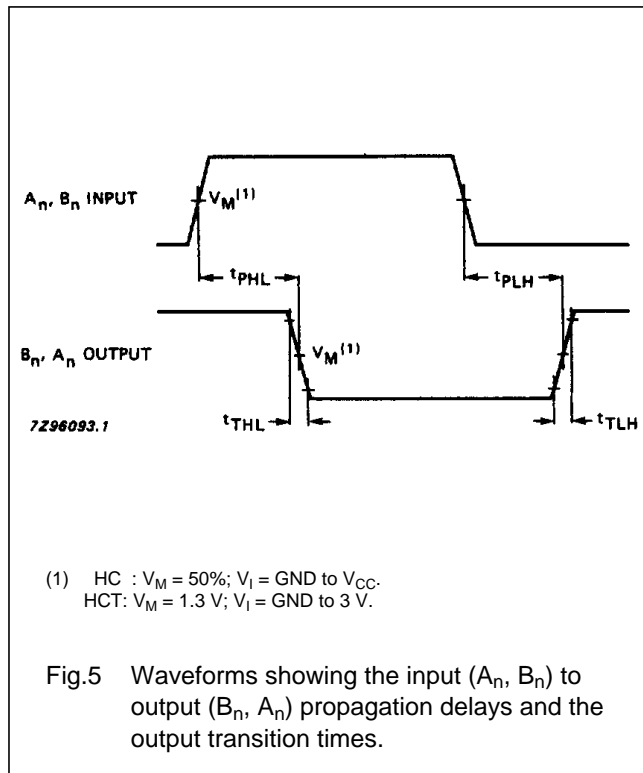
GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)								UNIT	TEST CONDITIONS	
		74HCT									V <sub>CC</sub> (V)	WAVEFORMS
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> to B <sub>n</sub> ; B <sub>n</sub> to A <sub>n</sub>		11	22		28		33	ns	4.5	Fig.5	
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time $\overline{OE}$ , DIR to A <sub>n</sub> ; $\overline{OE}$ , DIR to B <sub>n</sub>		18	30		38		45	ns	4.5	Fig.6	
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time $\overline{OE}$ , DIR to A <sub>n</sub> ; $\overline{OE}$ , DIR to B <sub>n</sub>		19	30		38		45	ns	4.5	Fig.6	
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		5	12		15		18	ns	4.5	Fig.5	

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AC WAVEFORMS



PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".