74HC74; 74HCT74

Dual D-type flip-flop with set and reset; positive edge-trigger

Rev. 5 — 3 December 2015 Product data sheet

1. General description

The 74HC74 and 74HCT74 are dual positive edge triggered D-type flip-flop. They have individual data (nD), clock (nCP), set ($\overline{n}SD$) and reset ($\overline{n}RD$) inputs, and complementary nQ and $n\overline{Q}$ outputs. Data at the nD-input, that meets the set-up and hold time requirements on the LOW-to-HIGH clock transition, is stored in the flip-flop and appears at the nQ output. Schmitt-trigger action in the clock input, makes the circuit highly tolerant to slower clock rise and fall times. Inputs include clamp diodes that enable the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2. Features and benefits

- Input levels:
  - For 74HC74: CMOS level
  - For 74HCT74: TTL level
- Symmetrical output impedance
- Low power dissipation
- High noise immunity
- Balanced propagation delays
- Specified in compliance with JEDEC standard no. 7A
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from –40 °C to +85 °C and from –40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC74D	–40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74HCT74D				
74HC74DB	–40 °C to +125 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74HCT74DB				

Table 1. Ordering information *…continued*

Type number	Package			
	Temperature range	Name	Description	Version
74HC74PW	−40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74HCT74PW				
74HC74BQ	−40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1
74HCT74BQ				

4. Functional diagram

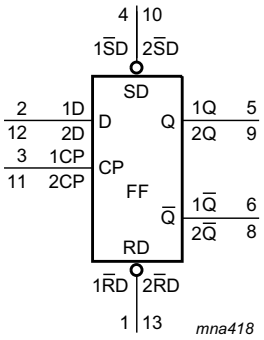


Fig 1. Logic symbol

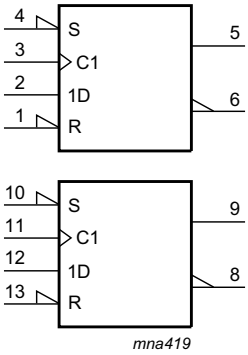


Fig 2. IEC logic symbol

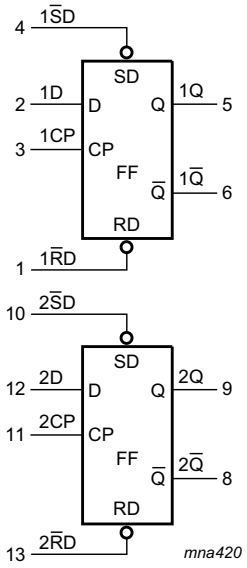


Fig 3. Functional diagram

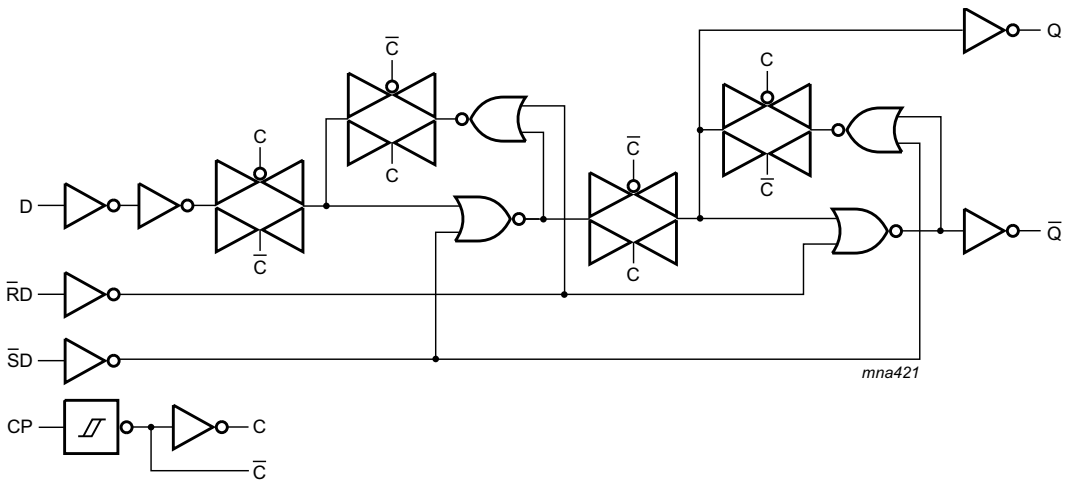


Fig 4. Logic diagram for one flip-flop

5. Pinning information

5.1 Pinning

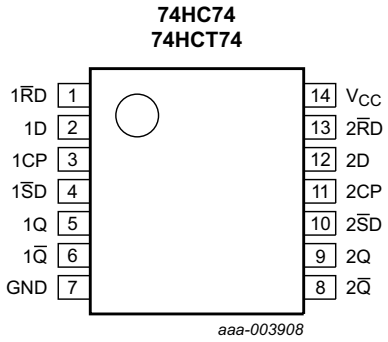
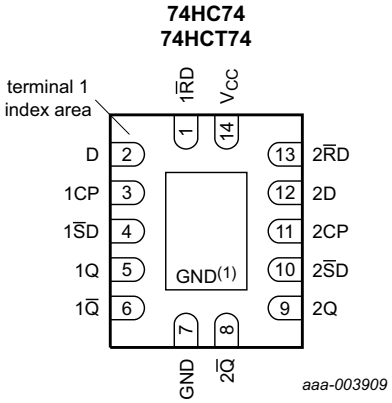


Fig 5. Pin configuration for SO14 and (T)SSOP14



Transparent top view

(1) This is not a supply pin. The substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However, if it is soldered, the solder land should remain floating or be connected to GND.

Fig 6. Pin configuration for DHVQFN14

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$1\overline{RD}$	1	asynchronous reset-direct input (active LOW)
1D	2	data input
1CP	3	clock input (LOW-to-HIGH, edge-triggered)
$1\overline{SD}$	4	asynchronous set-direct input (active LOW)
1Q	5	output
$1\overline{Q}$	6	complement output
GND	7	ground (0 V)
$2\overline{Q}$	8	complement output
2Q	9	output
$2\overline{SD}$	10	asynchronous set-direct input (active LOW)
2CP	11	clock input (LOW-to-HIGH, edge-triggered)
2D	12	data input
$2\overline{RD}$	13	asynchronous reset-direct input (active LOW)
V_{CC}	14	supply voltage

6. Functional description

Table 3. Function table[1]

Input				Output	
$\overline{nSD}$	$\overline{nRD}$	nCP	nD	nQ	$\overline{nQ}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care.

Table 4. Function table[1]

Input				Output	
$\overline{nSD}$	$\overline{nRD}$	nCP	nD	nQ_{n+1}	$\overline{nQ}_{n+1}$
H	H	↑	L	L	H
H	H	↑	H	H	L

[1] H = HIGH voltage level; L = LOW voltage level; ↑ = LOW-to-HIGH transition; Q_{n+1} = state after the next LOW-to-HIGH CP transition; X = don't care.

7. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		–0.5	+7	V
I_{IK}	input clamping current	$V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V	-	±20	mA
I_{OK}	output clamping current	$V_O < –0.5$ V or $V_O > V_{CC} + 0.5$ V	-	±20	mA
I_O	output current	$V_O = –0.5$ V to $(V_{CC} + 0.5$ V)	-	±25	mA
I_{CC}	supply current		-	+100	mA
I_{GND}	ground current		–100	-	mA
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	total power dissipation	SO14, (T)SSOP14 and DHVQFN14 packages [1]	-	500	mW

[1] For SO14 package: P_{tot} derates linearly with 8 mW/K above 70 °C.
For (T)SSOP14 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.
For DHVQFN14 packages: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC74			74HCT74			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	+25	+125	–40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V_{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T_{amb} = –40 °C to +85 °C			T_{amb} = –40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
74HC74								
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	1.5	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	3.15	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = –4.0 mA; V_{CC} = 4.5 V	3.84	4.32	-	3.7	-	V
		I_O = –5.2 mA; V_{CC} = 6.0 V	5.34	5.81	-	5.2	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	0.15	0.33	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±1.0	-	±1.0	μA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	40	-	80	μA
C_I	input capacitance		-	3.5	-	-	-	pF

Table 7. Static characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T_{amb} = –40 °C to +85 °C			T_{amb} = –40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
74HCT74								
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V						
		I_O = –4 mA	3.84	4.32	-	3.7	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V						
		I_O = 4.0 mA	-	0.15	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 5.5 V	-	-	±1.0	-	±1.0	µA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	40	-	80	µA
ΔI_{CC}	additional supply current	V_I = V_{CC} – 2.1 V; other inputs at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V; I_O = 0 A						
		per input pin; nD, $n\overline{R}D$ inputs	-	70	315	-	343	µA
		per input pin; $n\overline{S}D$, nCP input	-	80	360	-	392	µA
C_I	input capacitance		-	3.5	-	-	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.

10. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit see Figure 9.

Symbol	Parameter	Conditions	T_{amb} = –40 °C to +85 °C			T_{amb} = –40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
74HC74								
t_{pd}	propagation delay	nCP to nQ, n$\overline{Q}$; see Figure 7 [2]						
		V_{CC} = 2.0 V	-	47	220	-	265	ns
		V_{CC} = 4.5 V	-	17	44	-	53	ns
		V_{CC} = 5 V; C_L = 15 pF	-	14	-	-	-	ns
		V_{CC} = 6.0 V	-	14	37	-	45	ns
		n$\overline{SD}$ to nQ, n$\overline{Q}$; see Figure 8 [2]						
		V_{CC} = 2.0 V	-	50	250	-	300	ns
		V_{CC} = 4.5 V	-	18	50	-	60	ns
		V_{CC} = 5 V; C_L = 15 pF	-	15	-	-	-	ns
		V_{CC} = 6.0 V	-	14	43	-	51	ns
		n$\overline{RD}$ to nQ, n$\overline{Q}$; see Figure 8 [2]						
		V_{CC} = 2.0 V	-	52	250	-	300	ns
		V_{CC} = 4.5 V	-	19	50	-	60	ns
		V_{CC} = 5 V; C_L = 15 pF	-	16	-	-	-	ns
		V_{CC} = 6.0 V	-	15	43	-	51	ns
t_t	transition time	nQ, n$\overline{Q}$; see Figure 7 [3]						
		V_{CC} = 2.0 V	-	19	95	-	110	ns
		V_{CC} = 4.5 V	-	7	19	-	22	ns
		V_{CC} = 6.0 V	-	6	16	-	19	ns
t_W	pulse width	nCP HIGH or LOW; see Figure 7						
		V_{CC} = 2.0 V	100	19	-	120	-	ns
		V_{CC} = 4.5 V	20	7	-	24	-	ns
		V_{CC} = 6.0 V	17	6	-	20	-	ns
		n$\overline{SD}$, n$\overline{RD}$ LOW; see Figure 8						
		V_{CC} = 2.0 V	100	19	-	120	-	ns
		V_{CC} = 4.5 V	20	7	-	24	-	ns
		V_{CC} = 6.0 V	17	6	-	20	-	ns
t_{rec}	recovery time	n$\overline{SD}$, n$\overline{RD}$; see Figure 8						
		V_{CC} = 2.0 V	40	3	-	45	-	ns
		V_{CC} = 4.5 V	8	1	-	9	-	ns
		V_{CC} = 6.0 V	7	1	-	8	-	ns

Table 8. Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit see Figure 9.

Symbol	Parameter	Conditions	T_{amb} = –40 °C to +85 °C			T_{amb} = –40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t_{su}	set-up time	nD to nCP; see Figure 7						
		V_{CC} = 2.0 V	75	6	-	90	-	ns
		V_{CC} = 4.5 V	15	2	-	18	-	ns
		V_{CC} = 6.0 V	13	2	-	15	-	ns
t_h	hold time	nD to nCP; see Figure 7						
		V_{CC} = 2.0 V	3	–6	-	3	-	ns
		V_{CC} = 4.5 V	3	–2	-	3	-	ns
		V_{CC} = 6.0 V	3	–2	-	3	-	ns
f_{max}	maximum frequency	nCP; see Figure 7						
		V_{CC} = 2.0 V	4.8	23	-	4.0	-	MHz
		V_{CC} = 4.5 V	24	69	-	20	-	MHz
		V_{CC} = 5 V; C_L = 15 pF	-	76	-	-	-	MHz
		V_{CC} = 6.0 V	28	82	-	24	-	MHz
C_{PD}	power dissipation capacitance	C_L = 50 pF; f = 1 MHz; V_I = GND to V_{CC} [4]	-	24	-	-	-	pF
74HCT74								
t_{pd}	propagation delay	nCP to nQ, n$\overline{Q}$; see Figure 7 [2]						
		V_{CC} = 4.5 V	-	18	44	-	53	ns
		V_{CC} = 5 V; C_L = 15 pF	-	15	-	-	-	ns
		n$\overline{SD}$ to nQ, n$\overline{Q}$; see Figure 8 [2]						
		V_{CC} = 4.5 V	-	23	50	-	60	ns
		V_{CC} = 5 V; C_L = 15 pF	-	18	-	-	-	ns
		n$\overline{RD}$ to nQ, n$\overline{Q}$; see Figure 8 [2]						
		V_{CC} = 4.5 V	-	24	50	-	60	ns
		V_{CC} = 5 V; C_L = 15 pF	-	18	-	-	-	ns
t_t	transition time	nQ, n$\overline{Q}$; see Figure 7 [3]						
		V_{CC} = 4.5 V	-	7	19	-	22	ns
t_W	pulse width	nCP HIGH or LOW; see Figure 7						
		V_{CC} = 4.5 V	23	9	-	27	-	ns
		n$\overline{SD}$, n$\overline{RD}$ LOW; see Figure 8						
		V_{CC} = 4.5 V	20	9	-	24	-	ns
t_{rec}	recovery time	n$\overline{SD}$, n$\overline{RD}$; see Figure 8						
		V_{CC} = 4.5 V	8	1	-	9	-	ns
t_{su}	set-up time	nD to nCP; see Figure 7						
		V_{CC} = 4.5 V	15	5	-	18	-	ns

Table 8. Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit see Figure 9.

Symbol	Parameter	Conditions	T_{amb} = –40 °C to +85 °C			T_{amb} = –40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t_h	hold time	nD to nCP; see Figure 7						
		V_{CC} = 4.5 V	3	–3	-	3	-	ns
f_{max}	maximum frequency	nCP; see Figure 7						
		V_{CC} = 4.5 V	22	54	-	18	-	MHz
		V_{CC} = 5 V; C_L = 15 pF	-	59	-	-	-	MHz
C_{PD}	power dissipation capacitance	C_L = 50 pF; f = 1 MHz; V_I = GND to V_{CC} - 1.5 V [4]	-	29	-	-	-	pF

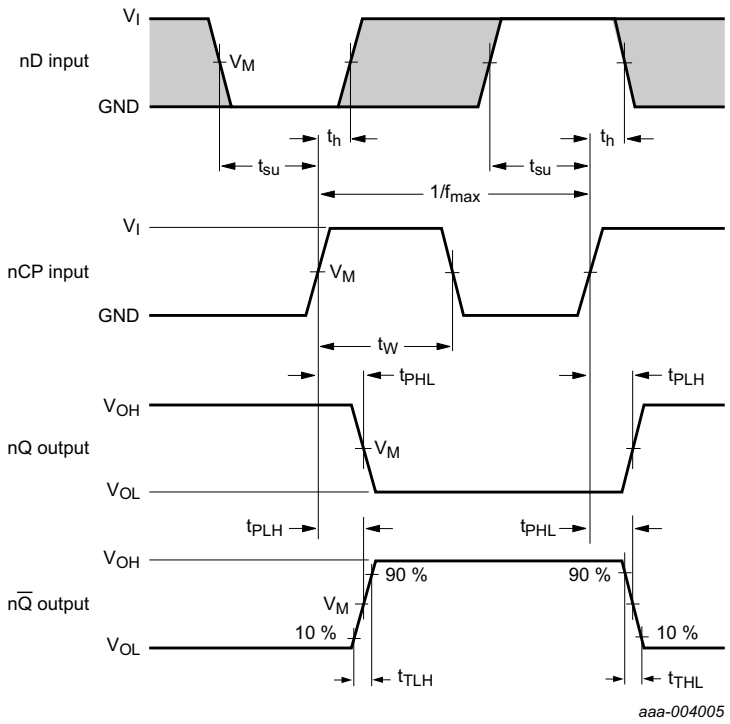
[1] All typical values are measured at T_{amb} = 25 °C.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] t_t is the same as t_{THL} and t_{TLH}.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

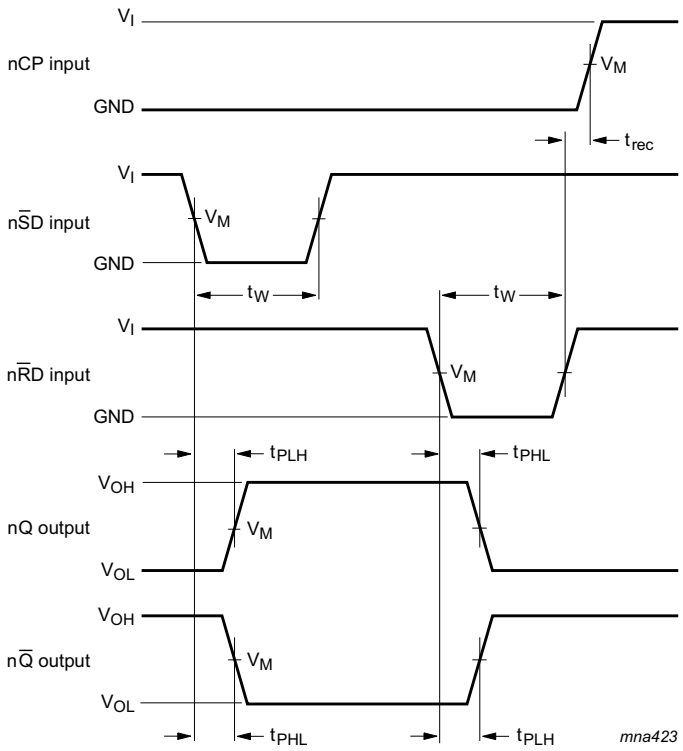
11. Waveforms



Measurement points are given in Table 9.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 7. Input to output propagation delay, output transition time, clock input pulse width and maximum frequency



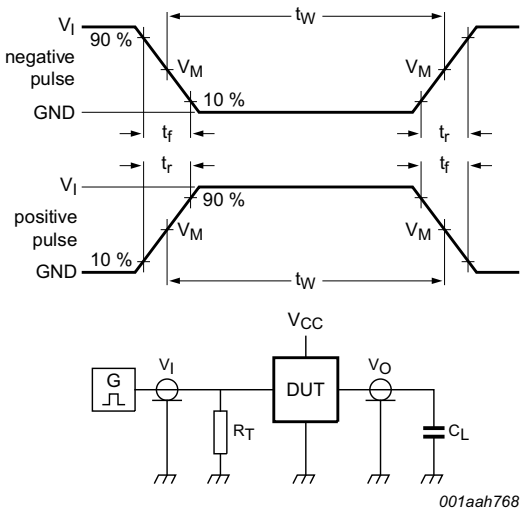
Measurement points are given in Table 9.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 8. Set and reset propogation delays, pulse widths and recovery time

Table 9. Measurement points

Type	Input	Output
	V_M	V_M
74HC74	$0.5V_{CC}$	$0.5V_{CC}$
74HCT74	1.3 V	1.3 V



Test data is given in Table 10.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

S1 = Test selection switch.

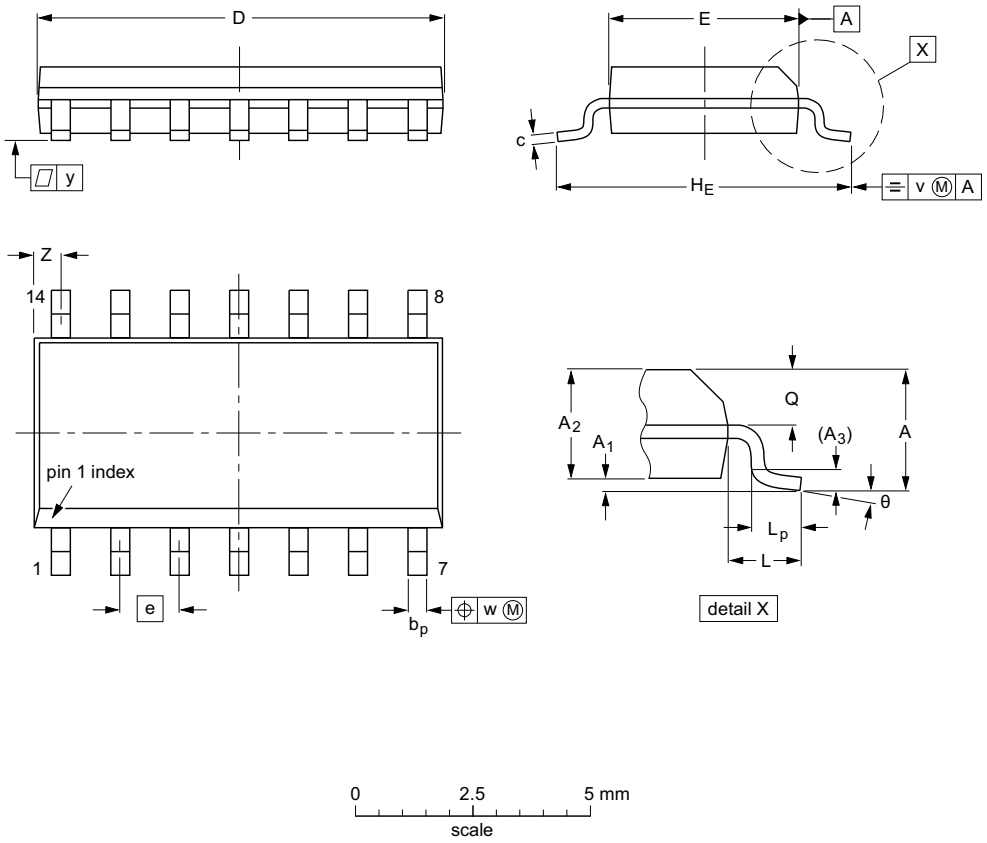
Fig 9. Test circuit for measuring switching times

Table 10. Test data

Type	Input		Load		Test
	V_I	t_r, t_f	C_L	R_L	
74HC74	V_{CC}	6 ns	15 pF, 50 pF	1 kΩ	t_{PLH}, t_{PHL}
74HCT74	3 V	6 ns	15 pF, 50 pF	1 kΩ	t_{PLH}, t_{PHL}

12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

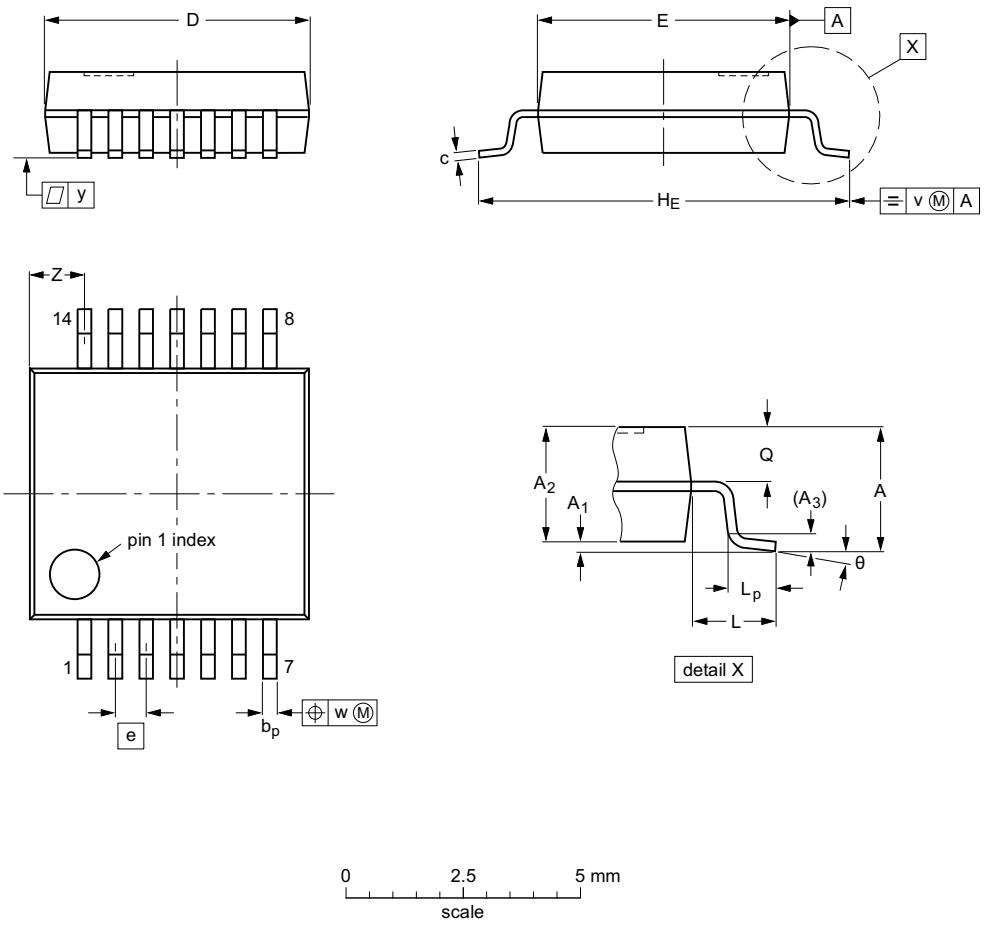
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Fig 10. Package outline SOT108-1 (SO14)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm **SOT337-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8^o 0^o

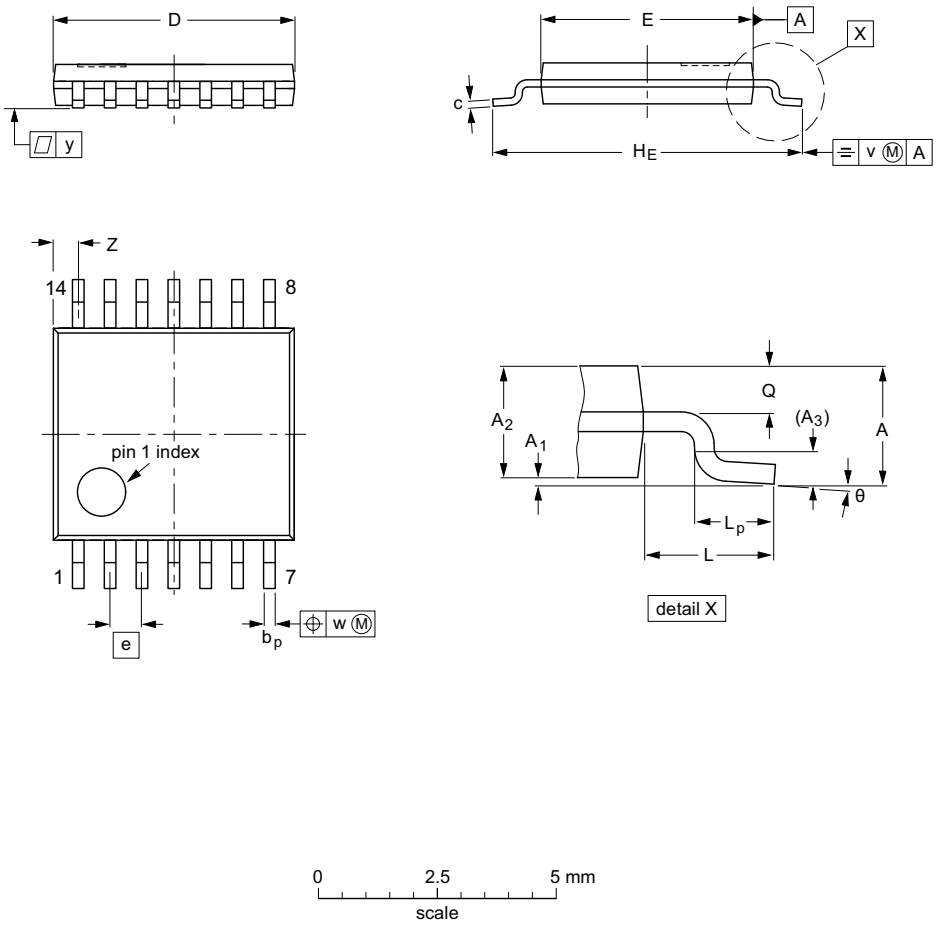
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT337-1		MO-150				~~99-12-27~~ 03-02-19

Fig 11. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

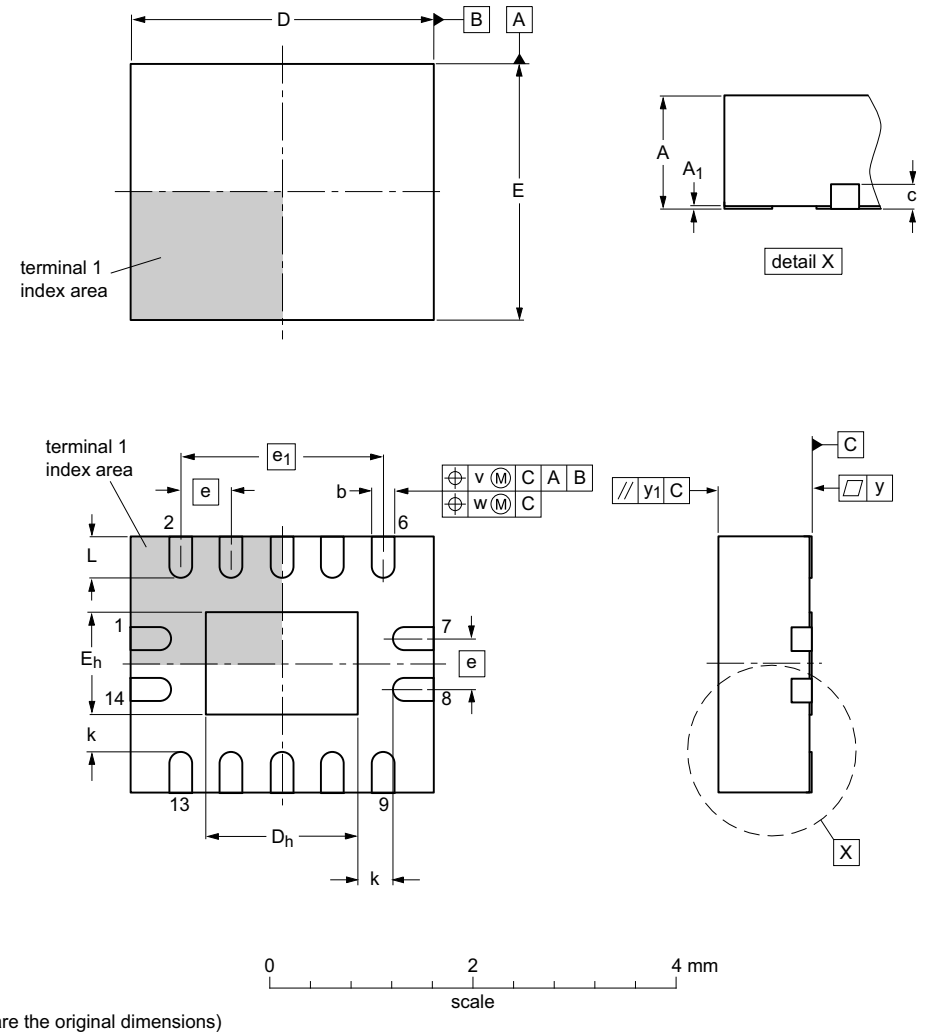
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Fig 12. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm **SOT762-1**



Dimensions (mm are the original dimensions)

Unit		$A^{(1)}$	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	k	L	v	w	y	y_1
	max	1	0.05	0.30		3.1	1.65	2.6	1.15				0.5				
mm	nom		0.02	0.25	0.2	3.0	1.50	2.5	1.00	0.5	2		0.4	0.1	0.05	0.05	0.1
	min		0.00	0.18		2.9	1.35	2.4	0.85			0.2	0.3				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot762-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT762-1		MO-241				~~15-04-10~~ 15-05-05

Fig 13. Package outline SOT762-1 (DHVQFN14)

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT74 v.5	20151203	Product data sheet	-	74HC_HCT74 v.4
Modifications:	• Type numbers 74HC74N and 74HCT74N (SOT27-1) removed.			
74HC_HCT74 v.4	20120827	Product data sheet	-	74HC_HCT74 v.3
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate.			
74HC_HCT74 v.3	20030710	Product data sheet	-	74HC_HCT74_CNV v.2
74HC_HCT74_CNV v.2	19980223	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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17. Contents

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Date of release: 03 December 2015