

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT4520

Dual 4-bit synchronous binary counter

Product specification
File under Integrated Circuits, IC06

December 1990

Dual 4-bit synchronous binary counter

74HC/HCT4520

FEATURES

- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4520 are high-speed Si-gate CMOS devices and are pin compatible with the "4520" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4520 are dual 4-bit internally synchronous binary counters with an active HIGH clock input (nCP₀) and an active LOW clock input (nCP₁), buffered outputs

from all four bit positions (nQ₀ to nQ₃) and an active HIGH overriding asynchronous master reset input (nMR).

The counter advances on either the LOW-to-HIGH transition of nCP₀ if nCP₁ is HIGH or the HIGH-to-LOW transition of nCP₁ if nCP₀ is LOW. Either nCP₀ or nCP₁ may be used as the clock input to the counter and the other clock input may be used as a clock enable input. A HIGH on nMR resets the counter (nQ₀ to nQ₃ = LOW) independent of nCP₀ and nCP₁.

APPLICATIONS

- Multistage synchronous counting
- Multistage asynchronous counting
- Frequency dividers

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | | UNIT |
|-------------------------------------|--|---|---------|-----|------|
| | | | HC | HCT | |
| t _{PHL} / t _{PLH} | propagation delay nCP ₀ , nCP ₁ to nQ _n | C _L = 15 pF; V _{CC} = 5 V | 24 | 24 | ns |
| t _{PHL} | propagation delay nMR to nQ _n | | 13 | 13 | ns |
| f _{max} | maximum clock frequency | | 68 | 64 | MHz |
| C _I | input capacitance | | 3.5 | 3.5 | pF |
| C _{PD} | power dissipation capacitance per counter | notes 1 and 2 | 29 | 24 | pF |

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

∑ (C_L × V_{CC}² × f_o) = sum of outputs

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}
For HCT the condition is V_I = GND to V_{CC} – 1.5 V

ORDERING INFORMATION

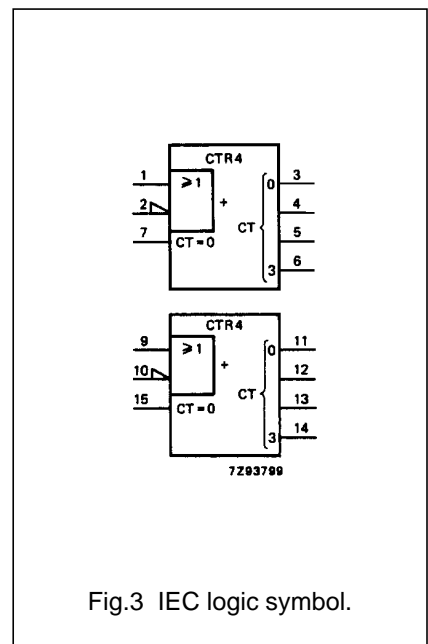
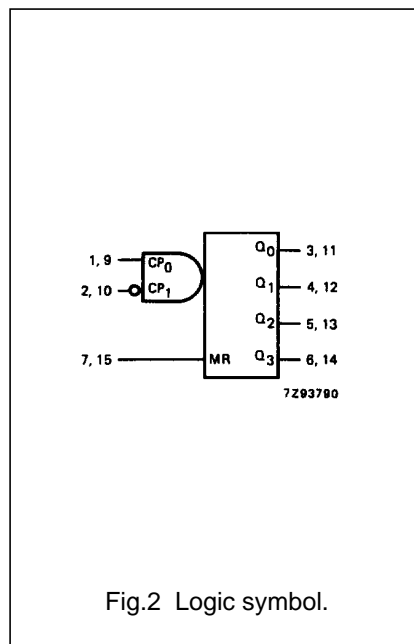
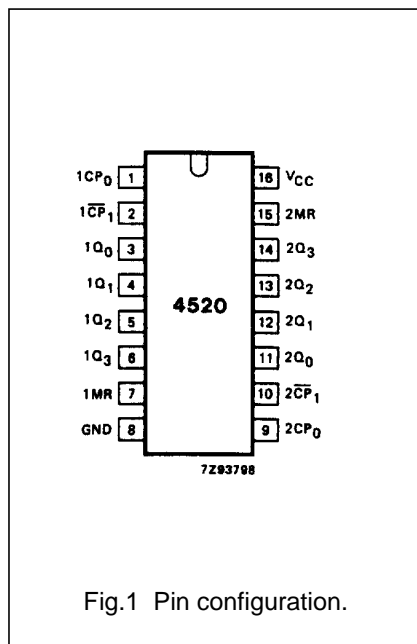
See "74HC/HCT/HCU/HCMOS Logic Package Information".

Dual 4-bit synchronous binary counter

74HC/HCT4520

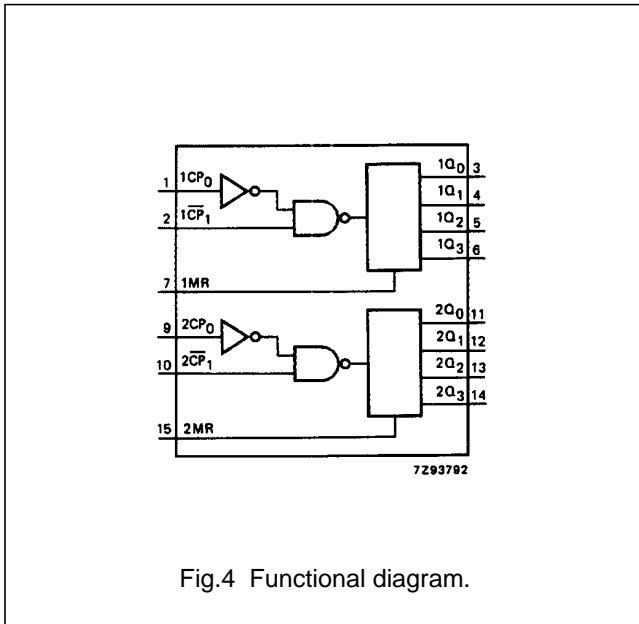
PIN DESCRIPTION

| PIN NO. | SYMBOL | NAME AND FUNCTION |
|----------------|-------------------------------------|--|
| 1, 9 | 1CP ₀ , 2CP ₀ | clock inputs (LOW-to-HIGH, edge-triggered) |
| 2, 10 | 1CP ₁ , 2CP ₁ | clock inputs (HIGH-to-LOW, edge-triggered) |
| 3, 4, 5, 6 | 1Q ₀ to 1Q ₃ | data outputs |
| 7, 15 | 1MR, 2MR | asynchronous master reset inputs (active HIGH) |
| 8 | GND | ground (0 V) |
| 11, 12, 13, 14 | 2Q ₀ to 2Q ₃ | data outputs |
| 16 | V _{CC} | positive supply voltage |



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74HC/HCT4520

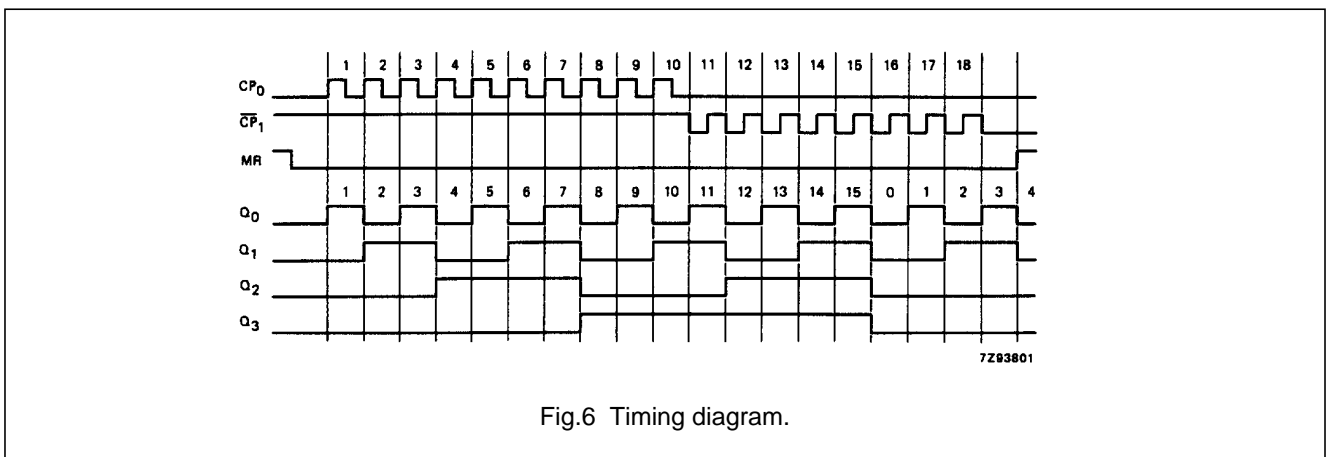
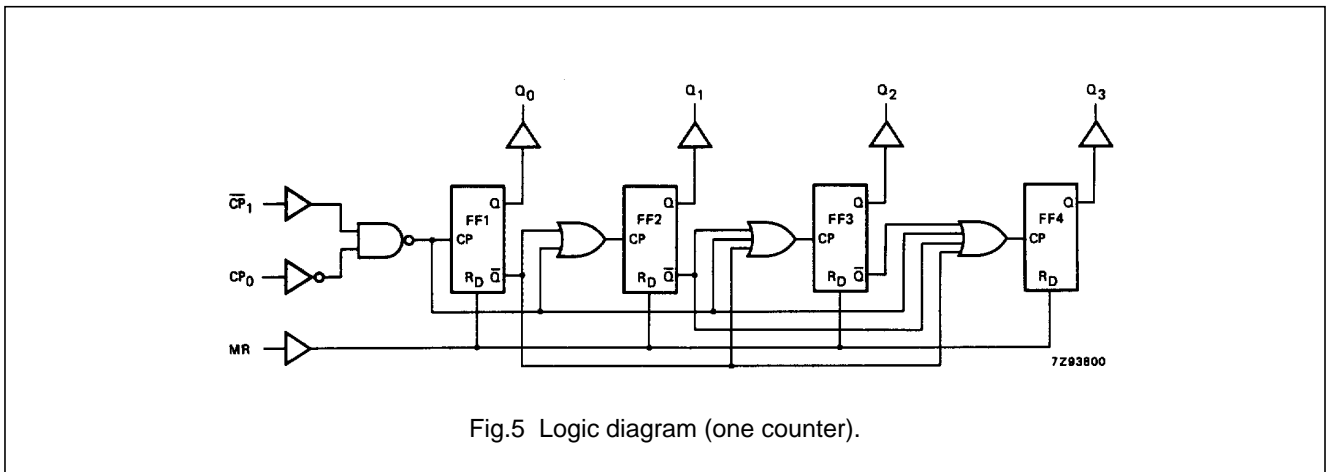


FUNCTION TABLE

| nCP ₀ | nCP ₁ | MR | MODE |
|------------------|------------------|----|--|
| ↑ | H | L | counter advances |
| L | ↓ | L | counter advances |
| ↓ | X | L | no change |
| X | ↑ | L | no change |
| ↑ | L | L | no change |
| H | ↓ | L | no change |
| X | X | H | Q ₀ to Q ₃ = LOW |

Notes

- H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH clock transition
↓ = HIGH-to-LOW clock transition



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DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

| SYMBOL | PARAMETER | T _{amb} (°C) | | | | | | UNIT | TEST CONDITIONS | | |
|-------------------------------------|---|-----------------------|------------------|-----------------|-----------------|-----------------|-----------------|-----------------|------------------------|-------------------|-------|
| | | 74HC | | | | | | | V _{CC} (V) | WAVEFORMS | |
| | | +25 | | | -40 to +85 | | -40 to +125 | | | | |
| | | min. | typ. | max. | min. | max. | min. | | | | max. |
| t _{PHL} / t _{PLH} | propagation delay nCP ₀ to nQ _n | | 77 28 22 | 240 48 41 | | 300 60 51 | | 360 72 61 | ns | 2.0 4.5 6.0 | Fig.8 |
| t _{PHL} / t _{PLH} | propagation delay nCP ₁ to nQ _n | | 77 28 22 | 240 48 41 | | 300 60 51 | | 360 72 61 | ns | 2.0 4.5 6.0 | Fig.8 |
| t _{PHL} | propagation delay nMR to nQ _n | | 44 16 13 | 150 30 26 | | 190 38 33 | | 225 45 38 | ns | 2.0 4.5 6.0 | Fig.9 |
| t _{THL} / t _{TLH} | output transition time | | 19 7 6 | 75 15 13 | | 95 19 16 | | 110 22 19 | ns | 2.0 4.5 6.0 | Fig.8 |
| t _w | clock pulse width HIGH or LOW | 80 16 14 | 22 8 6 | | 100 20 17 | | 120 24 20 | | ns | 2.0 4.5 6.0 | Fig.7 |
| t _w | master reset pulse width HIGH | 120 24 20 | 39 14 11 | | 150 30 26 | | 180 36 31 | | ns | 2.0 4.5 6.0 | Fig.7 |
| t _{rem} | removal time nMR to nCP ₀ ; nCP ₁ | 0 0 0 | -28 -10 -8 | | 0 0 0 | | 0 0 0 | | ns | 2.0 4.5 6.0 | Fig.7 |
| t _{su} | set-up time nCP ₁ to nCP ₀ ; nCP ₀ to nCP ₁ | 80 16 14 | 14 5 4 | | 100 20 17 | | 120 24 20 | | ns | 2.0 4.5 6.0 | Fig.8 |
| f _{max} | maximum clock pulse frequency | 6.0 30 35 | 19 58 69 | | 4.8 24 28 | | 4.0 20 24 | | MHz | 2.0 4.5 6.0 | Fig.7 |

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DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

| INPUT | UNIT LOAD COEFFICIENT |
|-------------------------------------|-----------------------|
| nCP ₀ , nCP ₁ | 0.80 |
| nMR | 1.50 |

AC CHARACTERISTICS FOR 74HCT

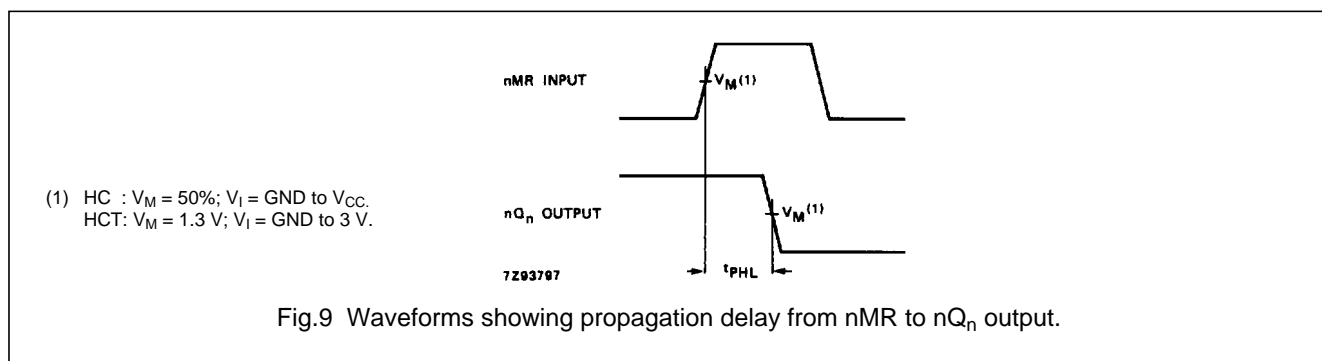
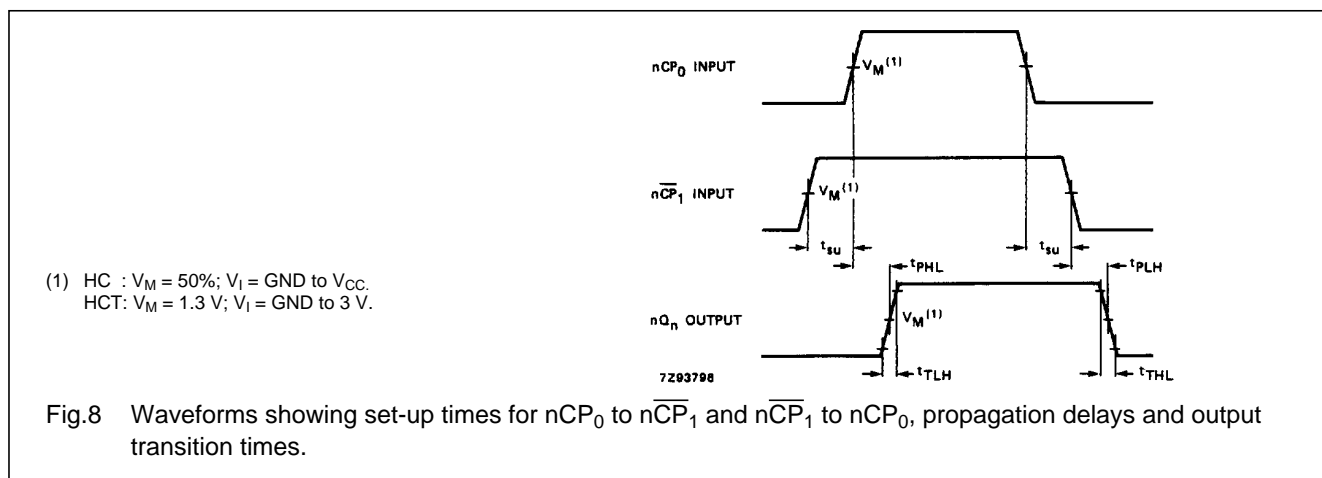
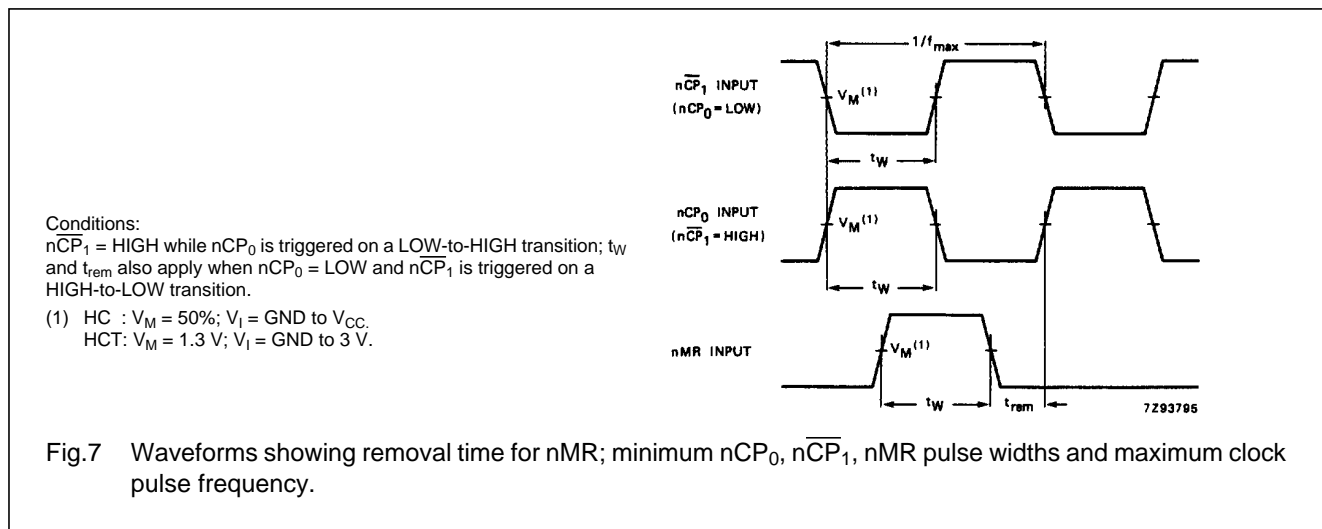
GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

| SYMBOL | PARAMETER | T _{amb} (°C) | | | | | | | UNIT | TEST CONDITIONS | |
|-------------------------------------|---|-----------------------|------|------|------------|------|-------------|------|------|------------------------|-----------|
| | | 74HCT | | | | | | | | V _{CC} (V) | WAVEFORMS |
| | | +25 | | | -40 to +85 | | -40 to +125 | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | |
| t _{PHL} / t _{PLH} | propagation delay nCP ₀ to nQ _n | | 28 | 53 | | 66 | | 80 | ns | 4.5 | Fig.8 |
| t _{PHL} / t _{PLH} | propagation delay nCP ₁ to nQ _n | | 25 | 53 | | 66 | | 80 | ns | 4.5 | Fig.8 |
| t _{PHL} | propagation delay nMR to nQ _n | | 16 | 35 | | 44 | | 53 | ns | 4.5 | Fig.9 |
| t _{THL} / t _{TLH} | output transition time | | 7 | 15 | | 19 | | 22 | ns | 4.5 | Fig.8 |
| t _W | clock pulse width HIGH or LOW | 20 | 10 | | 25 | | 30 | | ns | 4.5 | Fig.7 |
| t _W | master reset pulse width HIGH | 20 | 12 | | 25 | | 30 | | ns | 4.5 | Fig.7 |
| t _{rem} | removal time nMR to nCP ₀ ; nCP ₁ | 0 | -8 | | 0 | | 0 | | ns | 4.5 | Fig.7 |
| t _{su} | set-up time nCP ₁ to nCP ₀ ; nCP ₀ to nCP ₁ | 16 | 6 | | 20 | | 24 | | ns | 4.5 | Fig.8 |
| f _{max} | maximum clock pulse frequency | 30 | 58 | | 24 | | 20 | | MHz | 4.5 | Fig.7 |

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AC WAVEFORMS



PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".