74HC597; 74HCT597

8-bit shift register with input flip-flops

Rev. 3 — 15 April 2014 Product data sheet

1. General description

The 74HC597; 74HCT597 is an 8-bit shift register with input flip-flops. It consists of an 8-bit storage register feeding a parallel-in, serial-out 8-bit shift register. Both the storage register and the shift register have positive edge-triggered clocks. The shift register also has direct load (from storage) and clear inputs. Inputs include clamp diodes that enable the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2. Features and benefits

- Complies with JEDEC standard JESD7A
- Input levels:
  - For 74HC597: CMOS level
  - For 74HCT597: TTL level
- 8-bit parallel storage register inputs
- Shift register has direct overriding load and clear
- ESD protection:
  - HBM EIA/JESD22-A114F exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V
- Specified from −40 °C to +85 °C and from −40 °C to +125 °C
- Multiple package options

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC5974N	−40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
74HCT597N				
74HC597D	−40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT597D				
74HC597DB	−40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HCT597DB				
74HC597PW	−40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

4. Functional diagram

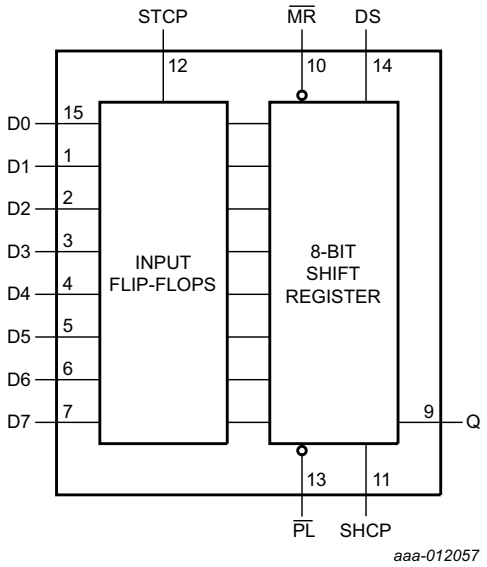


Fig 1. Functional diagram

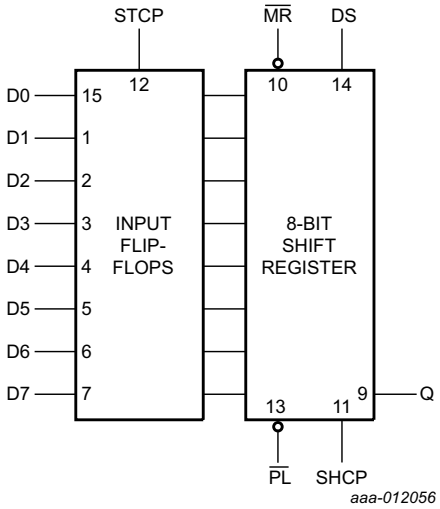


Fig 2. Logic symbol

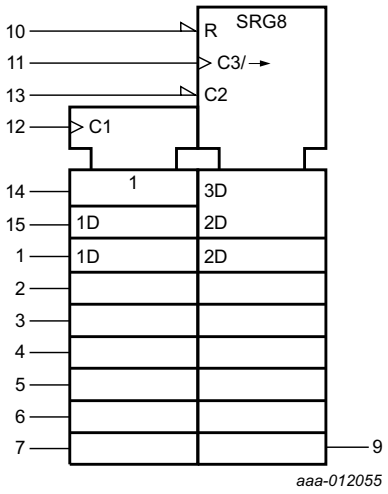


Fig 3. IEC Logic symbol

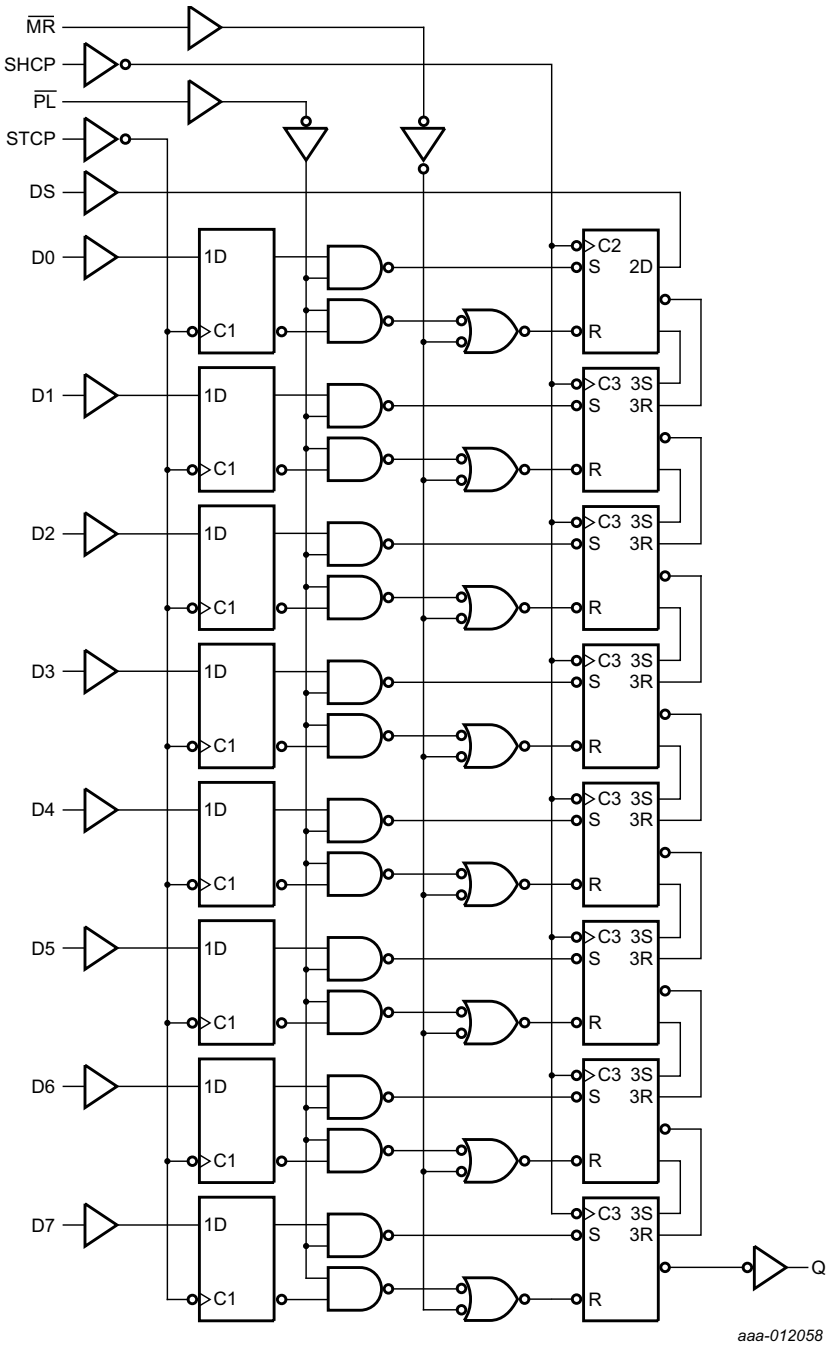


Fig 4. Logic diagram

5. Pinning information

5.1 Pinning

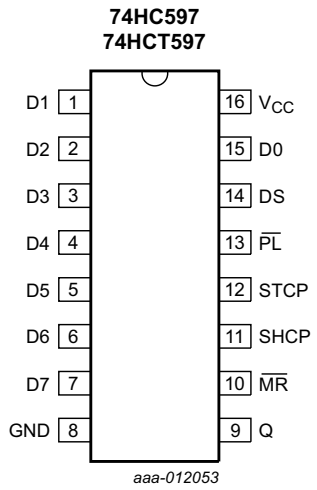


Fig 5. Pin configuration DIP16 and SO16

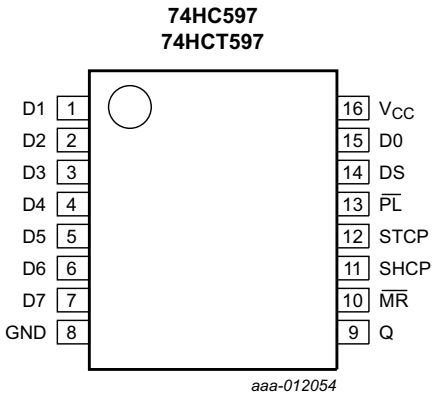


Fig 6. Pin configuration SSOP16 and TSSOP16

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
GND	8	ground (0 V)
Q	9	serial data output
$\overline{MR}$	10	asynchronous master reset input (active LOW)
SHCP	11	shift register clock input (LOW-to-HIGH, edge-triggered)
STCP	12	storage register clock input (LOW-to-HIGH, edge-triggered)
$\overline{PL}$	13	parallel load input (active LOW)
DS	14	serial data input
D0, D1, D2, D3, D4, D5, D6, D7	15, 1, 2, 3, 4, 5, 6, 7	parallel data inputs
V_{CC}	16	supply voltage

6. Functional description

Table 3. Function table[1]

Inputs				Function
STCP	SHCP	$\overline{PL}$	$\overline{MR}$	
↑	X	X	X	data loaded to input latches
↑	X	L	H	data loaded from inputs to shift register
no clock edge	X	L	H	data transferred from input flip-flops to shift register
X	X	L	L	invalid logic, state of shift register is indeterminate when signals removed
X	X	H	L	shift register cleared
X	↑	H	H	shift register clocked Qn = Qn−1, Q0 = DS

[1] H = HIGH voltage level.
L = LOW voltage level.
X = don't care.
↑ = positive-going transition.

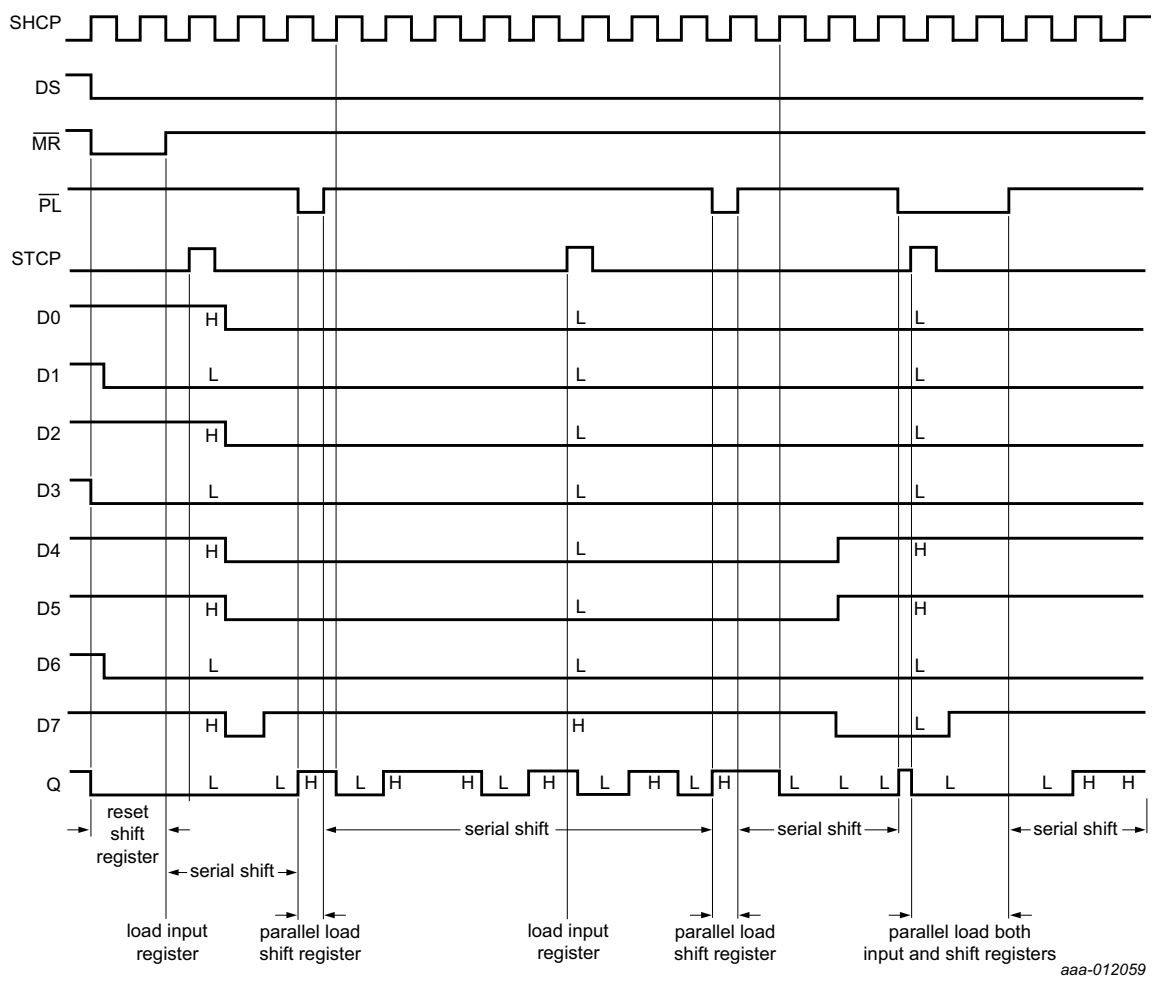


Fig 7. Timing diagram

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		−0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	-	±20	mA
I_O	output current	$V_O = -0.5$ V to $(V_{CC} + 0.5$ V)	-	±25	mA
I_{CC}	supply current		-	+50	mA
I_{GND}	ground current		−50	-	mA
T_{stg}	storage temperature		−65	+150	°C
P_{tot}	total power dissipation	DIP16 package [1]	-	750	mW
		SO16, SSOP16 and TSSOP16 packages [2]	-	500	mW

[1] For DIP16 package: P_{tot} derates linearly with 12 mW/K above 70 °C.

[2] For SO16: P_{tot} derates linearly with 8 mW/K above 70 °C.
For SSOP16 and TSSOP16 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC597			74HCT597			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		−40	+25	+125	−40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0$ V	-	-	625	-	-	-	ns/V
		$V_{CC} = 4.5$ V	-	1.67	139	-	1.67	139	ns/V
		$V_{CC} = 6.0$ V	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC597										
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = −20 μA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I_O = −20 μA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = −20 μA; V_{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I_O = −4.0 mA; V_{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I_O = −5.2 mA; V_{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = 20 μA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	8.0	-	80.0	-	160.0	μA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF
74HCT597										
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V								
		I_O = −20 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = −4.0 mA	3.98	4.32	-	3.84	-	3.7	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V								
		I_O = 20 μA	-	0	0.1	-	0.1	-	0.1	V
		I_O = 4.0 mA	-	0.15	0.26	-	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 5.5 V	-	-	±0.1	-	±1.0	-	±1.0	μA

Table 6. Static characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	8.0	-	80.0	-	160.0	µA
ΔI_{CC}	additional supply current	$V_I = V_{CC} - 2.1$ V; other inputs at V_{CC} or GND; $V_{CC} = 4.5$ V to 5.5 V; $I_O = 0$ A								
		per input pin; DS input	-	25	90	-	112.5	-	122.5	µA
		per input pin; Dn inputs	-	30	108	-	135	-	147	µA
		per input pin; $\overline{PL}$, $\overline{MR}$ inputs	-	150	540	-	675	-	735	µA
		per input pin; STCP, SHCP inputs	-	150	540	-	675	-	735	µA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit, see Figure 14.

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC597										
t_{pd}	propagation delay	SHCP to Q; see Figure 8 [1]								
		$V_{CC} = 2.0$ V	-	55	175	-	220	-	265	ns
		$V_{CC} = 4.5$ V	-	20	35	-	44	-	53	ns
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	17	-	-	-	-	-	ns
		$V_{CC} = 6.0$ V	-	16	30	-	37	-	45	ns
		$\overline{MR}$ to Q; see Figure 9 [1]								
		$V_{CC} = 2.0$ V	-	58	175	-	220	-	265	ns
		$V_{CC} = 4.5$ V	-	21	35	-	44	-	53	ns
		$V_{CC} = 6.0$ V	-	17	30	-	37	-	45	ns
		STCP to Q; see Figure 8 [1]								
		$V_{CC} = 2.0$ V	-	80	250	-	315	-	375	ns
		$V_{CC} = 4.5$ V	-	29	50	-	63	-	75	ns
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	25	-	-	-	-	-	ns
		$V_{CC} = 6.0$ V	-	23	43	-	54	-	64	ns
		$\overline{PL}$ to Q; see Figure 10 [1]								
		$V_{CC} = 2.0$ V	-	69	215	-	270	-	325	ns
		$V_{CC} = 4.5$ V	-	25	43	-	54	-	65	ns
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	21	-	-	-	-	-	ns
		$V_{CC} = 6.0$ V	-	20	37	-	46	-	55	ns

Table 7. Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit, see Figure 14.

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_t	transition time	see Figure 10 [2]								
		V_{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V_{CC} = 6.0 V	-	6	13	-	16	-	19	ns
t_W	pulse width	STCP HIGH or LOW; see Figure 8								
		V_{CC} = 2.0 V	80	11	-	100	-	120	-	ns
		V_{CC} = 4.5 V	16	4	-	20	-	24	-	ns
		V_{CC} = 6.0 V	14	3	-	17	-	20	-	ns
		SHCP HIGH or LOW; see Figure 8								
		V_{CC} = 2.0 V	80	14	-	100	-	120	-	ns
		V_{CC} = 4.5 V	16	5	-	20	-	24	-	ns
		V_{CC} = 6.0 V	14	4	-	17	-	20	-	ns
		$\overline{MR}$ LOW; see Figure 9								
		V_{CC} = 2.0 V	80	22	-	100	-	120	-	ns
		V_{CC} = 4.5 V	16	8	-	20	-	24	-	ns
		V_{CC} = 6.0 V	14	6	-	17	-	20	-	ns
		$\overline{PL}$ LOW; see Figure 10								
		V_{CC} = 2.0 V	80	22	-	100	-	120	-	ns
		V_{CC} = 4.5 V	16	8	-	20	-	24	-	ns
		V_{CC} = 6.0 V	14	6	-	17	-	20	-	ns
t_{rec}	recovery time	$\overline{MR}$ to SHCP; see Figure 11								
		V_{CC} = 2.0 V	60	–3	-	75	-	90	-	ns
		V_{CC} = 4.5 V	12	–1	-	15	-	18	-	ns
		V_{CC} = 6.0 V	10	–1	-	13	-	15	-	ns

Table 7. Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit, see Figure 14.

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{su}	set-up time	Dn to STCP; see Figure 12								
		V_{CC} = 2.0 V	60	8	-	75	-	90	-	ns
		V_{CC} = 4.5 V	12	3	-	15	-	18	-	ns
		V_{CC} = 6.0 V	10	2	-	13	-	15	-	ns
		DS to SHCP; see Figure 12								
		V_{CC} = 2.0 V	60	11	-	75	-	90	-	ns
		V_{CC} = 4.5 V	12	4	-	15	-	18	-	ns
		V_{CC} = 6.0 V	10	3	-	13	-	15	-	ns
		$\overline{PL}$ to SHCP; see Figure 13								
		V_{CC} = 2.0 V	60	11	-	75	-	90	-	ns
		V_{CC} = 4.5 V	12	4	-	15	-	18	-	ns
		V_{CC} = 6.0 V	10	3	-	13	-	15	-	ns
t_h	hold time	Dn to STCP; see Figure 12								
		V_{CC} = 2.0 V	5	–3	-	5	-	5	-	ns
		V_{CC} = 4.5 V	5	–1	-	5	-	5	-	ns
		V_{CC} = 6.0 V	5	–1	-	5	-	5	-	ns
		$\overline{PL}$, DS to SHCP; see Figure 12								
		V_{CC} = 2.0 V	5	–6	-	5	-	5	-	ns
		V_{CC} = 4.5 V	5	–2	-	5	-	5	-	ns
		V_{CC} = 6.0 V	5	–2	-	5	-	5	-	ns
f_{max}	maximum frequency	SHCP; see Figure 8								
		V_{CC} = 2.0 V	6.0	29	-	4.8	-	4.0	-	MHz
		V_{CC} = 4.5 V	30	87	-	24	-	20	-	MHz
		V_{CC} = 5.0 V; C_L = 15 pF	-	96	-	-	-	-	-	MHz
		V_{CC} = 6.0 V	35	104	-	28	-	24	-	MHz
C_{PD}	power dissipation capacitance	C_L = 50 pF; f = 1 MHz; V_I = GND to V_{CC} [3]	-	29	-	-	-	-	-	pF

Table 7. Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit, see Figure 14.

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HCT597										
t_{pd}	propagation delay	SHCP to Q; see Figure 8 [1]								
		V_{CC} = 4.5 V	-	23	40	-	50	-	60	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	20	-	-	-	-	-	ns
		$\overline{MR}$ to Q; see Figure 9 [1]								
		V_{CC} = 4.5 V	-	28	49	-	61	-	74	ns
		STCP to Q; see Figure 8 [1]								
		V_{CC} = 4.5 V	-	33	57	-	71	-	86	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	29	-	-	-	-	-	ns
		$\overline{PL}$ to Q; see Figure 10 [1]								
		V_{CC} = 4.5 V	-	30	52	-	65	-	78	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	26	-	-	-	-	-	ns
t_t	transition time	see Figure 8 [2]								
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns
t_W	pulse width	STCP HIGH or LOW; see Figure 8								
		V_{CC} = 4.5 V	16	6	-	20	-	24	-	ns
		SHCP HIGH or LOW; see Figure 8								
		V_{CC} = 4.5 V	16	7	-	20	-	24	-	ns
		$\overline{MR}$ LOW; see Figure 9								
		V_{CC} = 4.5 V	25	14	-	31	-	38	-	ns
		$\overline{PL}$ LOW; see Figure 10								
		V_{CC} = 4.5 V	20	10	-	25	-	30	-	ns
t_{rec}	recovery time	$\overline{MR}$ to SHCP; see Figure 11								
		V_{CC} = 4.5 V	12	–2	-	15	-	18	-	ns
t_{su}	set-up time	Dn to STCP; see Figure 12								
		V_{CC} = 4.5 V	12	5	-	15	-	18	-	ns
		DS to SHCP; see Figure 12								
		V_{CC} = 4.5 V	12	2	-	15	-	18	-	ns
		$\overline{PL}$ to SHCP; see Figure 13								
		V_{CC} = 4.5 V	12	4	-	15	-	18	-	ns

Table 7. Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit, see Figure 14.

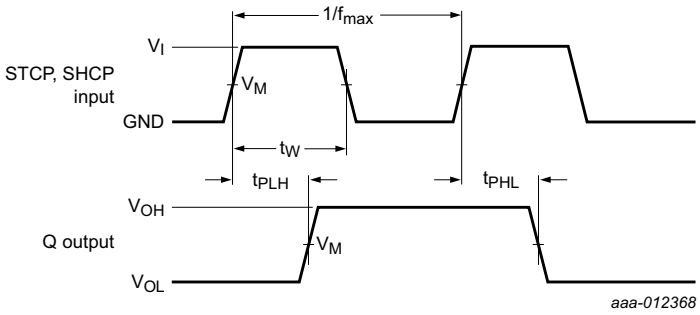
Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_h	hold time	Dn to STCP; see Figure 12								
		V_{CC} = 4.5 V	5	–1	-	5	-	5	-	ns
		$\overline{PL}$, DS to SHCP; see Figure 12								
		V_{CC} = 4.5 V	5	–2	-	5	-	5	-	ns
f_{max}	maximum frequency	SHCP; see Figure 8								
		V_{CC} = 4.5 V	30	75	-	24	-	20	-	MHz
		V_{CC} = 5.0 V; C_L = 15 pF	-	83	-	-	-	-	-	MHz
C_{PD}	power dissipation capacitance	C_L = 50 pF; f = 1 MHz; V_I = GND to V_{CC} – 1.5 V [3]	-	32	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.

[2] t_t is the same as t_{THL} and t_{TLH}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

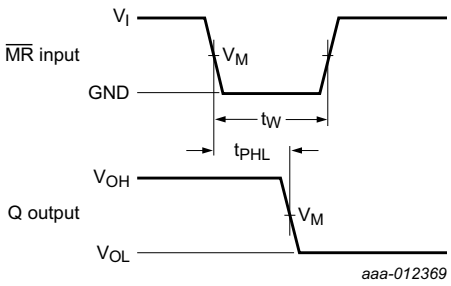
11. Waveforms



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

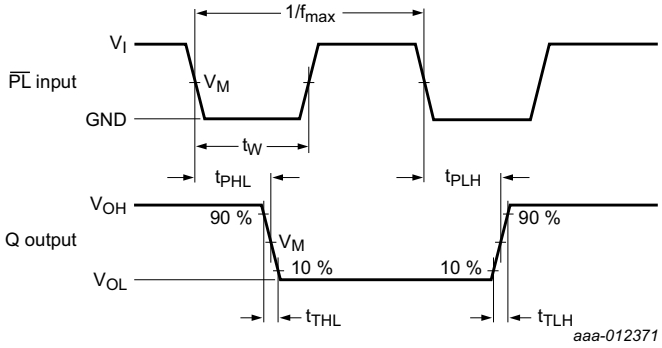
Fig 8. Shift clock and storage clock inputs to output, propagation delays, pulse widths and maximum clock frequency



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

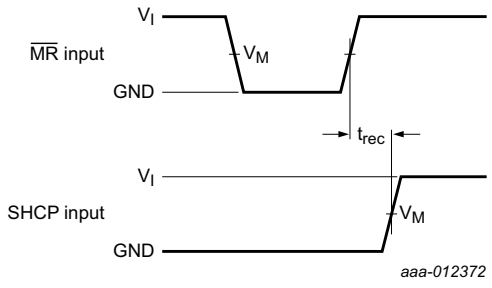
Fig 9. input ($\overline{MR}$) to (Q), output propagation delays and ($\overline{MR}$) pulse width



Measurement points are given in Table 8.

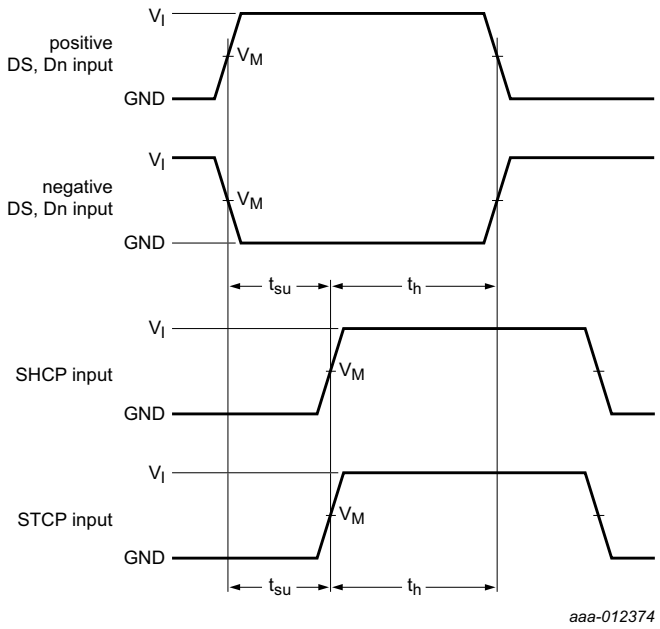
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 10. Input ($\overline{PL}$) to (Q), output propagation delays, $\overline{PL}$ pulse width and output transition times



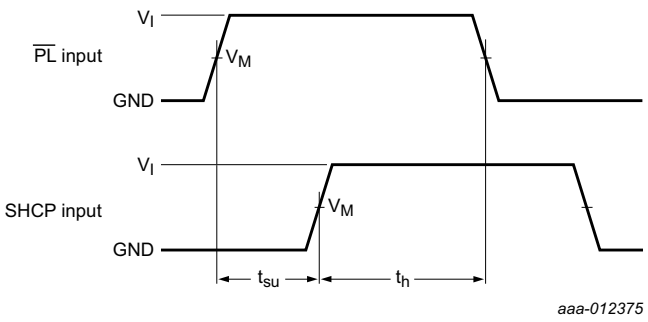
Measurement points are given in Table 8.

Fig 11. Input ($\overline{MR}$) to shift clock (SHCP) and storage clock (STCP) recovery times



Measurement points are given in Table 8.

Fig 12. Hold and set-up times for (DS), (Dn) inputs to (SHCP), (STCP) inputs

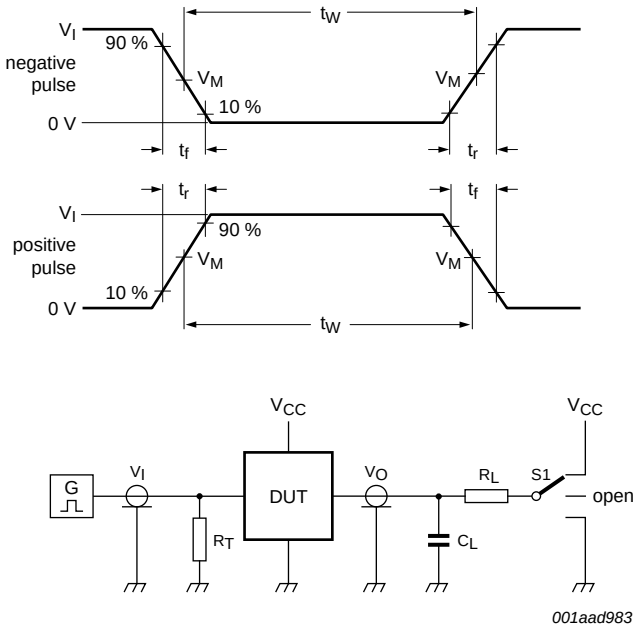


Measurement points are given in Table 8.

Fig 13. Set-up times for ($\overline{PL}$) input to (SHCP) input

Table 8. Measurement points

Type	Input		Output
	V_M	V_I	V_M
74HC597	$0.5 \times V_{CC}$	GND to V_{CC}	$0.5 \times V_{CC}$
74HCT597	1.3 V	GND to 3 V	1.3 V



Test data is given in Table 9.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

S1 = Test selection switch.

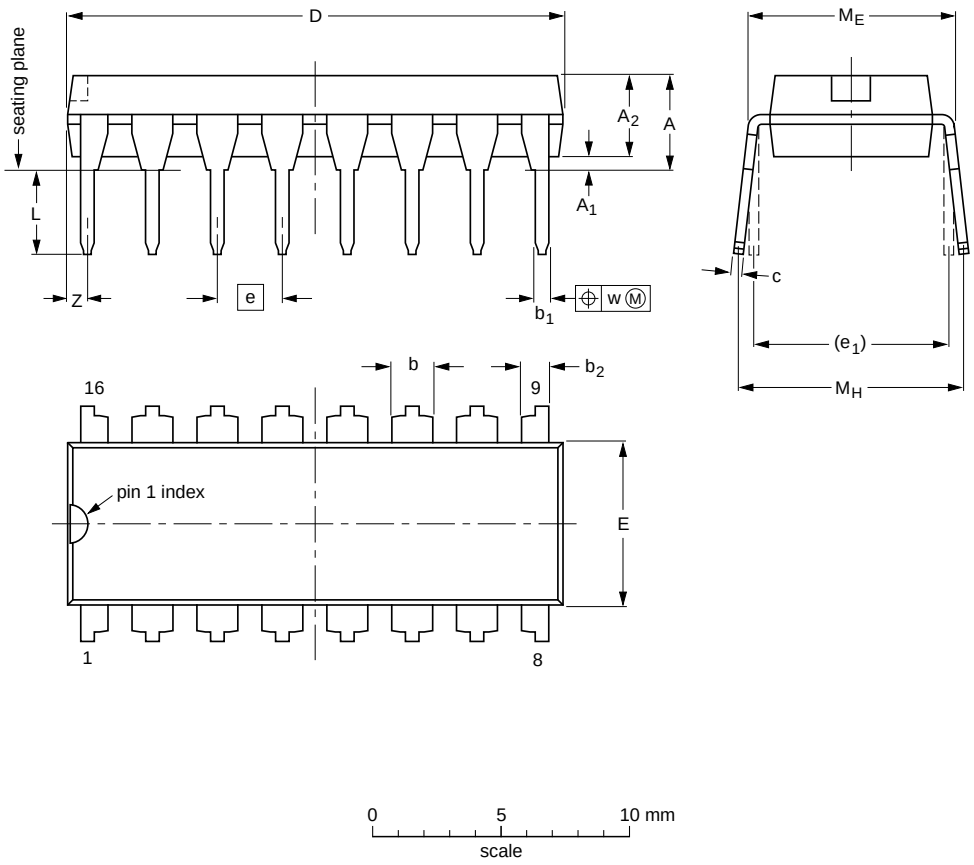
Fig 14. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load		S1 position		
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74HC597	V_{CC}	6 ns	15 pF, 50 pF	1 kΩ	open	GND	V_{CC}
74HCT597	3 V	6 ns	15 pF, 50 pF	1 kΩ	open	GND	V_{CC}

12. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil) **SOT38-4**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.03

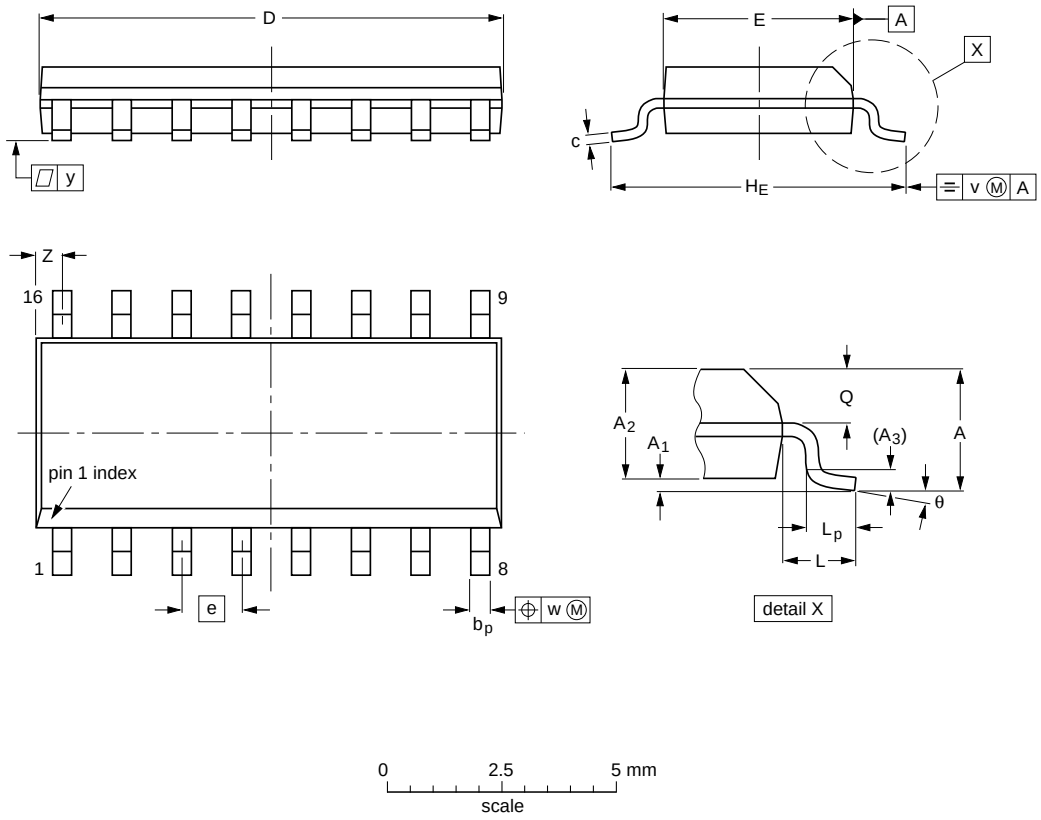
Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT38-4						~~95-01-14~~ 03-02-13

Fig 15. Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

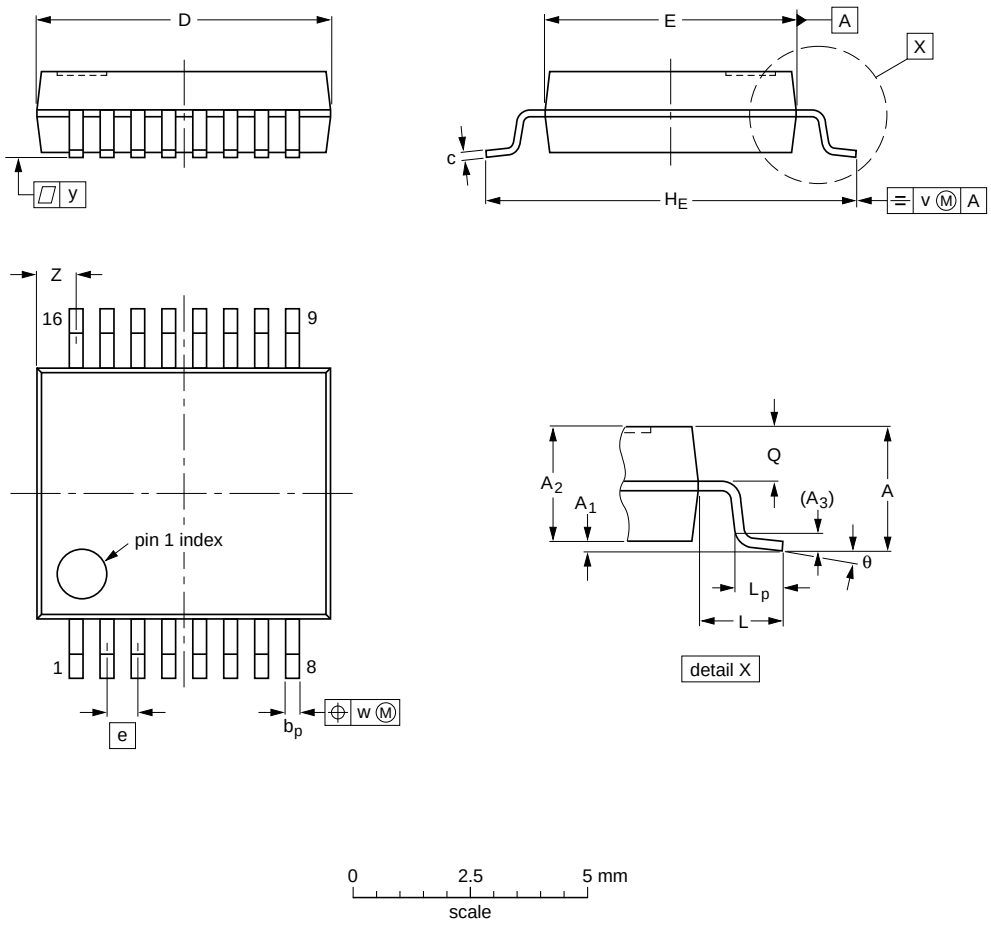
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 16. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8^o 0^o

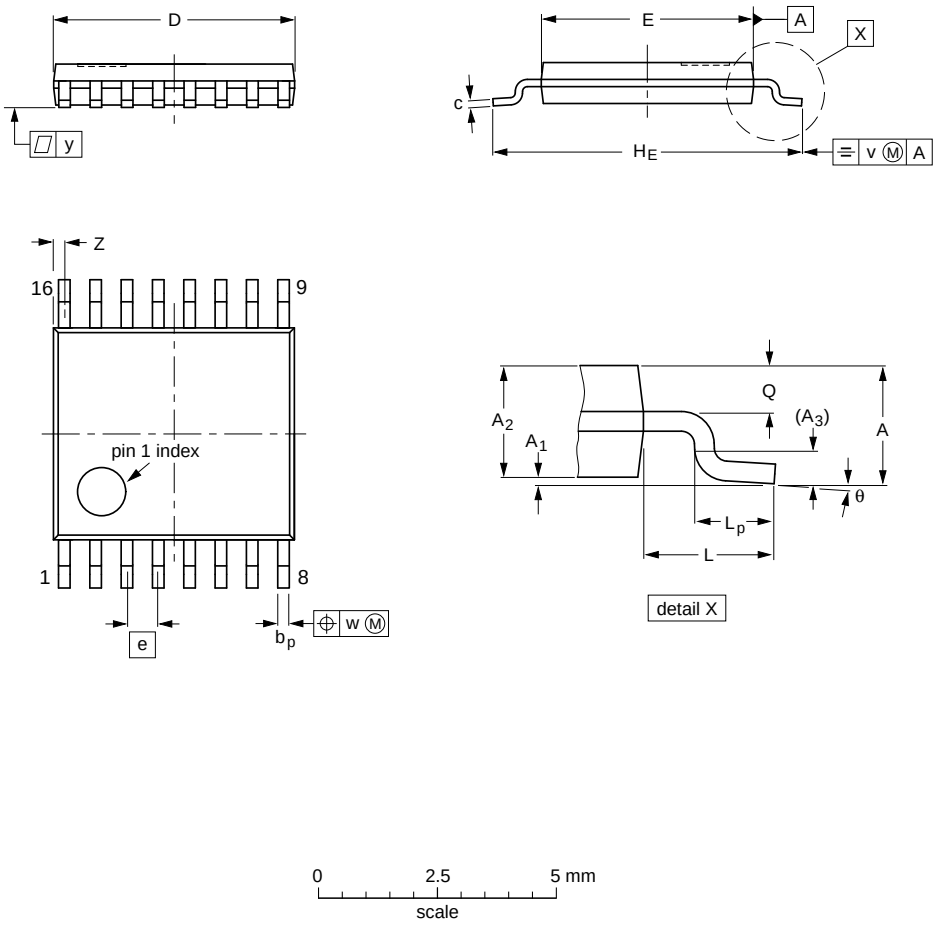
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT338-1		MO-150				~~99-12-27~~ 03-02-19

Fig 17. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 18. Package outline SOT403-1 (TSSOP16)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT597 v.3	20140415	Product data sheet	-	74HC_HCT597_CNV v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate.			
74HC_HCT597_CNV v.2	19901201	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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17. Contents

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