74HC04; 74HCT04

Hex inverter

Rev. 5 — 27 November 2015

Product data sheet

1. General description

The 74HC04; 74HCT04 is a hex inverter. The inputs include clamp diodes that enable the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

2. Features and benefits

- Complies with JEDEC standard JESD7A
- Input levels:
 - ♦ For 74HC04: CMOS level
 - ◆ For 74HCT04: TTL level
- ESD protection:
 - ♦ HBM JESD22-A114F exceeds 2000 V
 - ♦ MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from –40 °C to +85 °C and from –40 °C to +125 °C

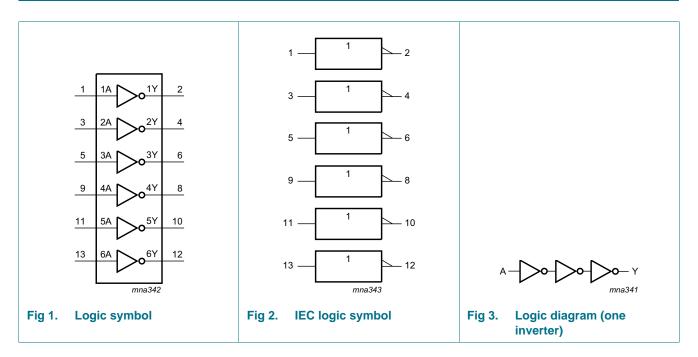
3. Ordering information

Table 1. Ordering information

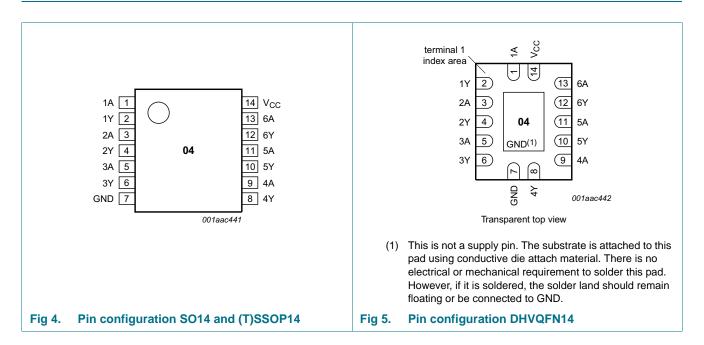
Type number	Package				
	Temperature range	Name	Description	Version	
74HC04D	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width	SOT108-1	
74HCT04D			3.9 mm		
74HC04DB	-40 °C to +125 °C	SSOP14	plastic shrink small outline package; 14 leads; body	SOT337-1	
74HCT04DB			width 5.3 mm		
74HC04PW	–40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads;	SOT402-1	
74HCT04PW			body width 4.4 mm		
74HC04BQ	−40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very	SOT762-1	
74HCT04BQ			thin quad flat package; no leads; 14 terminals; body $2.5 \times 3 \times 0.85$ mm		



4. Functional diagram



5. Pinning information



5.1 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A, 5A, 6A	1, 3, 5, 9, 11, 13	data input
1Y, 2Y, 3Y, 4Y, 5Y, 6Y	2, 4, 6, 8, 10, 12	data output
GND	7	ground (0 V)
V _{CC}	14	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level

Input	Output
nA	nY
L	Н
Н	L

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{CC}	supply voltage			-0.5	+7	V
I _{IK}	input clamping current	$V_{I} < -0.5 \text{ V or } V_{I} > V_{CC} + 0.5 \text{ V}$	<u>[1]</u>	-	±20	mA
I _{OK}	output clamping current	$V_O < -0.5 \text{ V or } V_O > V_{CC} + 0.5 \text{ V}$	<u>[1]</u>	-	±20	mA
Io	output current	$-0.5 \text{ V} < \text{V}_{\text{O}} < \text{V}_{\text{CC}} + 0.5 \text{ V}$		-	±25	mA
I _{CC}	supply current			-	50	mA
I _{GND}	ground current			-50	-	mA
T _{stg}	storage temperature			-65	+150	°C
P _{tot}	total power dissipation	SO14, (T)SSOP14 and DHVQFN14 packages	[2]	-	500	mW

^[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SO14 package: P_{tot} derates linearly with 8 mW/K above 70 $^{\circ}\text{C}.$

For (T)SSOP14 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

For DHVQFN14 packages: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	ons 74HC04		74HCT04			Unit	
			Min	Тур	Max	Min	Тур	Max	_
V _{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
VI	input voltage		0	-	V _{CC}	0	-	V _{CC}	V
Vo	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V _{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V _{CC} = 6.0 V	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C		–40 °C t	o +85 °C	–40 °C t	o +125 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	
74HC04										
V _{IH}	HIGH-level	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
	input voltage	V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
	input voltage	V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		$V_{CC} = 6.0 \text{ V}$	-	2.8	1.8	-	1.8	-	1.8	V
V _{OH} HIGH-level	$V_I = V_{IH}$ or V_{IL}									
	output voltage	$I_{O} = -20 \mu A; V_{CC} = 2.0 V$	1.9	2.0	-	1.9	-	1.9	-	V
		$I_{O} = -20 \mu A; V_{CC} = 4.5 V$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -20 \mu A; V_{CC} = 6.0 V$	5.9	6.0	-	5.9	-	5.9	-	V
		$I_O = -4.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	3.98	4.32	-	3.84	-	3.7	-	V
		$I_{O} = -5.2 \text{ mA}; V_{CC} = 6.0 \text{ V}$	5.48	5.81	-	5.34	-	5.2	-	V
V _{OL}	LOW-level	$V_I = V_{IH}$ or V_{IL}								
	output voltage	$I_O = 20 \mu A; V_{CC} = 2.0 V$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 20 \mu A; V_{CC} = 4.5 V$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 20 \mu A; V_{CC} = 6.0 \text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 4.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	0.15	0.26	-	0.33	-	0.4	V
		$I_O = 5.2 \text{ mA}; V_{CC} = 6.0 \text{ V}$	-	0.16	0.26	-	0.33	-	0.4	V
lı	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0 \text{ V}$	-	-	±0.1	-	±1	-	±1	μΑ
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0 \text{ V}$	-	-	2	-	20	-	40	μΑ

 Table 6.
 Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C		–40 °C t	o +85 °C	-40 °C to	o +125 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	
Cı	input capacitance		-	3.5	-	-	-	-	-	pF
74HCT0	4					1	1	1		
V_{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 \text{ V}$								
		$I_{O} = -20 \mu A$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_{O} = -4.0 \text{ mA}$	3.84	4.32	-	3.84	-	3.7	-	V
V _{OL}	LOW-level	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 \text{ V}$								
	output voltage	I _O = 20 μA	-	0	0.1	-	0.1	-	0.1	V
		I _O = 5.2 mA	-	0.15	0.26	-	0.33	-	0.4	V
l _l	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$	-	-	±0.1	-	±1	-	±1	μΑ
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	2	-	20	-	40	μΑ
Δl _{CC}	additional supply current	per input pin; $V_{I} = V_{CC} - 2.1 \text{ V; } I_{O} = 0 \text{ A;}$ other inputs at V_{CC} or GND; $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	120	432	-	540	-	590	μА
Cı	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

 $GND = 0 \ V; \ C_L = 50 \ pF;$ for test circuit see <u>Figure 7</u>.

Symbol	Parameter	Conditions			25 °C		–40 °C to	+125 °C	Unit
			Mir	n	Тур	Max	Max (85 °C)	Max (125 °C)	
74HC04									
t _{pd}	propagation delay	nA to nY; see Figure 6	1						
		V _{CC} = 2.0 V	-		25	85	105	130	ns
		V _{CC} = 4.5 V	-		9	17	21	26	ns
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-		7	-	-	-	ns
		V _{CC} = 6.0 V	-		7	14	18	22	ns
t _t	transition time	see Figure 6]						
		V _{CC} = 2.0 V	-		19	75	95	110	ns
		V _{CC} = 4.5 V	-		7	15	19	22	ns
		V _{CC} = 6.0 V	-		6	13	16	19	ns

Table 7. Dynamic characteristics ...continued GND = 0 V; $C_L = 50$ pF; for test circuit see <u>Figure 7</u>.

Symbol	Parameter	Conditions			25 °C		-40 °C to	+125 °C	Unit
				Min	Тур	Max	Max (85 °C)	Max (125 °C)	
C _{PD}	power dissipation capacitance	per package; $V_I = GND$ to V_{CC}	[3]	-	21	-	-	-	pF
74HCT04	ı								
t _{pd}	propagation delay	nA to nY; see Figure 6	[1]						
		V _{CC} = 4.5 V		-	10	19	24	29	ns
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$		-	8	-	-	-	ns
t _t	transition time	V _{CC} = 4.5 V; see <u>Figure 6</u>	[2]	-	7	15	19	22	ns
C _{PD}	power dissipation capacitance	per package; V _I = GND to V _{CC} – 1.5 V	[3]	-	24	-	-	-	pF

- [1] t_{pd} is the same as t_{PHL} and t_{PLH} .
- [2] t_t is the same as t_{THL} and t_{TLH} .
- [3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

 $P_D = C_{PD} \times V_{CC}{}^2 \times f_i \times N + \sum \left(C_L \times V_{CC}{}^2 \times f_o \right)$ where:

 f_i = input frequency in MHz;

f_o = output frequency in MHz;

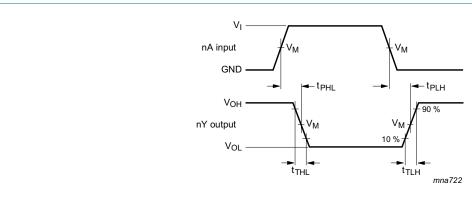
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

 $\sum (C_L \times V_{CC}^2 \times f_o) = \text{sum of outputs.}$

11. Waveforms



Measurement points are given in Table 8.

 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 6. The input (nA) to output (nY) propagation delay times

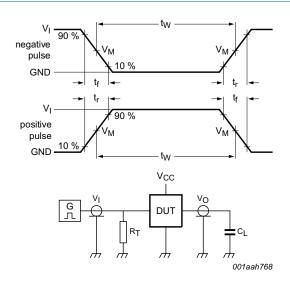
Table 8. Measurement points

Туре	Input	Output		
	V _M	V _M		
74HC04	0.5V _{CC}	0.5V _{CC}		
74HCT04	1.3 V	1.3 V		

74HC_HCT04

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Test data is given in Table 9.

Definitions test circuit:

 R_T = termination resistance should be equal to output impedance Z_0 of the pulse generator.

 C_L = load capacitance including jig and probe capacitance.

Fig 7. Test circuit for measuring switching times

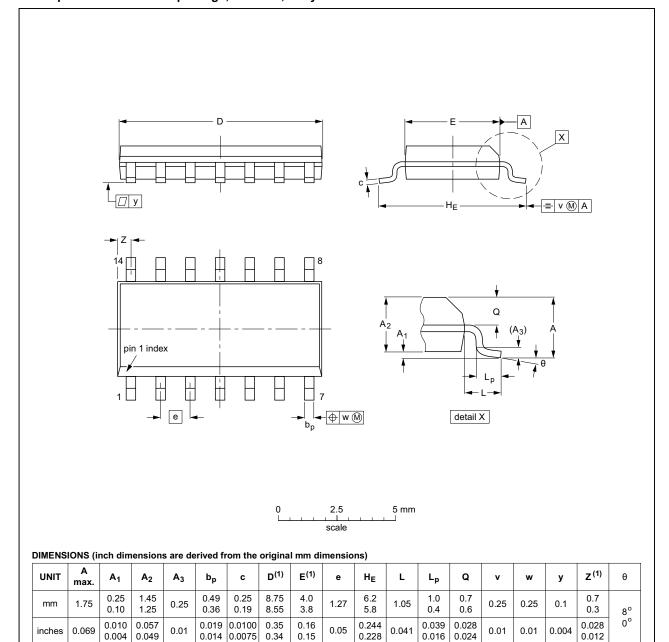
Table 9. Test data

Туре	Input L		Load	Test
	VI	t _r , t _f	CL	
74HC04	V _{CC}	6.0 ns	15 pF, 50 pF	t _{PLH} , t _{PHL}
74HCT04	3.0 V	6.0 ns	15 pF, 50 pF	t _{PLH} , t _{PHL}

12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

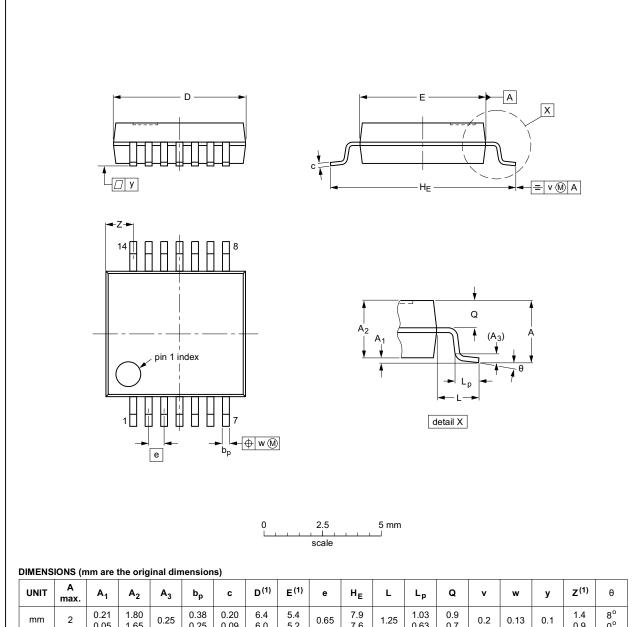
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SOT108-1	076E06	MS-012				99-12-27 03-02-19

Fig 8. Package outline SOT108-1 (SO14)

74HC_HCT04

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1



UNIT	A max.	A ₁	A ₂	A ₃	b _p	C	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

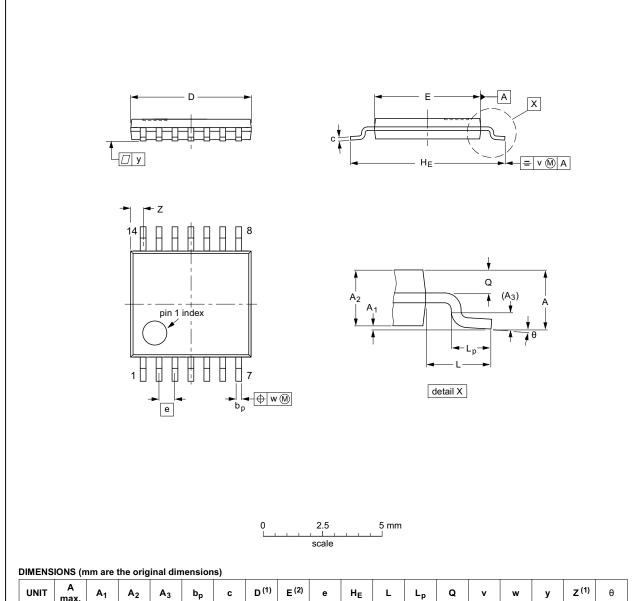
OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE	
SOT337-1		MO-150				99-12-27 03-02-19	

Package outline SOT337-1 (SSOP14) Fig 9.

74HC_HCT04

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



LINUT	Α `						D (1)	E (2)	_	l							- (1)	
UNIT	max.	A ₁	A ₂	А3	р	С	ייע	E (-/	е	HE	L	Lp	Q	V	w	У	Z (·)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

(OUTLINE		REFER	EUROPEAN	ISSUE DATE				
\ \ \	VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE		
S	SOT402-1		MO-153				99-12-27 03-02-18		
8	SOT402-1		MO-153				∌		

Fig 10. Package outline SOT402-1 (TSSOP14)

74HC_HCT04

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body $2.5 \times 3 \times 0.85$ mm

SOT762-1

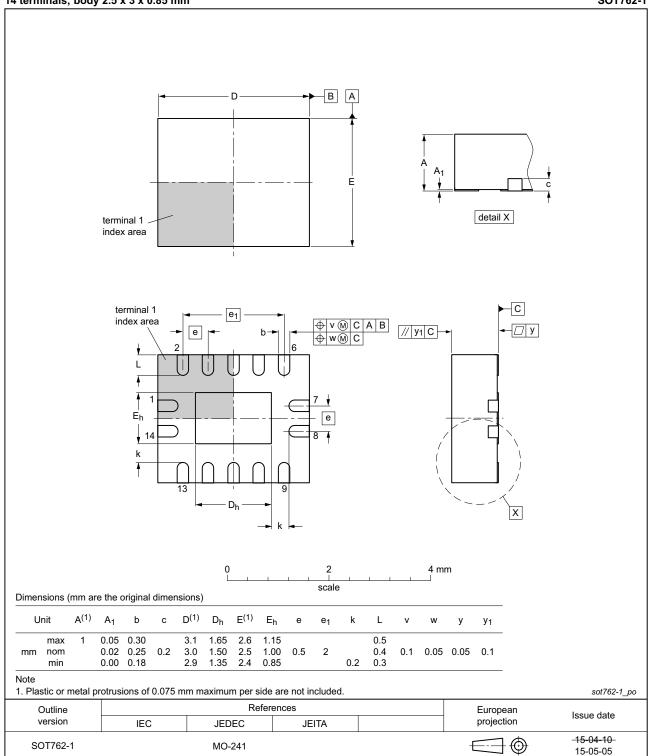


Fig 11. Package outline SOT762-1 (DHVQFN14)

74HC_HCT04

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes				
74HC_HCT04 v.5	20151127	Product data sheet	-	74HC_HCT04 v.4				
Modifications:	Type numbers	s 74HC04N and 74HCT04N (S	OT27-1) removed.					
74HC_HCT04 v.4	20120803	Product data sheet	-	74HC_HCT04 v.3				
Modifications:		 The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. 						
	 Legal texts have been adapted to the new company name where appropriate. 							
74HC_HCT04 v.3	20030723	Product data sheet	-	74HC_HCT04_CNV v.2				
74HC_HCT04_CNV v.2	19970826	Product specification	-	-				

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15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
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74HC_HCT04

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17. Contents

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