74F125

Quad buffers; 3-State

Rev. 4 — 23 January 2013 Product data sheet

1. General description

The 74F125 provides four non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs (nY) are controlled by the output enable input ($n\overline{OE}$). A HIGH at $n\overline{OE}$ causes the outputs to assume a high-impedance OFF-state.

2. Features and benefits

- High impedance NPN base inputs for reduced loading (20 μA in HIGH and LOW states)

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
N74F125N	0 °C to +70 °C	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1
N74F125D	0 °C to +70 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1

4. Functional diagram

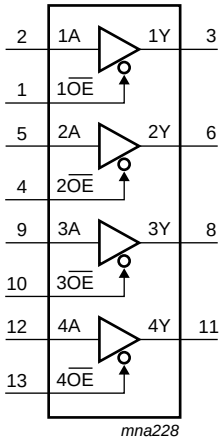


Fig 1. Logic symbol

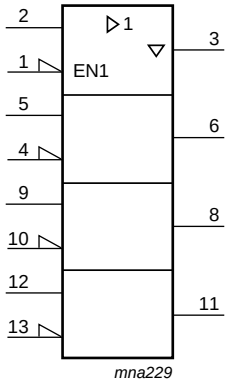


Fig 2. IEC logic symbol

5. Pinning information

5.1 Pinning

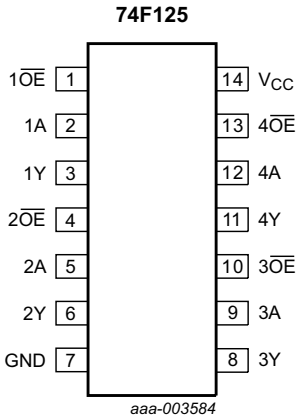


Fig 3. Pin configuration DIP14 and SO14 package

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description	Unit load HIGH/LOW	Load value[1] HIGH/LOW
$1\overline{OE}$ to $4\overline{OE}$	1, 4, 10, 13	output enable input (active LOW)	1.0/0.033	20 μA/20 μA
1A to 4A	2, 5, 9, 12	data input	1.0/0.033	20 μA/20 μA
1Y to 4Y	3, 6, 8, 11	data output	750/106.7	15 mA/64 mA
GND	7	ground (0 V)	-	-
V_{CC}	14	supply voltage	-	-

[1] One FAST Unit Load (UL) is defined as 20 μA in HIGH state, 0.6 μA in LOW state.

6. Functional description

Table 3. Function table[1]

Control	Input	Output
$n\overline{OE}$	nA	nY
L	L	L
	H	H
H	X	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			−0.5	+7.0	V
V_I	input voltage		[1]	−0.5	+7.0	V
V_O	output voltage	output in HIGH-state	[1]	−0.5	V_{CC}	V
I_{IK}	input clamping current	$V_I < 0$ V		−30	+5	mA
I_O	output current	output in LOW-state		-	128	mA
T_{amb}	ambient temperature	in free air	[2]	0	70	°C
T_{stg}	storage temperature			−65	+150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
I_{IK}	input clamping current		–18	-	-	mA
I_{OH}	HIGH-level output current		–15	-	-	mA
I_{OL}	LOW-level output current		-	-	64	mA
T_{amb}	ambient temperature		0		70	°C

9. Static characteristics

Table 6. Static characteristics

Symbol	Parameter	Conditions	25 °C			0 °C to +70 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{IK}	input clamping voltage	V_{CC} = 4.5 V; I_{IK} = –18 mA	–1.2	–0.73	-	–1.2	-	V
V_{OH}	HIGH-level output voltage	V_{CC} = 4.5 V; V_{IL} = 0.8 V; V_{IH} = 2.0 V						
		I_{OH} = –3 mA						
		V_{CC} = ±10 %	-	-	-	2.4	-	V
		V_{CC} = ±5 %	-	3.3	-	2.7	-	V
		I_{OH} = –15 mA						
		V_{CC} = ±10 %	-	-	-	2.0	-	V
V_{OL}	LOW-level output voltage	V_{CC} = 4.5 V; V_{IL} = 0.8 V; V_{IH} = 2.0 V						
		I_{OL} = 64 mA						
		V_{CC} = ±10 %	-	-	-	-	0.55	V
		V_{CC} = ±5 %	-	0.42	-	-	0.55	V
I_I	input leakage current	V_{CC} = 0 V; V_I = 7.0 V	-	-	-	-	100	µA
I_{IH}	HIGH-level input current	V_{CC} = 5.5 V; V_I = 2.7 V	-	-	-	-	20	µA
I_{IL}	LOW-level input current	V_{CC} = 5.5 V; V_I = 0.5 V	-	-	-	–20	-	µA
I_{OZ}	OFF-state output current	V_{CC} = 5.5 V						
		V_O = 2.7 V	-	-	-	-	50	µA
		V_O = 0.5 V	-	-	-	–50	-	µA
I_O	output current	V_{CC} = 5.5 V [2]	-	-	-	–225	–100	mA
I_{CC}	supply current	V_{CC} = 5.5 V; V_I = GND or V_{CC}						
		outputs HIGH-state	-	17	-	-	24	mA
		outputs LOW-state	-	28	-	-	40	mA
		outputs OFF-state	-	25	-	-	35	mA

[1] All typical values are measured at V_{CC} = 5 V.

[2] No more than one output should be tested at a time, and the duration of the test should not exceed one second.

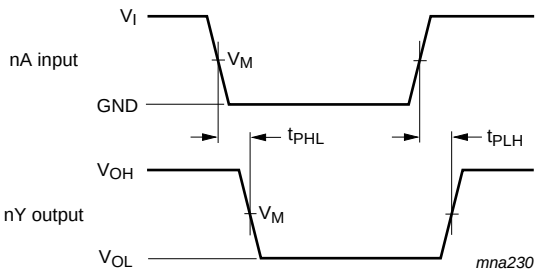
10. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V. Test circuit is shown in Figure 6.

Symbol	Parameter	Conditions	25 °C; V_{CC} = 5.0 V			0 °C to +70 °C; V_{CC} = 5.0 V ± 0.5 V		Unit
			Min	Typ	Max	Min	Max	
t_{PLH}	LOW to HIGH propagation delay	nA to nY, see Figure 4	2.0	4.0	6.0	2.0	6.5	ns
t_{PHL}	HIGH to LOW propagation delay	nA to nY; see Figure 4	3.0	5.5	7.5	3.0	8.0	ns
t_{PZH}	OFF-state to HIGH propagation delay	$n\overline{OE}$ to nY; see Figure 5	3.5	5.5	7.5	3.5	8.5	ns
t_{PZL}	OFF-state to LOW propagation delay	$n\overline{OE}$ to nY; see Figure 5	4.0	6.0	8.0	4.0	9.0	ns
t_{PHZ}	HIGH to OFF-state propagation delay	$n\overline{OE}$ to nY; see Figure 5	1.5	3.5	5.0	1.5	6.0	ns
t_{PLZ}	LOW to OFF-state propagation delay	$n\overline{OE}$ to nY; see Figure 5	1.5	3.5	5.5	1.5	6.0	ns

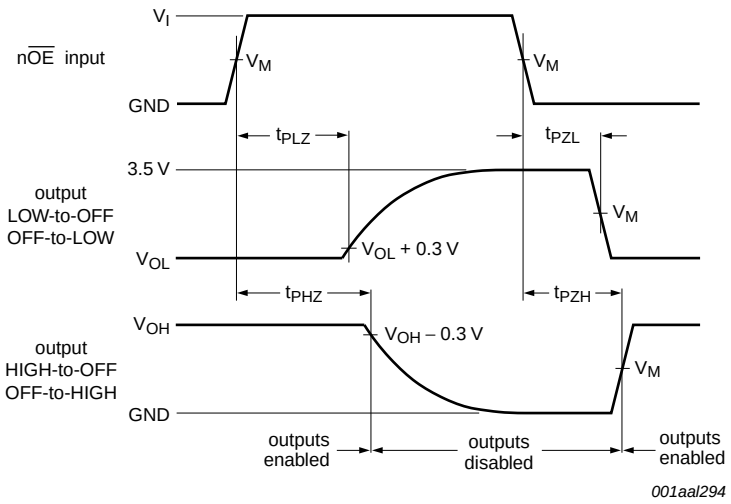
11. Waveforms



V_M = 1.5 V

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

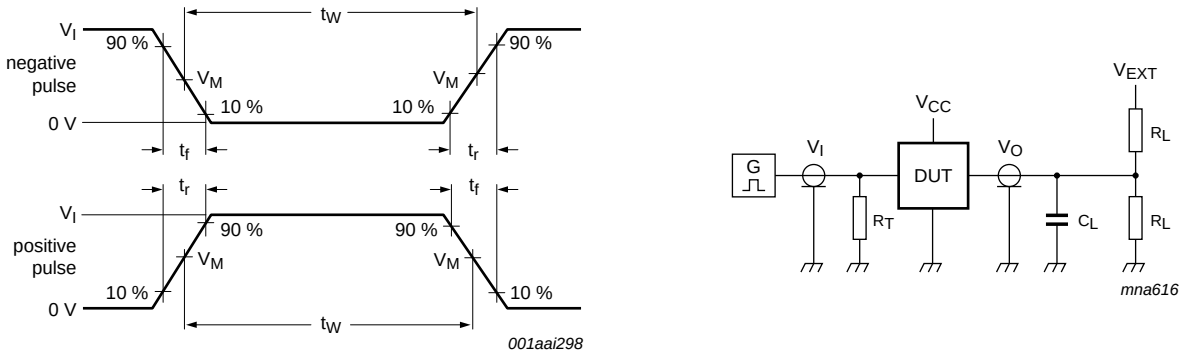
Fig 4. Propagation delay input (nA) to output (nY)



V_M = 1.5 V

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 5. Enable and disable times



a. Input pulse definition

b. Test circuit

Test data is given in Table 8.

Test circuit definitions:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = Test voltage for switching times.

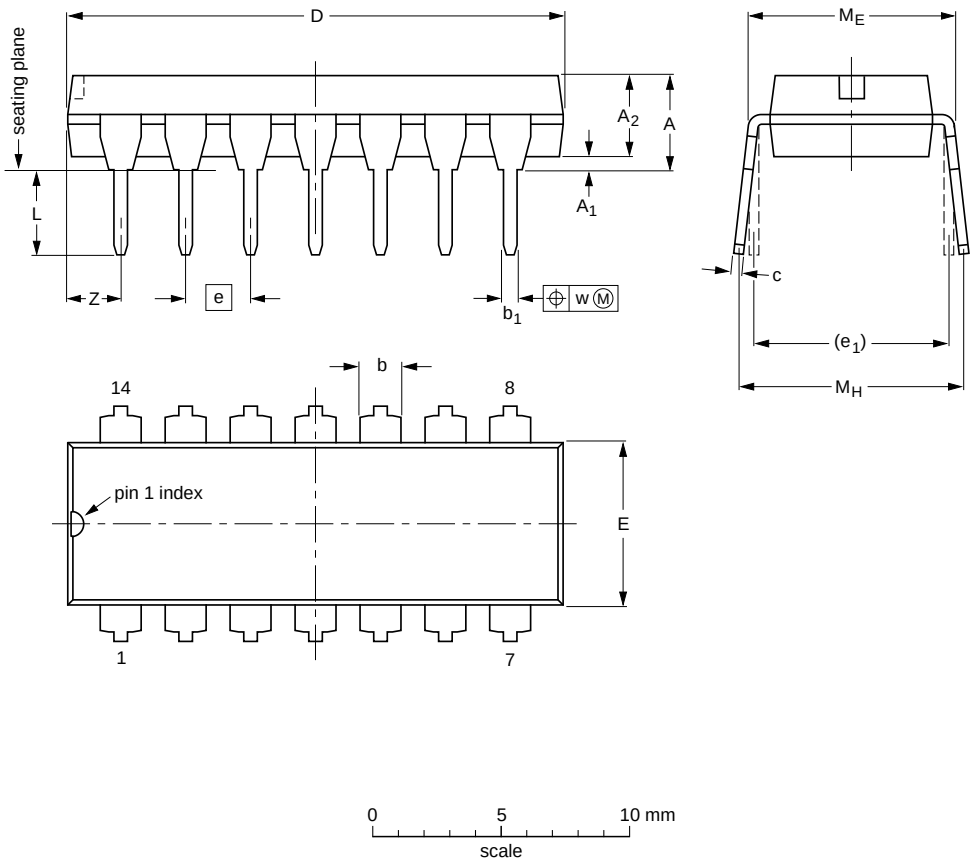
Fig 6. Load circuitry for switching times

Table 8. Test data

Input				Load		V_{EXT}		
V_I	f_i	t_W	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
3.0 V	1 MHz	500 ns	≤ 2.5 ns	50 pF	500 Ω	open	open	7.0 V

12. Package outline

DIP14: plastic dual in-line package; 14 leads (300 mil) **SOT27-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.02	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

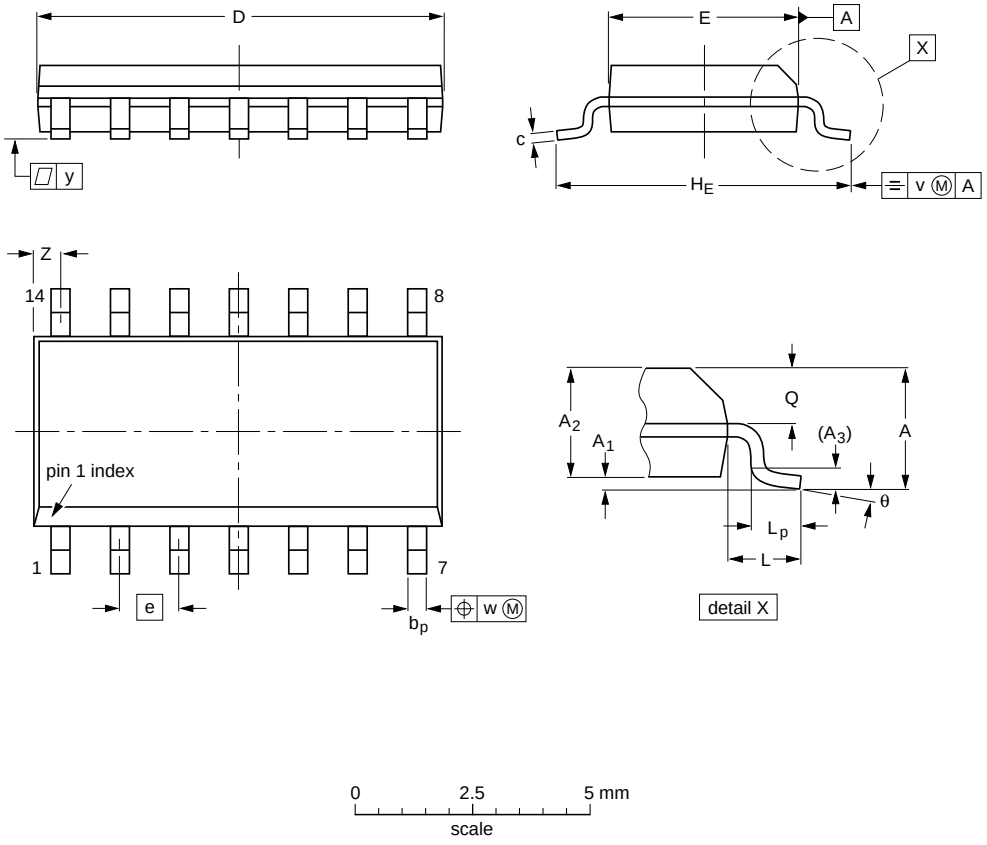
Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT27-1	050G04	MO-001	SC-501-14			~~99-12-27~~ 03-02-13

Fig 7. Package outline SOT27-1 (DIP14)

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Fig 8. Package outline SOT108-1 (SO14)

13. Abbreviations

Table 9. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
LSTTL	Low-power Schottky Transistor-Transistor Logic
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
CDM	Charge-Device Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74F125 v.4	20130123	Product data sheet	-	74F125 v.3
Modifications:	• Features and benefits: Changed mA into μA (errata).			
74F125 v.3	20130118	Product data sheet	-	74F125 v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate.			
74F125 v.2	19890328	Product data sheet	-	74F125 v.1

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15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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17. Contents

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