Panasonic

NN30295A

http://www.semicon.panasonic.co.jp/en/

6 A Synchronous DC-DC Step down Regulator with I²C Interface (V_{IN} = 4.5 V to 5.6 V, V_{OUT} = 0.6 V to 3.5 V)

FEATURES

- High-Speed Response DC-DC Step Down Regulator Circuit that employs Hysteretic Control System
- Integrated two 25 mΩ (Typ) MOSFETs for High Efficiency at 6 A
- Mode Selection Option via I²C:
  (1) Pulse Skip Mode (PSM) with coast mode function for high efficiency at light load
  (2) Forced Continuous Conduction Mode (FCCM) for quick load transient response
- Maximum Output Current : 6A
- Input Voltage Range : AV_{IN} : 4.5 V to 5.6 V,
  PV_{IN} : 3.1 V to 5.6 V, VDD : 1.7 V to 3.3 V
  Output Voltage Range : 0.6 V to 3.5 V
  Selectable Switching Frequency 500 kHz to 2 MHz
  (7 steps) using I²C : Default 1 MHz
- Adjustable Soft Start
- Low Operating and Standby Quiescent Current
- Open Drain Power Good Indication for Output Over / Under Voltage
- Built-in Under Voltage Lock-Out (UVLO), Thermal Shut Down (TSD), Over Voltage Detection (OVD), Under Voltage Detection (UVD), Over Current Protection (OCP), Short Circuit Protection (SCP)
- 24 pin Plastic Quad Flat Non-leaded Package Heat Slug Down (QFN Type)
  (Size : 4 mm × 4 mm × 0.7 mm, 0.5 mm pitch)

DESCRIPTION

NN30295A is a synchronous DC-DC Step down Regulator (1-ch) comprising of a Controller IC and two power MOSFETs and employs a hysteretic control system.

This system responds rapidly to sudden variations in load current, thus maintaining the fluctuations in the output voltage to a minimum level. The system does not require external components for phase compensation.

Together with the use of capacitors with small capacitance, this IC realizes downsizing of the set and reduces to a great extent, the number of external parts required for the system.

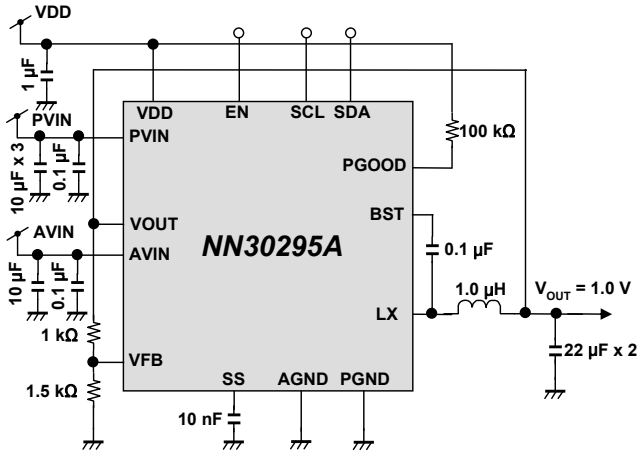
Output voltage is adjustable by user.
Maximum current is 6 A.

APPLICATIONS

High Current Distributed Power Systems such as :

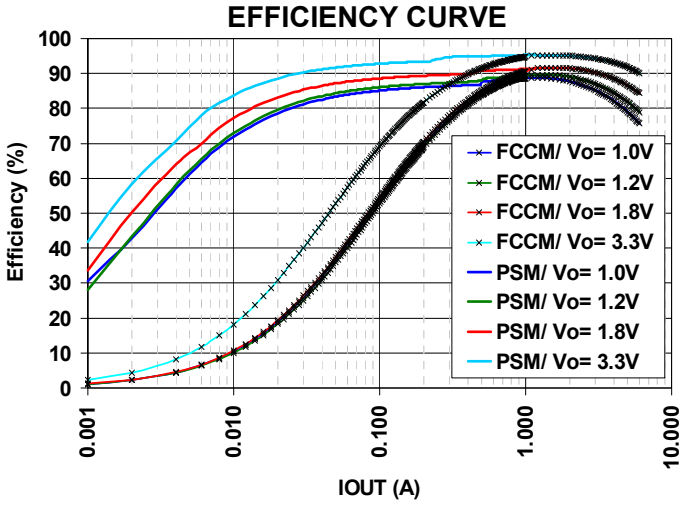
- HDDs (Hard Disk Drives)
- SSDs (Solid State Drives)
- PCs
- Game consoles
- Servers
- Security Cameras
- Network TVs
- Home Appliances
- OA Equipment etc.

APPLICATION CIRCUIT EXAMPLE



Note : The application circuit is an example. The operation of the mass production set is not guaranteed. Sufficient evaluation and verification is required in the design of the mass production set. The Customer is fully responsible for the incorporation of the above illustrated application circuit in the design of the equipment.

EFFICIENCY CURVE



Condition:
V_{IN} = 5.0 V, V_{OUT} = 1.0 V, 1.2 V, 1.8 V, 3.3 V,
Lo = 1 µH, Co = 44 µF (22 µF x 2), f_{SW} = 0.5 MHz

Established : 2012-06-21
Revised : 2013-06-25

PRODUCT ORDER INFORMATION

Product Order Code	Features	Package	Packing
NN30295A-VB	Maximum Output Current : 6 A	24-Pin HQFN	Emboss Taping

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Notes
Supply voltage	V_{IN}	6.0	V	*1
	VDD	3.6	V	*1
Operating free-air temperature	T_{opr}	– 40 to + 85	°C	*2
Operating junction temperature	T_j	– 40 to + 150	°C	*2
Storage temperature	T_{stg}	– 55 to + 150	°C	*2
Input Voltage Range	V_{EN}, V_{OUT}, V_{FB}	– 0.3 to (V_{IN} + 0.3)	V	*1, *3
	V_{SCL}, V_{SDA}	– 0.3 to (VDD + 0.3)	V	*1, *3
Output Voltage Range	V_{LX}, V_{PGOOD}	– 0.3 to (V_{IN} + 0.3)	V	*1, *3
ESD	HBM	2	kV	—

Notes: Do not apply external currents and voltages to any pin not specifically mentioned above.
This product may sustain permanent damage if subjected to conditions higher than the above stated absolute maximum rating. This rating is the maximum rating and device operating at this range is not guaranteed as it is higher than our stated recommended operating range. When subjected under the absolute maximum rating for a long time, the reliability of the product may be affected. V_{IN} is the voltage for AVIN, PVIN.
$V_{IN} = AV_{IN} = PV_{IN}$. VDD is the voltage for VDD.
*1 : The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.
*2 : Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for T_a = 25 °C.
*3 : (V_{IN} + 0.3) V must not exceed 6 V. (VDD + 0.3) V must not exceed 3.6 V.

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POWER DISSIPATION RATING

Package	θ_{JA}	$\theta_{j\text{-}C}$	PD (Ta = 25 °C)	PD (Ta = 85 °C)	Notes
24 pin Plastic Quad Flat Non-leaded Package Heat Slug Down (QFN Type)	63.0 °C / W	8.6 °C / W	1.984 W	1.031 W	*1
	40.4 °C / W	6.1 °C / W	3.094 W	1.608 W	*2

Notes: For the actual usage, please refer to the P_D–T_a characteristics diagram in the package specification.
Follow the power supply voltage, load and ambient temperature conditions to ensure that there is enough margin and the thermal design does not exceed the allowable value.
*1 : Glass Epoxy Substrate (4 Layers) [50 × 50 × 0.8 t (mm)]
*2 : Glass Epoxy Substrate (4 Layers) with Thermal Via [50 × 50 × 1.57 t (mm)]

CAUTION

Although this IC has built-in ESD protection circuit, it may still sustain permanent damage if not handled properly. Therefore, proper ESD precautions are recommended to avoid electrostatic damage to the MOS gates.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage range	AV_{IN}	4.5	5.0	5.6	V	—
	PV_{IN}	3.1	5.0	5.6	V	—
	VDD	1.7	2.5	3.3	V	—
Input Voltage Range	V_{EN}	– 0.3	—	V_{IN} + 0.3	V	*1
	V_{SDA}	– 0.3	—	VDD + 0.3	V	*1
	V_{SCL}	– 0.3	—	VDD + 0.3	V	*1
Output Voltage Range	V_{LX}	– 0.3	—	V_{IN} + 0.3	V	*1
	V_{PGOOD}	– 0.3	—	V_{IN} + 0.3	V	*1

Note: Do not apply external currents and voltages to any pin not specifically mentioned above.
Voltage values, unless otherwise specified, are with respect to GND. GND is voltage for AGND, PGND.
AGND = PGND.
V_{IN} is voltage for pins AVIN, PVIN. AVIN = PVIN .

*1 : (V_{IN} + 0.3) V must not exceed 6 V. (VDD + 0.3) V must not exceed 3.6 V.

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ELECTRICAL CHARACTERISTICS

Co = 22 µF × 2, Lo= 1 µH, V_{OUT} Setting = 1.0 V, V_{IN} = AV_{IN} = PV_{IN} = 5 V, VDD = 2.5 V,
Switching Frequency = 1 MHz, Mode = Pulse Skip Mode (PSM),
T_a = 25 °C ± 2 °C unless otherwise specified.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Current Consumption							
Consumption current at active	I_{OPR}	V_{EN} = 5 V, I_{OUT} = 0 A R_{FB1} = 1.0 kΩ R_{FB2} = 1.5 kΩ	—	400	700	µA	—
Consumption current at standby	I_{STB}	V_{EN} = 0 V, I_{OUT} = 0 A	—	—	2	µA	—
Logic Pin Characteristics							
EN pin Low-level input voltage	V_{ENL}	—	– 0.3	—	0.3	V	—
EN pin High-level input voltage	V_{ENH}	—	1.5	—	V_{IN} + 0.3	V	—
EN pin leak current	I_{leakEN}	V_{EN} = 5 V	—	3.5	10.0	µA	—
VFB Characteristics							
VFB comparator threshold	V_{FBTH}	—	0.595	0.603	0.611	V	—
VFB pin leak current 1	I_{leakF1}	V_{FB} = 0 V	– 1	—	1	µA	—
VFB pin leak current 2	I_{leakF2}	V_{FB} = 3.6 V	– 1	—	1	µA	—
Under Voltage Lock Out (UVLO)							
PVIN UVLO trigger voltage	$V_{UVLODET1}$	PV_{IN} = 5 V to 0 V	2.45	2.60	2.75	V	—
PVIN UVLO hysteresis voltage	$V_{UVLOHYS1}$	PV_{IN} = 0 V to 5 V	50	200	350	mV	—
AVIN UVLO trigger voltage	$V_{UVLODET2}$	AV_{IN} = 5 V to 0 V	3.25	3.40	3.55	V	—
AVIN UVLO hysteresis voltage	$V_{UVLOHYS2}$	AV_{IN} = 0 V to 5 V	10	100	250	mV	—
VDD UVLO trigger voltage	$V_{UVLODET3}$	VDD = 3 V to 0 V	1.00	1.25	1.50	V	—
VDD UVLO recover voltage	$V_{UVLOHYS3}$	VDD = 0 V to 3 V	10	50	90	mV	—
PGOOD Characteristics							
PGOOD Threshold 1 (V_{FB} ratio for UVD detect)	V_{PGUV}	V_{PGOOD} : High to Low	78	85	92	%	—
PGOOD Hysteresis 1 (UVD Hysteresis)	ΔV_{PGUV}	V_{PGOOD} : Low to High	2	5	8	%	—
PGOOD Threshold 2 (V_{FB} ratio for OVD detect)	V_{PGOV}	V_{PGOOD} : High to Low	108	115	122	%	—
PGOOD Hysteresis 2 (OVD Hysteresis)	ΔV_{PGOV}	V_{PGOOD} : Low to High	2	5	8	%	—
PGOOD ON resistance	R_{PGOOD}	V_{EN} = 0 V	—	10	15	Ω	—

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ELECTRICAL CHARACTERISTICS (Continued)

Co = 22 µF × 2, Lo= 1 µH, V_{OUT} Setting = 1.0 V, V_{IN} = AV_{IN} = PV_{IN} = 5 V, VDD = 2.5 V,
Switching Frequency = 1 MHz, Mode = Pulse Skip Mode (PSM),
T_a = 25 °C ± 2 °C unless otherwise specified.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
DC-DC Characteristics							
Line regulation	V_{LIN}	V_{IN} = 4.5 V to 5.6 V I_{OUT} = 4 A	—	0.5	1.5	%/V	—
Load regulation	V_{LOA}	I_{OUT} = 10 mA to 6 A	—	3	—	%	*1
Output ripple voltage 1	V_{R1}	I_{OUT} = 10 mA	—	25	—	mV [p-p]	*1
Output ripple voltage 2	V_{R2}	I_{OUT} = 4 A	—	10	—	mV [p-p]	*1
Load transient response 1	ΔV_{TR1}	I_{OUT} = 100 mA to 4 A Δ t = 0.5 A / µs	—	20	—	mV	*1
Load transient response 2	ΔV_{TR2}	I_{OUT} = 4 A to 100 mA Δt = 0.5 A / µs	—	20	—	mV	*1
High Side Power MOSFET ON resistance	R_{ONH}	V_{GS} = 5 V	—	25	50	mΩ	—
Low Side Power MOSFET ON resistance	R_{ONL}	V_{GS} = 5 V	—	25	50	mΩ	—
MIN input and output voltage difference	V_{diff}	V_{diff} = V_{IN} – V_{OUT}	—	2	—	V	*1

Note : *1 : Typical Design Value

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ELECTRICAL CHARACTERISTICS (Continued)

Co = 22 µF × 2, Lo= 1 µH, V_{OUT} Setting = 1.0 V, V_{IN} = AV_{IN} = PV_{IN} = 5 V, VDD = 2.5 V,
Switching Frequency = 1 MHz, Mode = Pulse Skip Mode (PSM),
T_a = 25 °C ± 2 °C unless otherwise specified.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Protection							
Over Current Protection Limit	I_{LMT}	—	—	9	—	A	*1
Short Circuit Protection Threshold	I_{short}	V_{FB} = 0.6 V to 0.0 V	55	70	85	%	—
Thermal Shut Down (TSD) Threshold	T_{TSDTH}	—	—	140	—	°C	*1
Thermal Shut Down (TSD) Hysteresis	T_{TSDHYS}	—	—	25	—	°C	*1
Soft Start Timing							
SS Charge Current	I_{SSCH}	V_{SS} = 0.3 V	—	2	4	µA	—
SS Discharge Resistance (Shut-down)	R_{SSDCH}	V_{EN} = 0 V, I_{OUT} = 0 A	—	2	4	kΩ	—
Switching Frequency							
Switching Frequency 1	f_{SW1}	I_{OUT} = 6 A I^2C Setting: 10h:10h	—	500	—	kHz	*1
Switching Frequency 2	f_{SW2}	I_{OUT} = 6 A I^2C Setting: 10h:30h	—	1000	—	kHz	*1
Switching Frequency 3	f_{SW3}	I_{OUT} = 6 A I^2C Setting: 10h:70h	—	2000	—	kHz	*1

Note : *1 : Typical Design Value

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ELECTRICAL CHARACTERISTICS (Continued)

REFERENCE VALUES FOR DESIGN

Co = 22 µF × 2, Lo= 1 µH, V_{OUT} Setting = 1.0 V, V_{IN} = AV_{IN} = PV_{IN} = 5 V, VDD = 1.85 V,
Switching Frequency = 1 MHz, Mode = Pulse Skip Mode (PSM),
T_a = 25 °C ± 2 °C unless otherwise specified.

Parameter	Symbol	Condition	Reference Values			Unit	Note
			Min	Typ	Max		
I²C Bus (Internal I/O Stage Characteristics)							
Low-level input voltage	V_{IL}	Voltage which recognized that SDA and SCL are Low-level	– 0.5	—	0.3 × VDD	V	*1
High-level input voltage	V_{IH}	Voltage which recognized that SDA and SCL are High-level	0.7 × VDD	—	VDD_{max} +0.5	V	*1
Low-level output voltage 1	V_{OL1}	VDD > 2 V SDA (sink current=3 mA)	0	—	0.4	V	—
Low-level output voltage 2	V_{OL2}	VDD < 2 V SDA (sink current=3 mA)	0	—	0.2 × VDD	V	—
Input current each I/O pin	I_L	SDA, SCL = 0.1 × VDD_{max} to 0.9 × VDD_{max}	– 10	—	10	µA	—
SCL clock frequency	F_{OSC}	—	0	—	400	kHz	—
Hysteresis of Schmitt trigger input 1	V_{hys1}	V_{IO} > 2 V, Hysteresis 1 of SDA, SCL	0.05 × VDD	—	—	V	*2
Hysteresis of Schmitt trigger input 2	V_{hys2}	V_{IO} < 2 V, Hysteresis 2 of SDA, SCL	0.1 × VDD	—	—	V	*2
Output fall time from V_{IHmin} to V_{ILmax}	T_{of}	Bus capacitance : 10 pF to 400 pF $I_P \leq 6$ mA, (V_{OLmax} = 0.6 V) I_P : Max. sink current	20+ 0.1×C_b	—	250	ns	*2
Pulse width of spikes which must be suppressed by the input filter	T_{sp}	—	0	—	50	ns	*2
Capacitance for each I/O pin	C_i	—	—	—	10	pF	*2

Notes: Checked by design, not production tested.

*1 : The input threshold voltage of I²C bus (V_{th}) is linked to VDD.
In case the pull-up voltage is not VDD, the threshold voltage (V_{th}) is fixed to ((VDD / 2) ± (Schmitt width) / 2) and High-level, Low-level of input voltage are not specified.
In this case, pay attention to Low-level (max.) value (V_{ILmax}).
It is recommended that the pull-up voltage of I²C bus is set to the I²C bus I/O stage supply voltage (VDD).

*2 : The timing of Fast-mode devices in I²C-bus is specified based on V_{IHmin} and V_{ILmax} levels.

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ELECTRICAL CHARACTERISTICS (Continued)

REFERENCE VALUES FOR DESIGN (Continued)

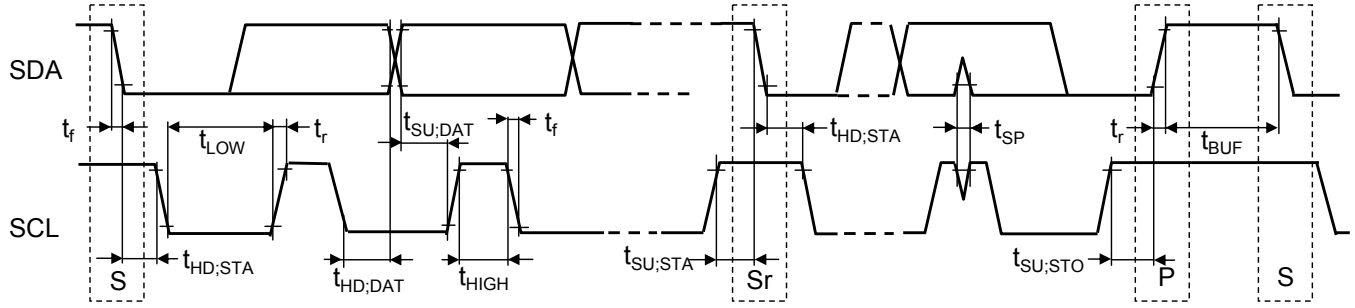
Co = 22 µF × 2, Lo= 1 µH, V_{OUT} Setting = 1.0 V, V_{IN} = AV_{IN} = PV_{IN} = 5 V, VDD = 1.85 V,
Switching Frequency = 1 MHz, Mode = Pulse Skip Mode (PSM),
T_a = 25 °C ± 2 °C unless otherwise specified.

Parameter	Symbol	Condition	Reference Values			Unit	Note
			Min	Typ	Max		
I²C bus (Internal I/O stage characteristics)							
Hold time (repeated) START condition	$t_{HD:STA}$	The first clock pulse is generated after $t_{HD:STA}$.	0.6	—	—	µs	*1
Low period of the SCL clock	t_{LOW}	—	1.3	—	—	µs	*1
High period of the SCL clock	t_{HIGH}	—	0.6	—	—	µs	*1
Set-up time for a repeat START condition	$t_{SU:STA}$	—	0.6	—	—	µs	*1
Data hold time	$t_{HD:DAT}$	—	0	—	0.9	µs	*1
Data set-up time	$t_{SU:DAT}$	—	100	—	—	ns	*1
Rise time of both SDA and SCL signals	t_r	—	20 + 0.1×C_b	—	300	ns	*1 *2
Fall time of both SDA and SCL signals	t_f	—	20 + 0.1×C_b	—	300	ns	*1 *2
Set-up time of STOP condition	$t_{SU:STO}$	—	0.6	—	—	µs	*1
Bus free time between STOP and START condition	t_{BUF}	—	1.3	—	—	µs	*1
Capacitive load for each bus line	C_b	—	—	—	400	pF	*1
Noise margin at the Low-level for each connected device	V_{nL}	—	0.1 × VDD	—	—	V	*1
Noise margin at the High-level for each connected device	V_{nH}	—	0.2 × VDD	—	—	V	*1

Notes : Checked by design, not production tested.

*1 : The timing of Fast-mode devices in I²C-bus is specified as the following.
All values referred to V_{IHmin} and V_{ILmax} level.

*2 : For Standard-mode I²C devices, the minimum limits for t_r and t_f are not specified.



S : START condition
Sr : Repeat START condition
P : STOP condition

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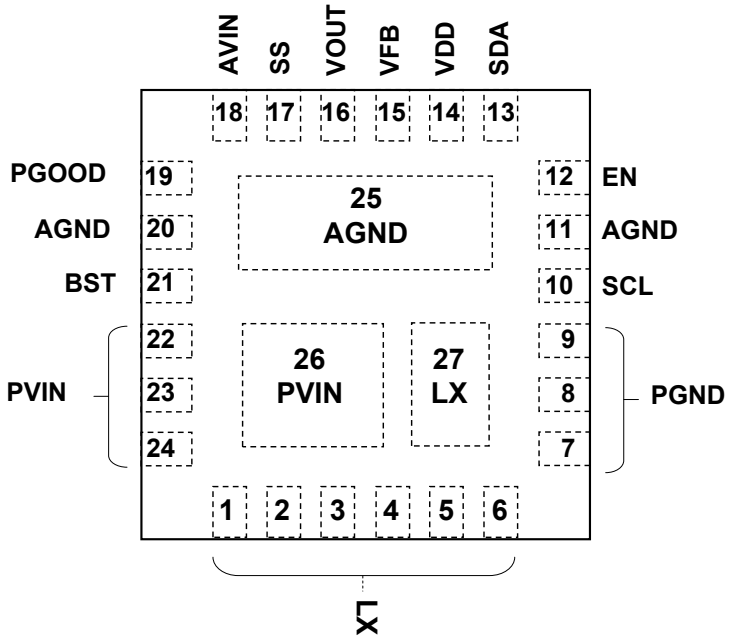
PIN CONFIGURATION

Top View



PIN FUNCTIONS

Pin No.	Pin name	Type	Description
1 2 3 4 5 6	LX	Output	Power MOSFET output pin An inductor is connected and switching operation is carried out between V_{IN} and GND. Due to high current and large amplitude at this terminal, the parasitic inductance and impedance of the routing path can cause an increase in noise and a degradation in the efficiency. Routing path should be kept as short as possible.
7 8 9	PGND	Ground	Ground pin for Power MOSFET
10	SCL	Input	I^2C Interface Clock Input pin
11 20	AGND	Ground	Ground pin
12	EN	Input	DC-DC ON / OFF control pin DC-DC stops operation at Low level input, and starts operation at High level input.
13	SDA	Input / Output	I^2C Interface Data I/O pin
14	VDD	Power Supply	Power supply pin for Digital Circuit

Note: Detailed pin descriptions are provided in the OPERATION and APPLICATION INFORMATION section.

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PIN FUNCTIONS (Continued)

Pin No.	Pin name	Type	Description
15	VFB	Input	Comparator's negative input pin VFB terminal voltage is regulated to REF output (internal reference voltage). Since VFB is a high impedance terminal, it should not be routed near other noisy path (LX, BST, etc.) or the inductor. Routing path should be kept as short as possible.
16	VOUT	Input	Output voltage sense pin Switching frequency is controlled by monitoring output voltage.
17	SS	Output	Soft start capacitor connect pin The startup output voltage is smoothly controlled by adjusting the Soft Start time. Connect capacitor between SS and GND.
18	AVIN	Power supply	Power supply pin Recommended rise time (time to reach 90 % of set value) setting is greater than or equal to 10 µs and less than or equal to 1 s.
19	PGOOD	Output	Power Good function pin The PGOOD pin is made of an open drain MOSFET structure. This requires the connection of a pull-up resistor between PGOOD and VDD terminal. Output is low during Over or Under Voltage Detection conditions.
21	BST	Output	High side Power MOSFET gate driver pin Bootstrap operation is carried out in order to drive the gate voltage of High side Power MOSFET. Please connect a capacitor between BST and LX pin. Routing path should be kept as short as possible to minimize noise.
22	PVIN	Power supply	Power supply pin for Power MOSFET Recommended rise time (time to reach 90 % of set value) setting is greater than or equal to 10 µs and less than or equal to 1 s.
23			
24			
25	AGND	Ground	Ground pin for heat radiation.
26	PVIN	Power supply	Power supply pin for heat radiation.
27	LX	Output	Power MOSFET output pin for heat radiation.

Note: Detailed pin descriptions are provided in the OPERATION and APPLICATION INFORMATION section.

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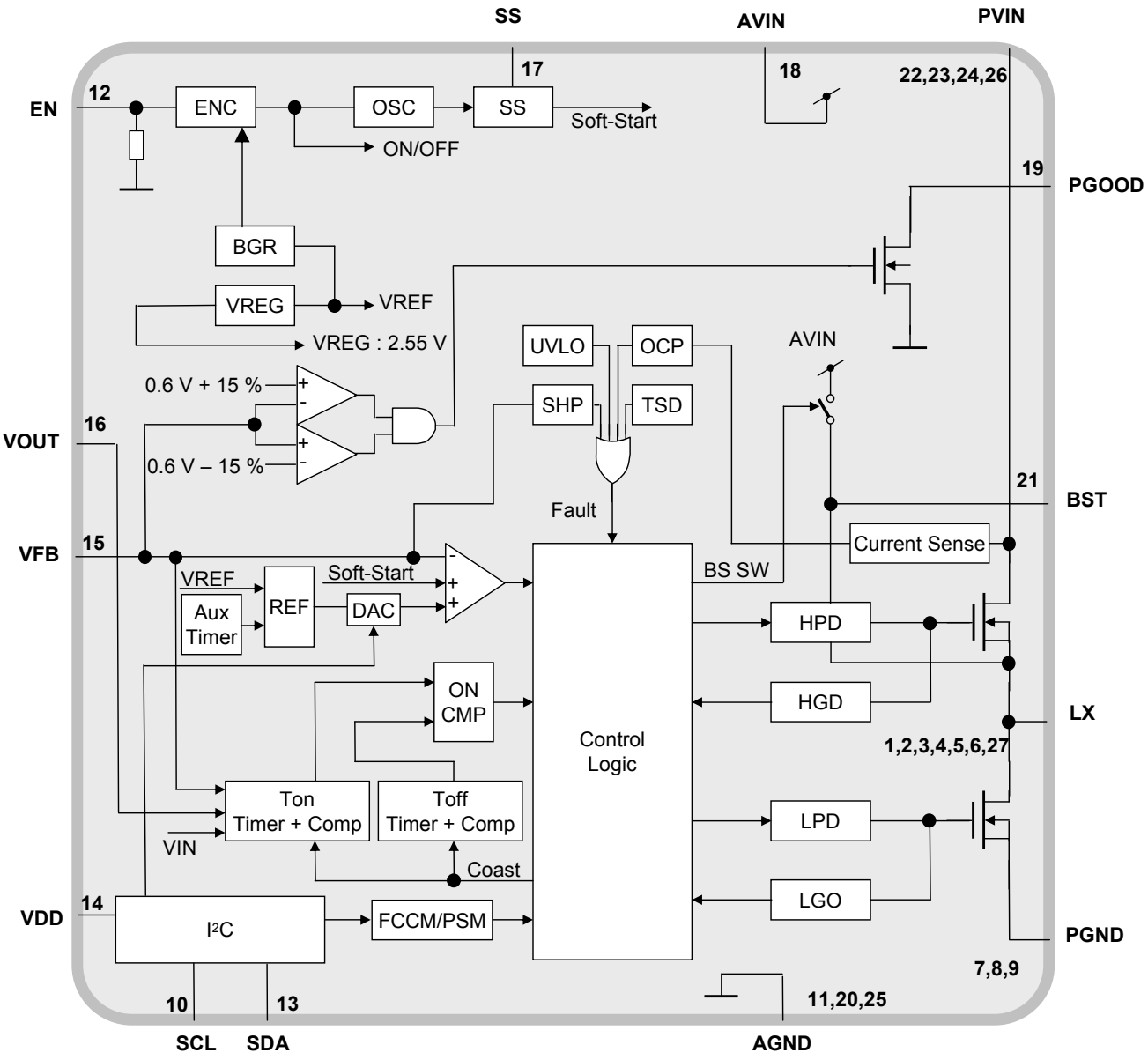
FUNCTIONAL BLOCK DIAGRAM



Note: This block diagram is for explaining functions. Part of the block diagram may be omitted, or it may be simplified.

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OPERATION

1. Protection

(1) Over Current Protection (OCP) and Short Circuit Protection (SCP)

1) The Over Current Protection is activated at about 9 A (Typ.) During the OCP, the output voltage continues to drop at the specified current.

2) The Short-Circuit Protection function is implemented when the output voltage decreases and the VFB pin reaches to about 70 % of the set voltage of 0.6 V.

3) The SCP operates intermittently at 2 ms-ON, 16 ms-OFF intervals.

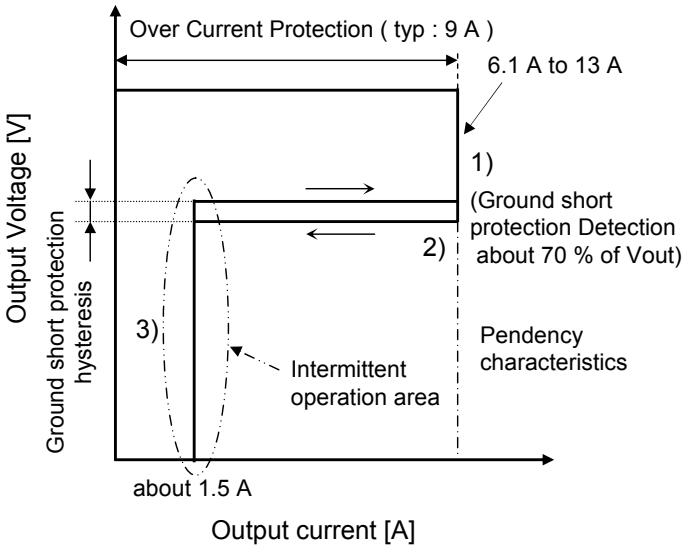

Figure : OCP and SCP Operation

(2) Over Voltage Detection (OVD) and Under Voltage Detection (UVD)

1) The MOSFET connected to the PGOOD pin turns ON when the output voltage rises and the VFB pin voltage reaches 115 % of its set voltage (0.603 V).

2) After (1) above, the MOSFET connected to the PGOOD pin is turned OFF after 1 ms when the output voltage drops and the VFB pin voltage reaches 110 % of its set voltage (0.603 V).

3) The MOSFET connected to the PGOOD pin turns ON when the output voltage drops and the VFB pin voltage reaches 85 % of its set voltage (0.603 V).

4) After (3) above, the MOSFET connected to the PGOOD pin is turned OFF after 1 ms when the output voltage drops and the VFB pin voltage reaches 90 % of its set voltage (0.603 V).

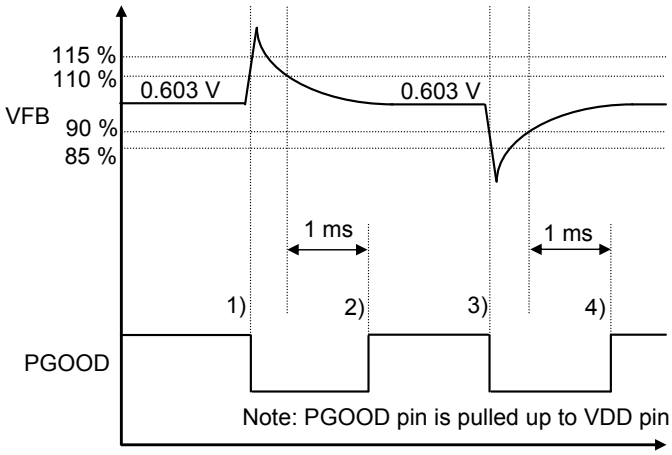

Figure : OVD and UVD Operation

(3) Thermal Shut Down (TSD)

When the IC internal temperature becomes more than about 140 °C, TSD operates and DC-DC turns off.

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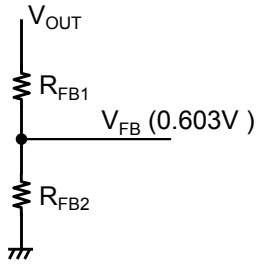
OPERATION (Continued)

2. Output Voltage Setting

The Output Voltage is set by adjusting the value of the external resistors R_{FB1} and R_{FB2}. The equation below represents the relation between the external resistors and V_{OUT}.

(V_{IN} = 5.0 V, I_{OUT} = 1 A, FCCM, f_{SW} = 1 MHz)



$$V_{OUT} = -0.0119 \left(\frac{R_{FB1}}{R_{FB2}}\right)^2 + 0.616 \left(\frac{R_{FB1}}{R_{FB2}}\right) + 0.593$$

The following table represents the Feedback Resistor (R_{FB}) setting for standard output voltage setups.

V_{OUT} [V]	R_{FB1} [Ω]	R_{FB2} [Ω]
1.8	3.0 k	1.5 k
1.2	1.0 k	1.0 k
1.0	1.0 k	1.5 k

Note: R_{FB2} can be set to a maximum value of 10 kΩ. A larger R_{FB2} value will be more susceptible to noise.

VFB comparator threshold is adjusted to ± 1.33 %, but the actual output voltage accuracy becomes more than ± 1.33 % due to the influence from the circuits other than VFB comparator.

In the case of V_{OUT} setting = 1.0 V, the actual output voltage accuracy becomes ± 2 %.

(V_{IN} = 5.0 V, I_{OUT} = 1 A, FCCM, f_{SW} = 1 MHz)

3. Soft Start Setting

Soft Start function maintains the smooth control of the output voltage during start up by adjusting soft start time. When the EN pin becomes “High”, a current of 2 µA begins to charge the external capacitor (C_{ss}) at the SS pin, and the SS pin voltage increases linearly.

The SS pin voltage controls the FB pin voltage, resulting in a linear increase in the FB pin voltage. The FB voltage remains constant after its designed value is reached.

On the other hand, the SS pin voltage continues to increase up to the designed value of about 2.55 V.

The calculation of Soft Start Time is as follows.

$$\text{Soft Start Setting [s]} = \frac{0.6}{2\mu} \times C_{SS}$$

When Css is set at 10 nF, soft-start time is approximately 3 ms.

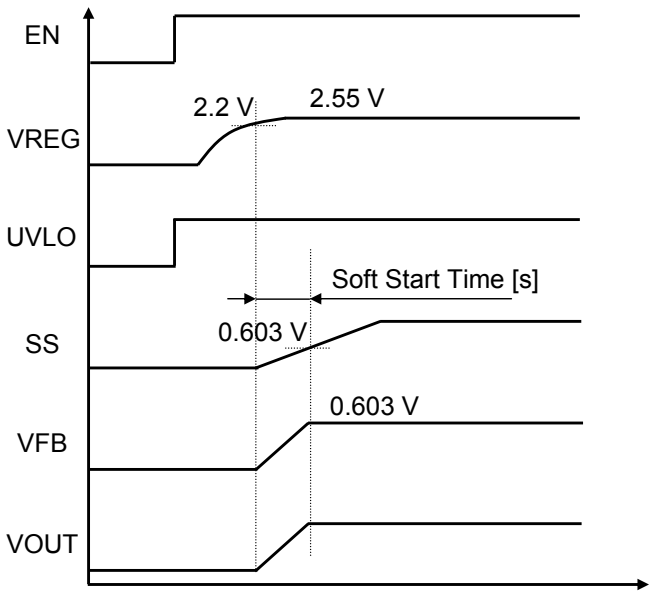


Figure : Soft Start Operation

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OPERATION (Continued)

4. Power ON / OFF sequence

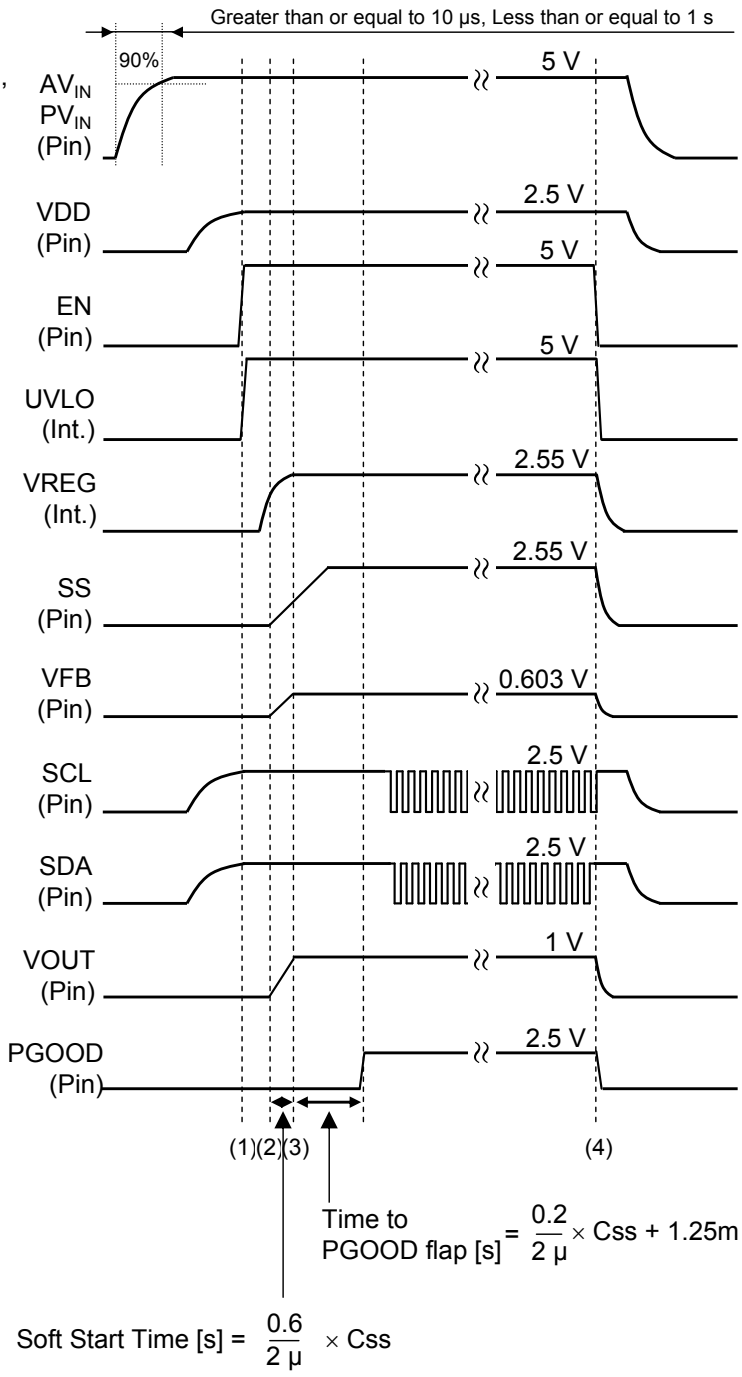
(1) When the EN pin is set to “High” after the V_{IN} settles, the UVLO is released after V_{IN} exceeds its threshold. (Recommended V_{IN} rise time (time to reach 90 % of set value) setting is greater than or equal to 10 µs and less than or equal to 1 s

(2) After the UVLO is released, the VREG (built-in LDO for internal power supply) starts up. The SOFT START sequence is initiated when the VREG exceeds its threshold. The capacitor connected to the SS pin begins to charge and the SS pin voltage increases linearly.

(3) The VOUT pin (DCDC Output) voltage increases at the same rate as the SS pin. Normal operation begins after the VOUT pin reaches the set voltage.

(4) When the EN pin is set to “Low”, the VREG and UVLO stop operation and the VOUT pin / SS pin voltage drops to 0V. VOUT pin discharge time depends on the output load current and the feedback resistor value.

Note: The SS pin capacitor should be discharged completely before restarting the startup sequence. An incomplete discharge process might result in an overshoot of the output voltage.



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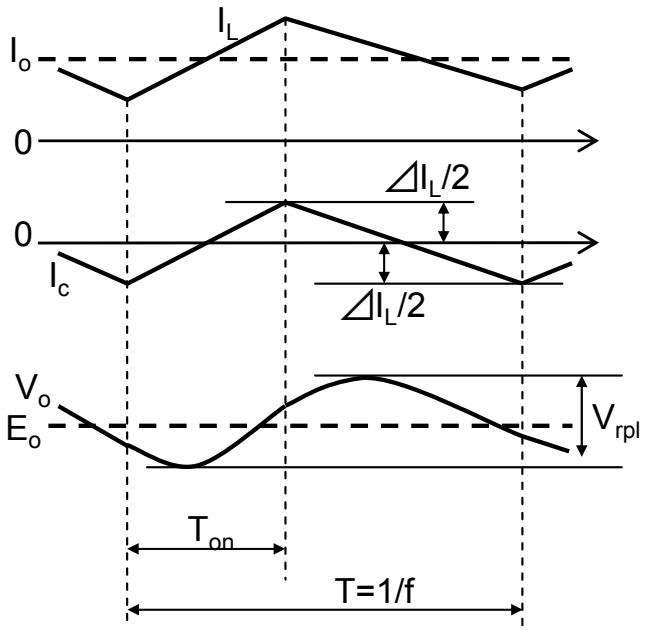
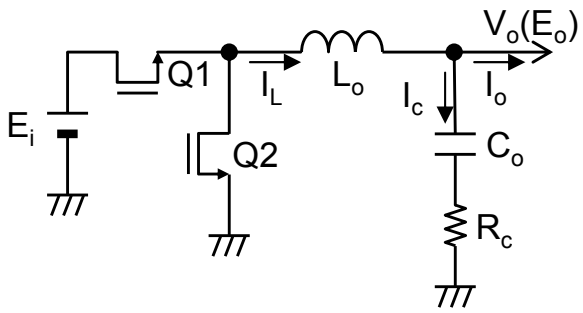
OPERATION (Continued)

5. Inductor and Output Capacitor Setting





Given the desired input and output voltages, the inductor value and operating frequency determine the ripple current.

$$\Delta IL = \frac{Eo \cdot (Ei - Eo)}{Ei \cdot Lo \cdot f}$$

$$Iox = \frac{\Delta IL}{2}$$

Highest efficiency operation is obtained at low frequency with small ripple current. However, achieving this requires a large inductor. There is a trade-off among component size, efficiency and operating frequency.

A reasonable starting point is to choose a ripple current that is about 40 % of I_O (Max.). The largest ripple current occurs at the highest E_i. To guarantee that ripple current does not exceed a specified maximum, the inductance should be chosen according to:

$$Lo \geq \frac{Eo \cdot (Ei - Eo)}{2Ei \cdot Iox \cdot f} \quad @\ \mathrm{Ei} = \mathrm{Ei\_max}$$

And its maximum current rating is

$$\mathrm{IL\_max} = \mathrm{Io\_max} + \frac{\Delta \mathrm{IL}}{2} \quad (@\ \mathrm{Ei} = \mathrm{Ei\_max})$$

The selection of C_O is primarily determined by the ESR (R_c) required to minimize voltage ripple and load transients. The output ripple V_{rpl} is approximately bounded by:

$$Vrpl = Vop - Vob = Ei \cdot \frac{Co \cdot Rc^2}{2Lo} + \frac{\Delta IL}{8Co \cdot f}$$

$$= Ei \cdot \frac{Co \cdot Rc^2}{2Lo} + \frac{Eo \cdot (Ei - Eo)}{8Ei \cdot Lo \cdot Co \cdot f^2}$$

From the above equation, to achieve desired output ripple, low ESR ceramic capacitors are recommended, and its required RMS current rating is:

$$Ic(\mathrm{rms})\_\mathrm{max} = \frac{\Delta IL}{2\sqrt{3}} \quad (@\ \mathrm{Ei} = \mathrm{Ei\_max})$$

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OPERATION (Continued)

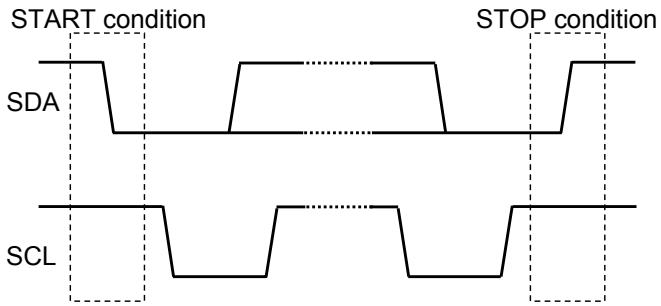
6. I²C-bus Interface

a) Basic Rules

- This IC, I²C-bus, is designed to correspond to the Standard-mode (100 kbps) and Fast-mode (400 kbps) devices in the version 2.1 of NXP's specification. However, it does not correspond to the H_S-mode (to 3.4 Mbps).
- This IC will operate as a slave device in the I²C-bus system. This IC will not operate as a master device.
- The program operation check of this IC has not been conducted on the multi-master bus system and the mix-speed bus system, yet. The connected confirmation of this IC to the CBUS receiver also has not been checked. Please confirm with our company if the IC will be used in these mode systems.
- The I²C is the brand of NXP.

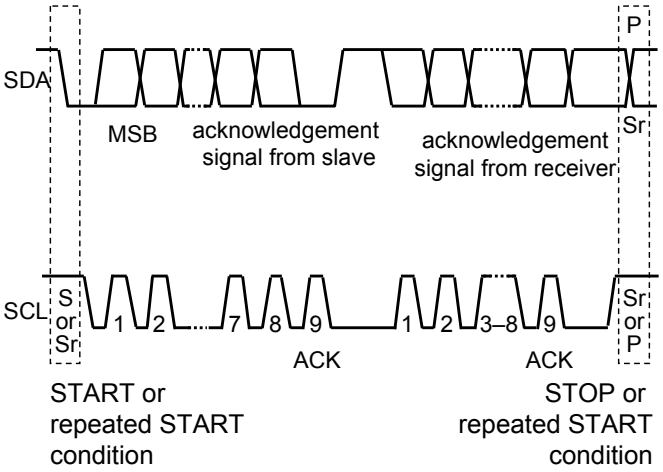
b) START and STOP conditions

- A High to Low transition on the SDA line while SCL is High is one such unique case. This situation indicates START condition. A Low to High transition on the SDA line while SCL is High defines STOP condition.
- START and STOP conditions are always generated by the master. After START condition occur, the bus will be busy. The bus is considered to be free again a certain time after the STOP condition.



c) Transferring Data

Every byte put on the SDA line must be 8-bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first.



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OPERATION (Continued)

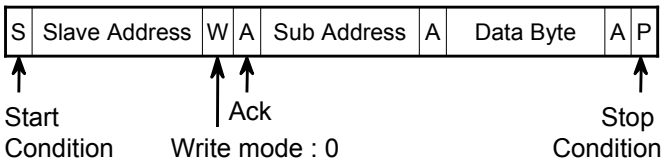
6. I²C-bus Interface (Continued)

d) Data format

Slave Address

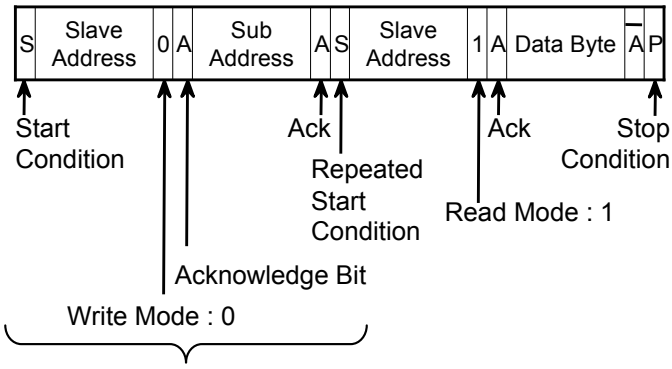
A6	A5	A4	A3	A2	A1	A0	R/W	Hex
1	1	1	0	0	1	0	x	72h

Write mode



Read mode (Continued)

d2) When Sub address is specified

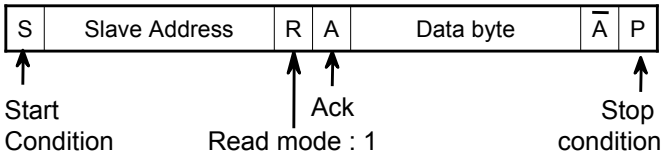


Sub-address should be assigned first.

Read mode

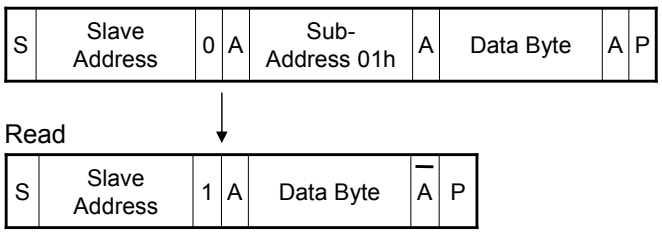
d1) When Sub address is not specified

When data is read without assigning sub-address, it is possible to read the value of sub-address specified in Write mode immediately before.



Ex) When writing data into address and reading data from "01 h".

Write



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OPERATION (Continued)

6. I²C-bus Interface (Continued)

Sub Address	R/W	Register Name	Bit	Data							
				D7	D6	D5	D4	D3	D2	D1	D0
10h	R/W	CNT	Name	—	FSEL[6:4]			—	—	FCCM	DCDCOFF
			Default	—	0	0	0	—	—	0	0
11h	R/W	DAC	Name	—	—	—	—	VDC[3:0]			
			Default	—	—	—	—	0	0	0	0

Sub Address : 10h
D6 – D4 (FSEL Setting)

FSEL [6:4]			FREQUENCY (MHz)
D6	D5	D4	
0	0	0	1.00 (Default)
0	0	1	0.50
0	1	0	0.75
0	1	1	1.00
1	0	0	1.25
1	0	1	1.50
1	1	0	1.75
1	1	1	2.00

Sub Address : 10h
D0 : DCDCOFF

0 : DC-DC ON (Default)
1 : DC-DC OFF

Sub Address : 10h
D1 : FCCM

0 : Pulse Skip Mode (Default)
1 : Forced Continuous Conduction Mode

Sub Address : 11h
D6 – D4 (FSEL Setting)

VDC [3:0]				Output Voltage [V]
D3	D2	D1	D0	
0	0	0	0	1.000 (Default)
0	0	0	1	0.880
0	0	1	0	0.895
0	0	1	1	0.910
0	1	0	0	0.925
0	1	0	1	0.940
0	1	1	0	0.955
0	1	1	1	0.970
1	0	0	0	0.985
1	0	0	1	1.000
1	0	1	0	1.015
1	0	1	1	1.030
1	1	0	0	1.045
1	1	0	1	1.060
1	1	1	0	1.075
1	1	1	1	1.090

Note: The required output voltage is set by changing the DAC step by 1 bit at a time. An interval of more than 50 µs is required at every bit step while changing the DAC.

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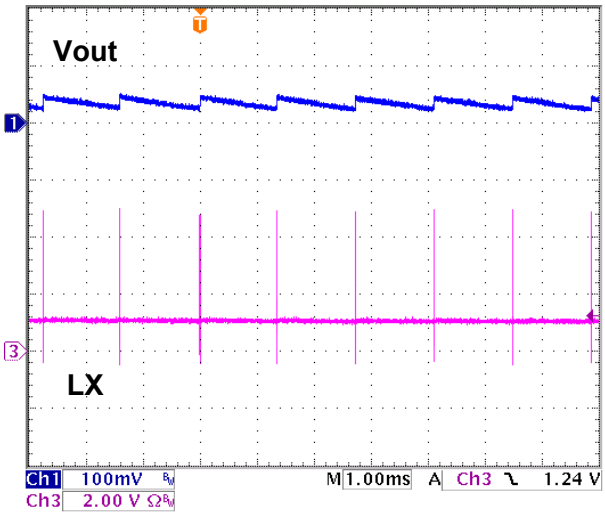
TYPICAL CHARACTERISTICS CURVES

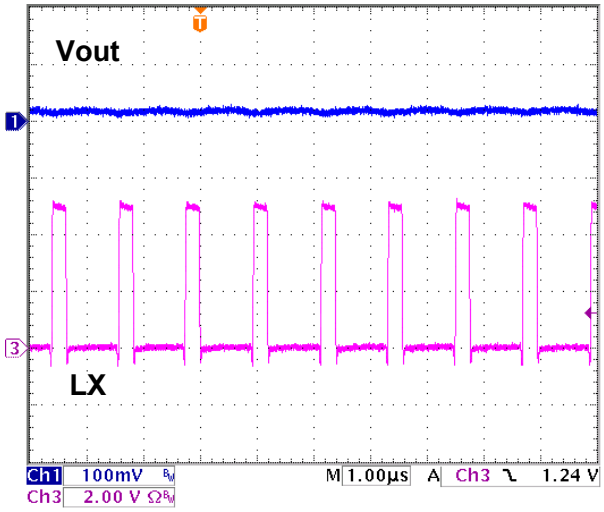
(1) Output Ripple Voltage

Condition : V_{IN} = 5.0 V, V_{OUT} = 1.0 V, f_{SW} = 1.0 MHz, PSM, L_O = 1 µH, C_O = 44 µF (22 µF x 2),

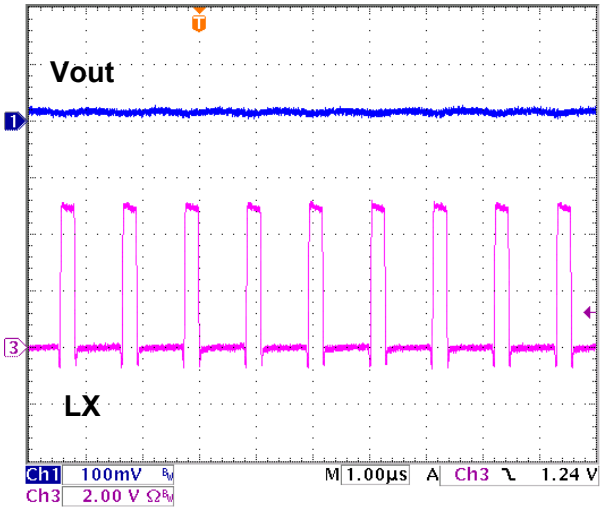
I_{OUT} = 0A



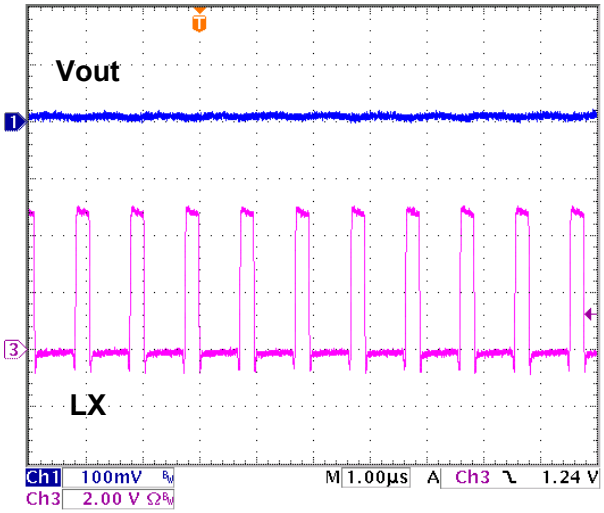
I_{OUT} = 1A



I_{OUT} = 3A



I_{OUT} = 6A



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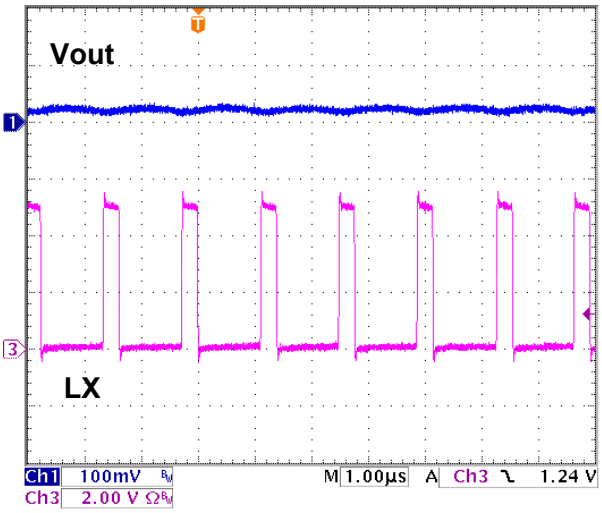
TYPICAL CHARACTERISTICS CURVES (Continued)

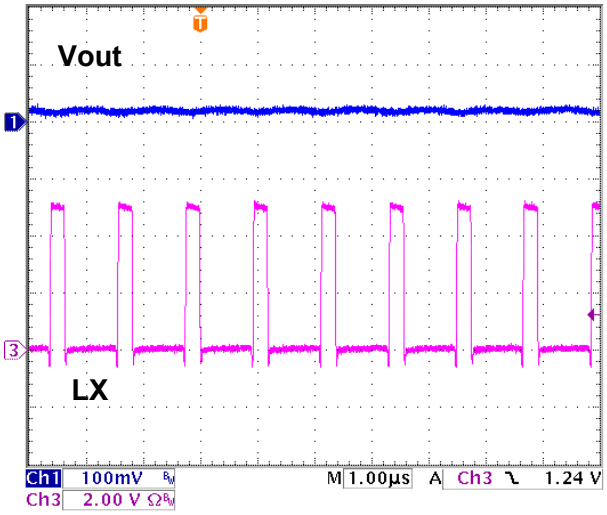
(1) Output Ripple Voltage (Continued)

Condition : V_{IN} = 5.0 V, V_{OUT} = 1.0 V, f_{SW} = 1.0 MHz, FCCM, L_O = 1 µH, C_O = 44 µF (22 µF x 2),

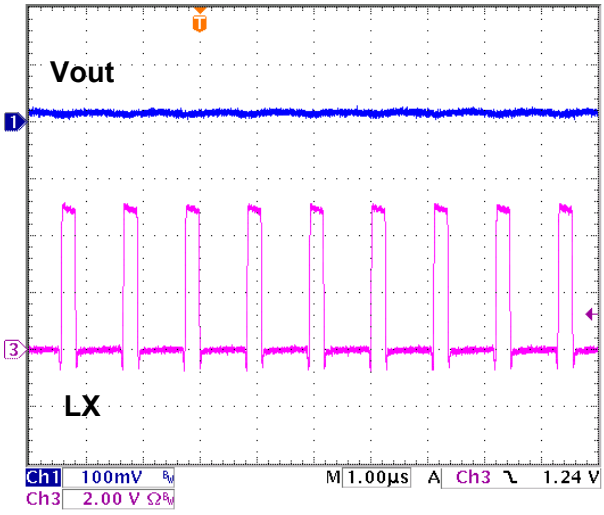
I_{OUT} = 0A



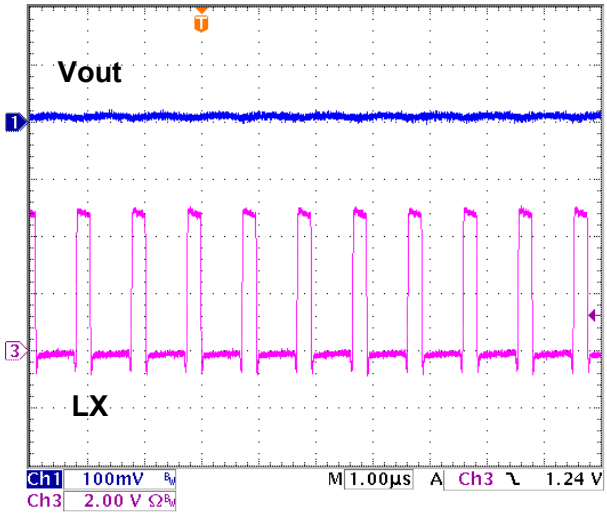
I_{OUT} = 1A



I_{OUT} = 3A



I_{OUT} = 6A



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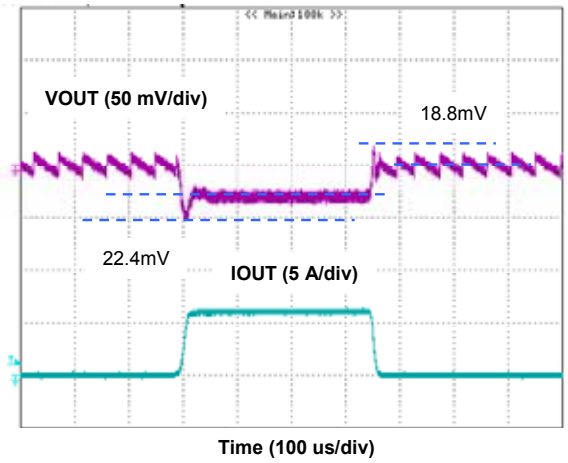
TYPICAL CHARACTERISTICS CURVES (Continued)

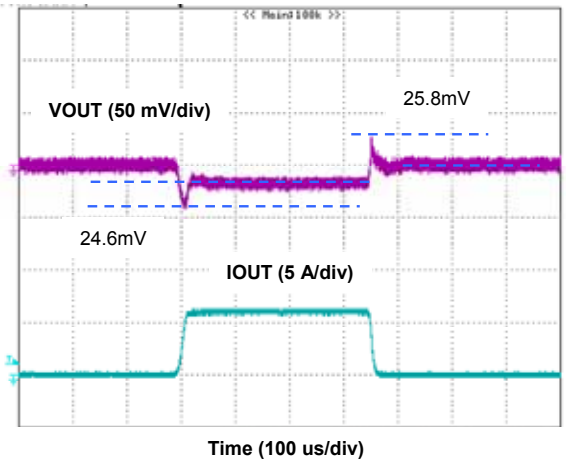
(2) Load transient response

Condition : V_{IN} = 5.0 V, V_{OUT} = 1.0 V, f_{SW} = 1.0 MHz, I_{OUT} = 10 mA to 6 A (0.5 A / µs),
L_O = 1 µH, C_O = 44 µF (22 µF x 2),

PSM

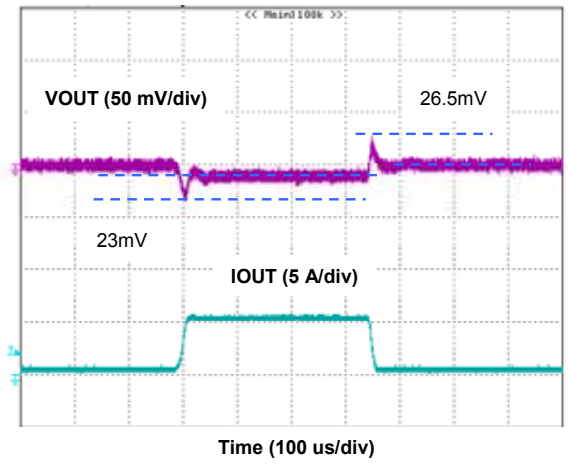


FCCM

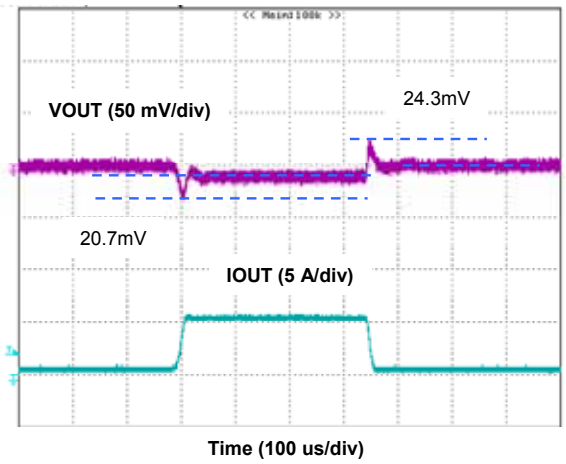


Condition : V_{IN} = 5 V, V_{OUT} = 1.0 V, f_{SW} = 1.0 MHz, I_{OUT} = 0.6 A to 5.4 A (0.5 A / µs),
L_O = 1 µH, C_O = 44 µF (22 µF x 2),

PSM



FCCM



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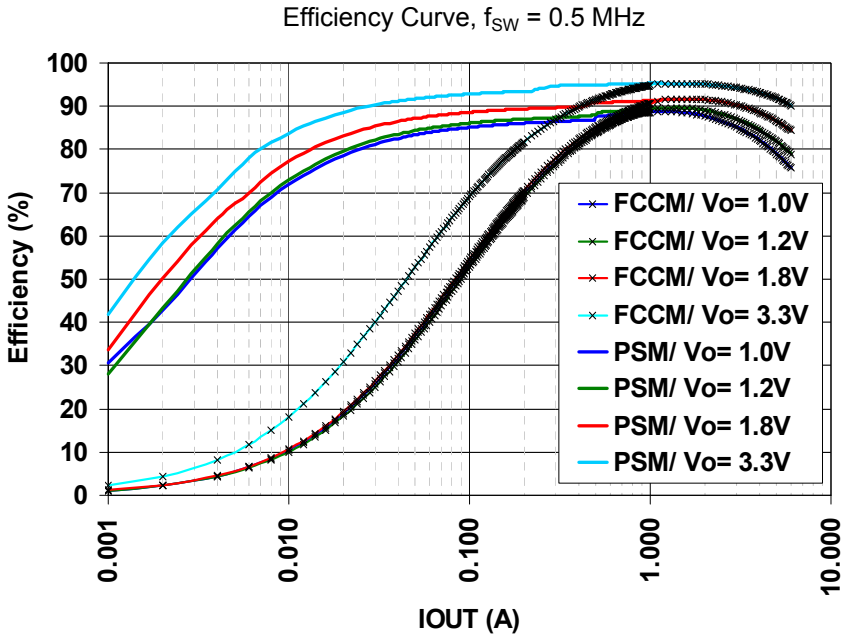
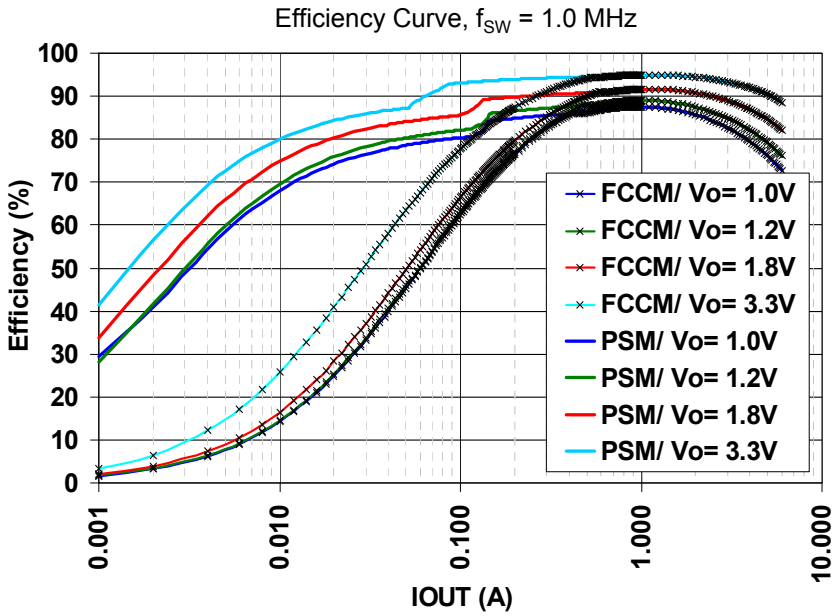
TYPICAL CHARACTERISTICS CURVES (Continued)

(3) Efficiency

Condition : V_{IN} = 5.0 V, V_{OUT} = 1.0 V / 1.2 V / 1.8 V / 3.3 V, f_{SW} = 0.5 MHz
L_O = 1 µH, C_O = 44 µF (22 µF x 2)



Condition : V_{IN} = 5.0 V, V_{OUT} = 1.0 V / 1.2 V / 1.8 V / 3.3 V, f_{SW} = 1.0 MHz
L_O = 1 µH, C_O = 44 µF (22 µF x 2)



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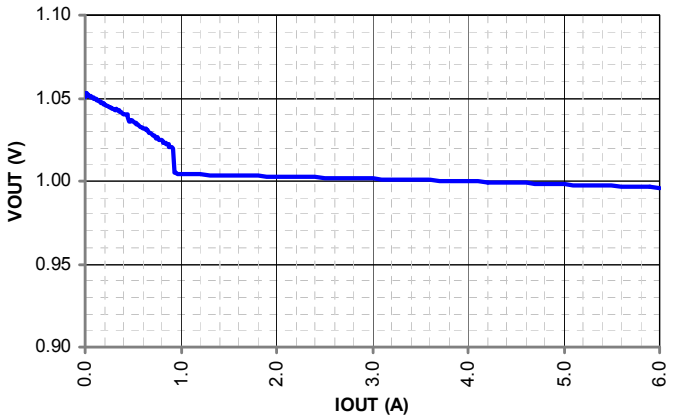
TYPICAL CHARACTERISTICS CURVES (Continued)

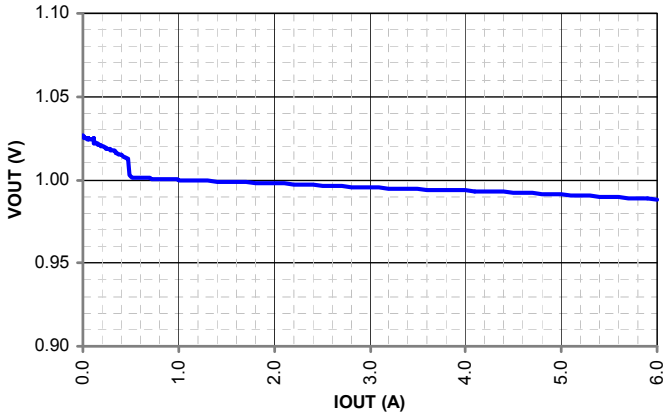
(4) Load Regulation

Condition : V_{IN} = 5.0 V, V_{OUT} = 1.0 V, f_{SW} = 0.5 MHz, L_O = 1 µH, C_O = 44 µF (22 µF x 2)

Load regulation f_{SW} = 0.5 MHz PSM

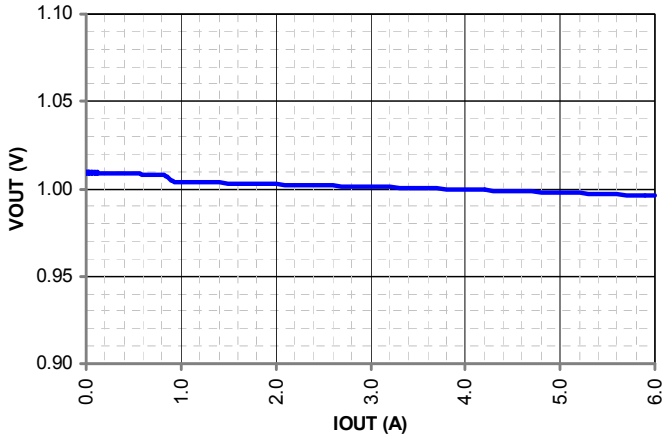


Load regulation f_{SW} = 0.5 MHz FCCM

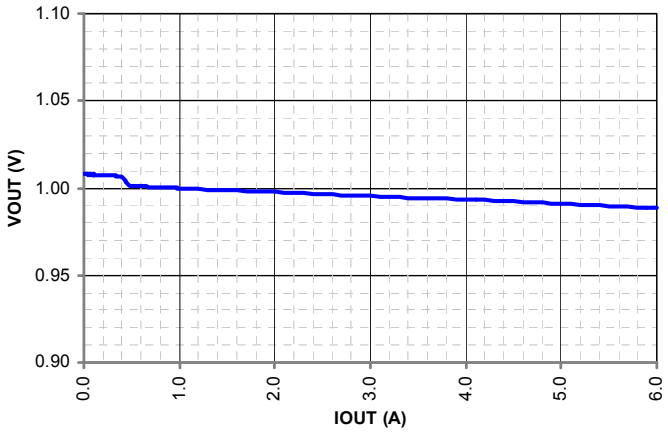


Condition : V_{IN} = 5.0 V, V_{OUT} = 1.0 V, f_{SW} = 1.0 MHz, L_O = 1 µH, C_O = 44 µF (22 µF x 2)

Load regulation f_{SW} = 1.0 MHz PSM



Load regulation f_{SW} = 1.0 MHz FCCM



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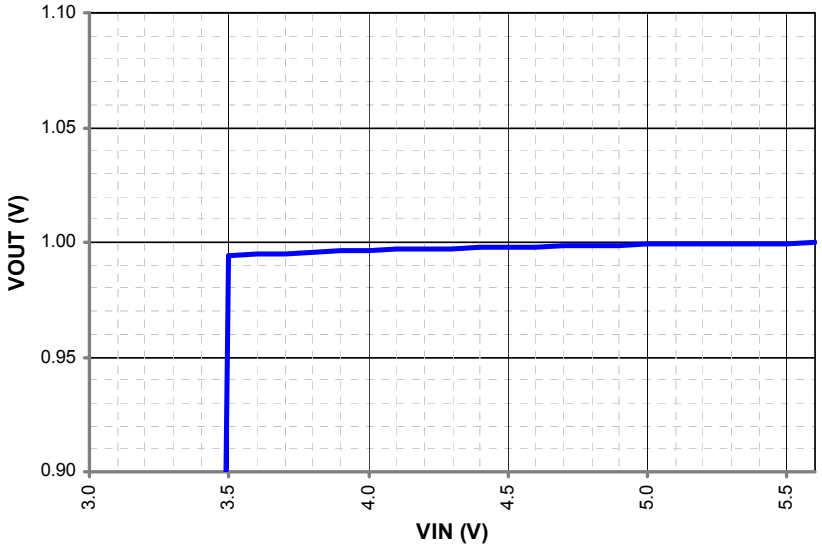
TYPICAL CHARACTERISTICS CURVES (Continued)

(5) Line Regulation

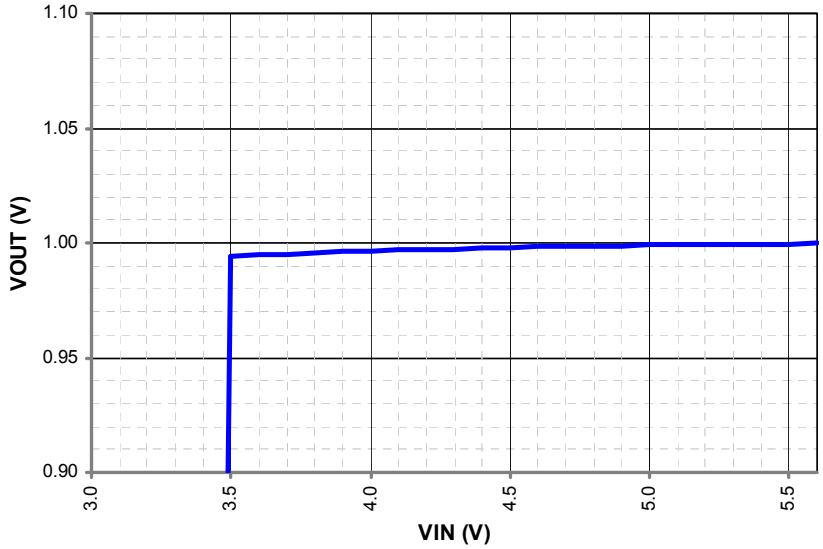
Condition : V_{OUT} = 1.0 V, I_{OUT} = 1.5 A, f_{SW} = 0.5 MHz, PSM, L_O = 1 µH, C_O = 44 µF (22 µF x 2)

Line regulation f_{SW} = 0.5 MHz PSM



Condition : V_{OUT} = 1.0 V, I_{OUT} = 1.5 A, f_{SW} = 1.0 MHz, FCCM, L_O = 1 µH, C_O = 44 µF (22 µF x 2)

Line regulation f_{SW} = 1.0 MHz FCCM



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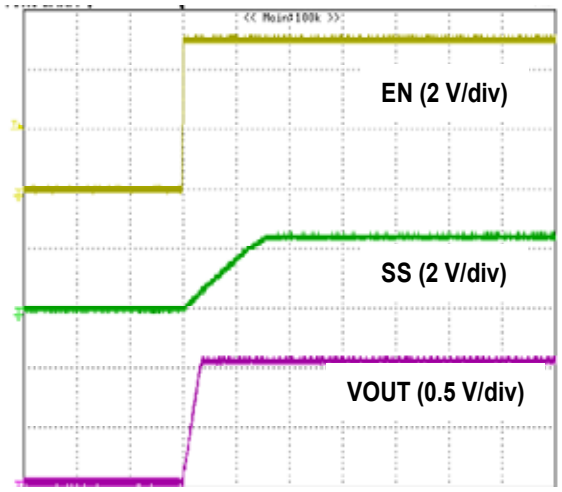
TYPICAL CHARACTERISTICS CURVES (Continued)

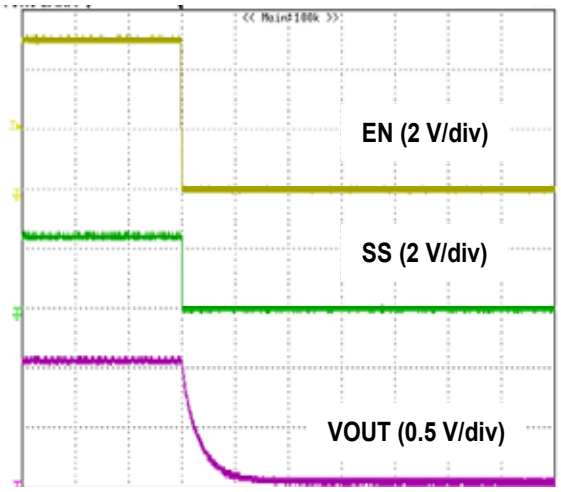
(6) Startup / Shutdown

Condition : V_{IN} = 5.0 V, V_{OUT} = 1.0 V, f_{SW} = 1 MHz, PSM, I_{OUT} = 0 A, L_O = 1 µH, C_O = 44 µF (22 µF x 2)

Startup

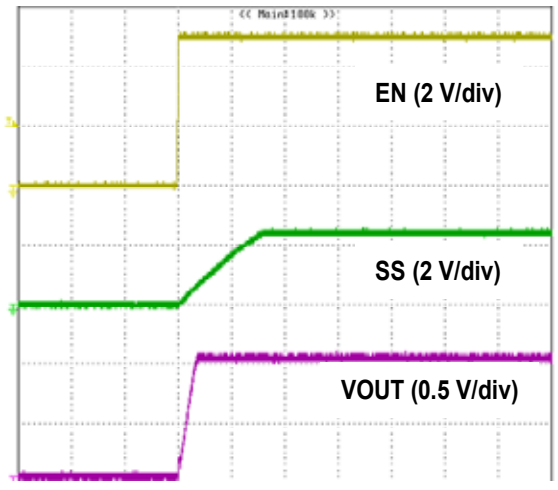


Shutdown

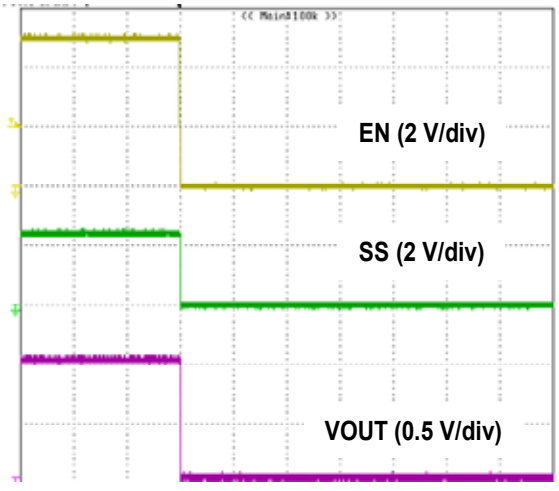


Condition : V_{IN} = 5.0 V, V_{OUT} = 1.0 V, f_{SW} = 1 MHz, PSM, R_{OUT} = 0.5 Ω, L_O = 1 µH, C_O = 44 µF (22 µF x 2)

Startup



Shutdown



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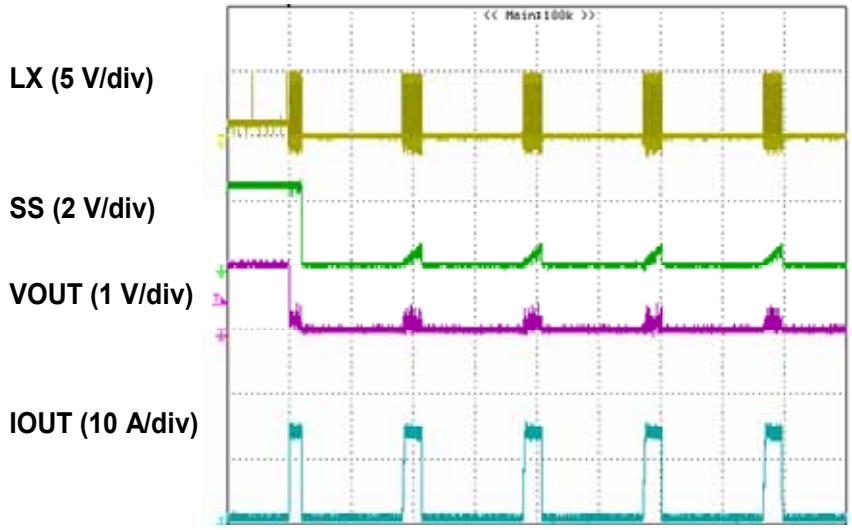
TYPICAL CHARACTERISTICS CURVES (Continued)

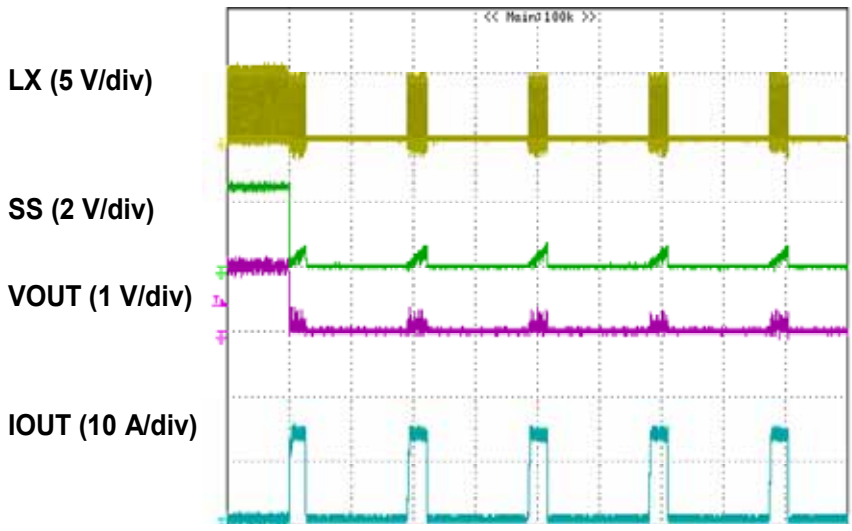
(7) Short Current Protection

Condition : V_{IN} = 5.0 V, V_{OUT} = 1.0 V, f_{SW} = 1 MHz, L_O = 1 µH, C_O = 44 µF (22 µF x 2)

PSM



FCCM



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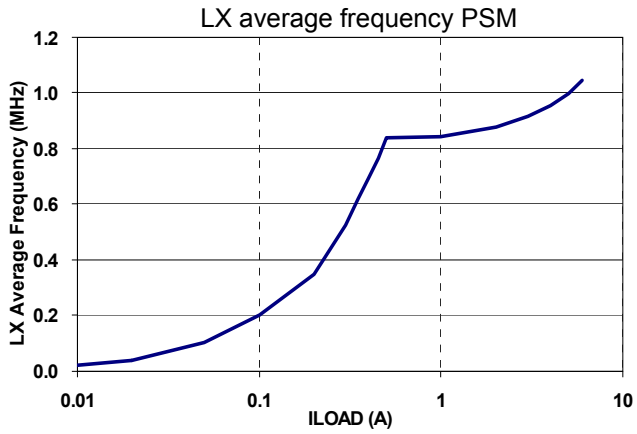
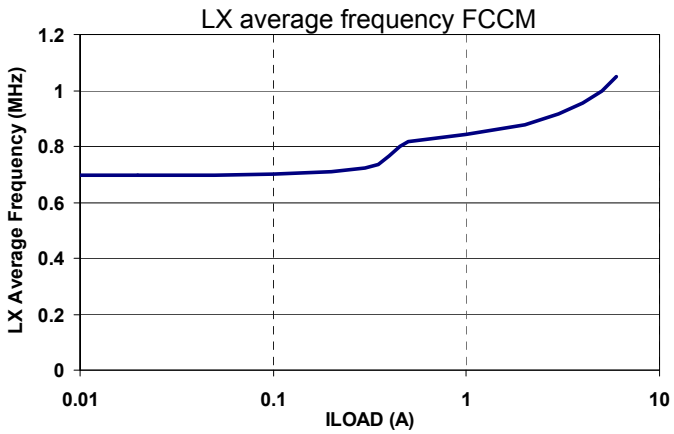
TYPICAL CHARACTERISTICS CURVES (Continued)

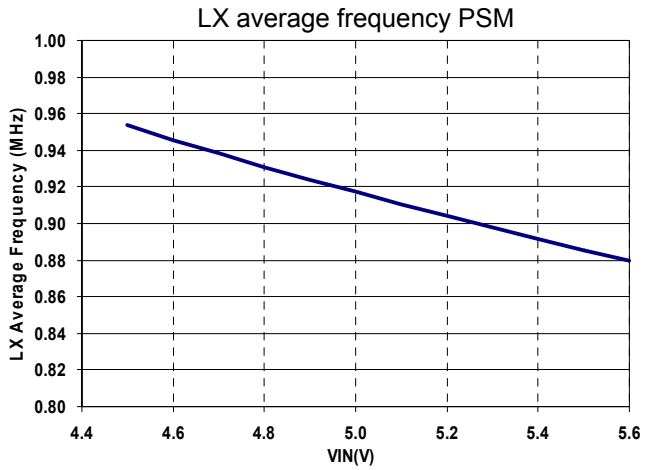
(8) Switching frequency

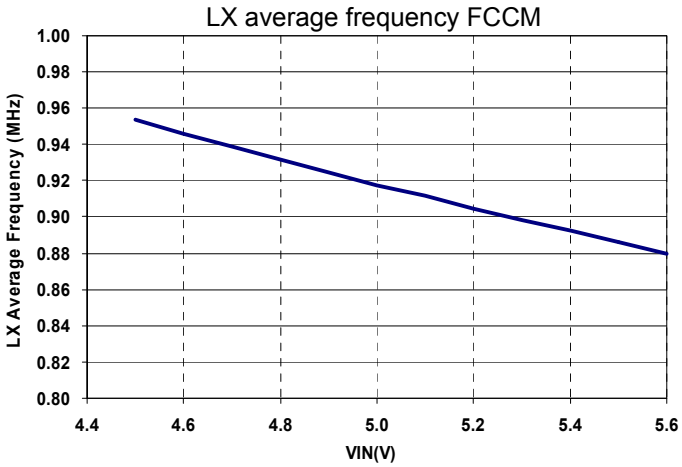
Condition : V_{IN} = 5.0 V, V_{OUT} = 1.0 V, f_{SW} = 1 MHz, I_{OUT} = 1 mA to 6 A, L_O = 1 µH, C_O = 44 µF (22 µF x 2)





Condition : V_{OUT} = 1.0 V, f_{SW} = 1 MHz, I_{OUT} = 3 A, L_O = 1 µH, C_O = 44 µF (22 µF x 2)





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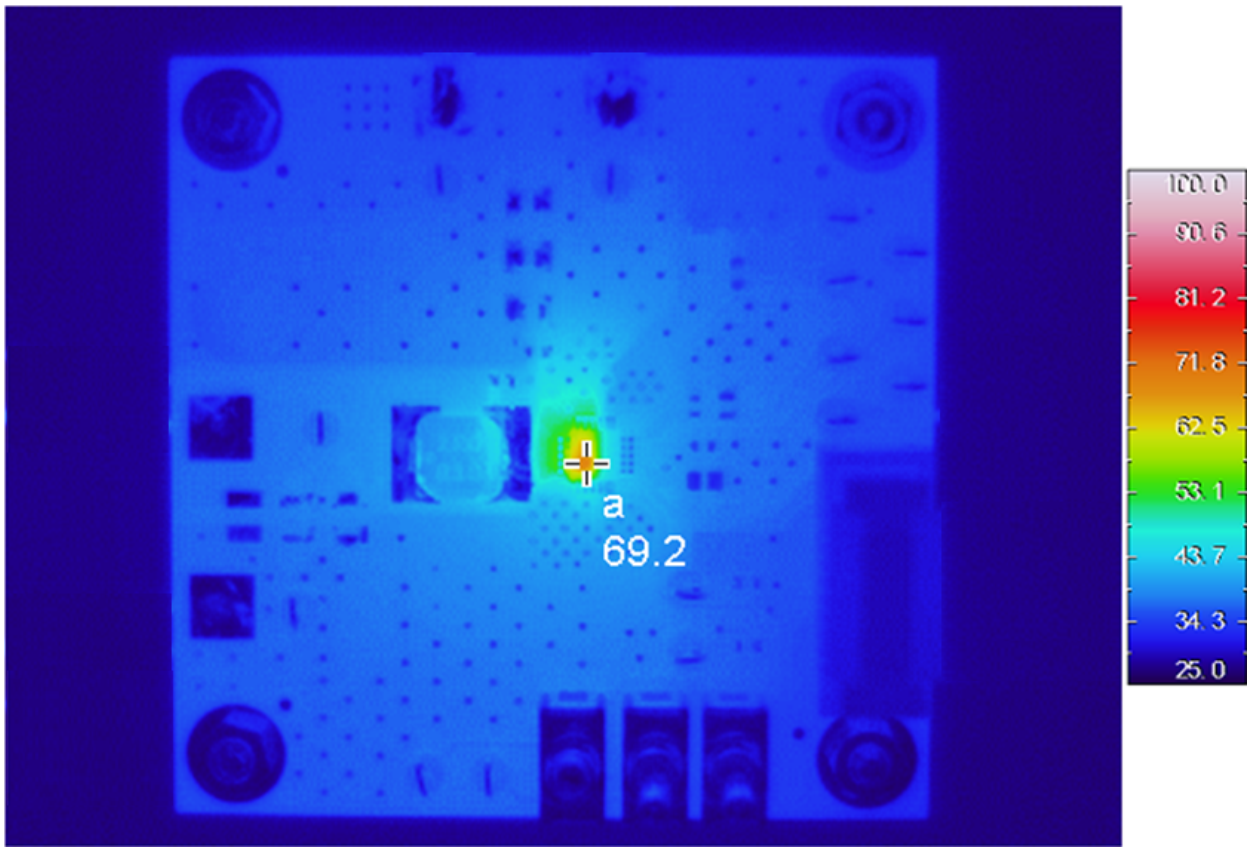
TYPICAL CHARACTERISTICS CURVES (Continued)

(9) Thermal performance

Condition : V_{IN} = 5.0 V, V_{OUT} = 1.0 V, f_{SW} = 1 MHz, I_{OUT} = 5 A, FCCM, L_O = 1 µH, C_O = 44 µF (22 µF x 2)



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APPLICATION INFORMATION

1. Evaluation Board Information

Condition : V_{OUT} Setting = 1.0 V, f_{SW} = 1 MHz, PSM

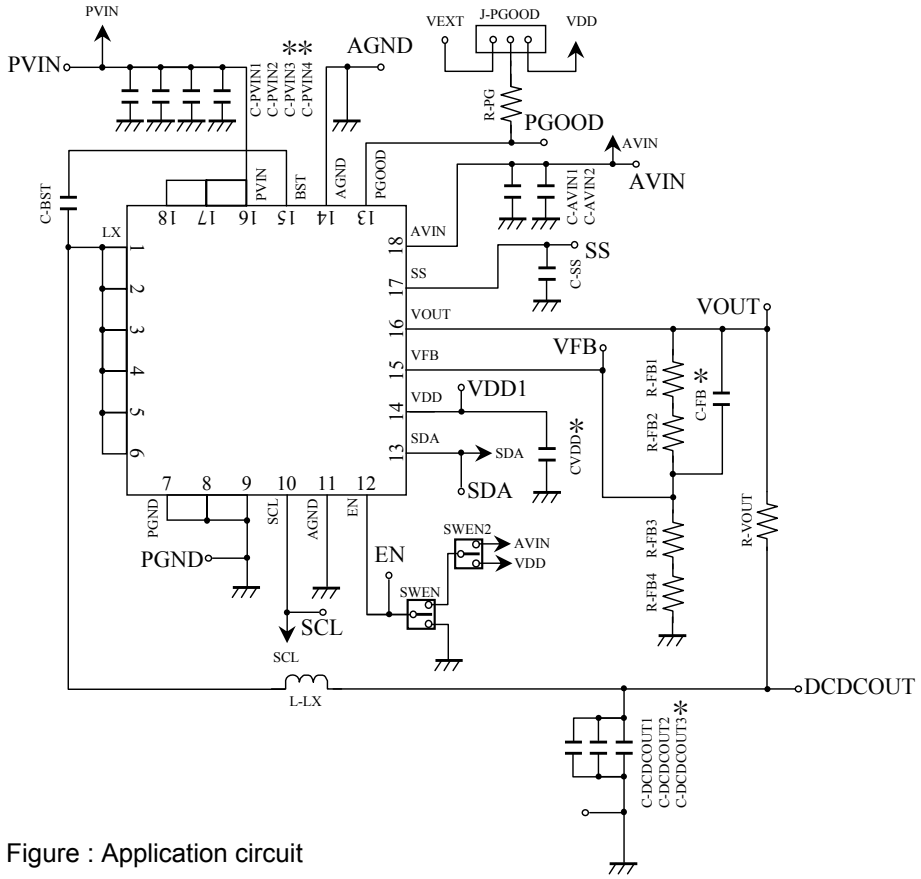

Figure : Application circuit

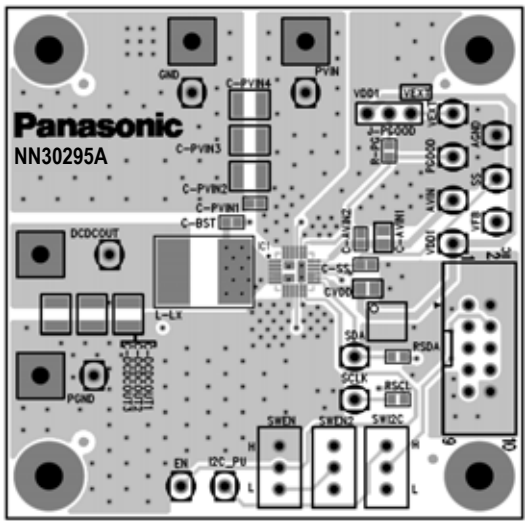

Figure : Top Layer with silk screen
(Top View) with Evaluation board

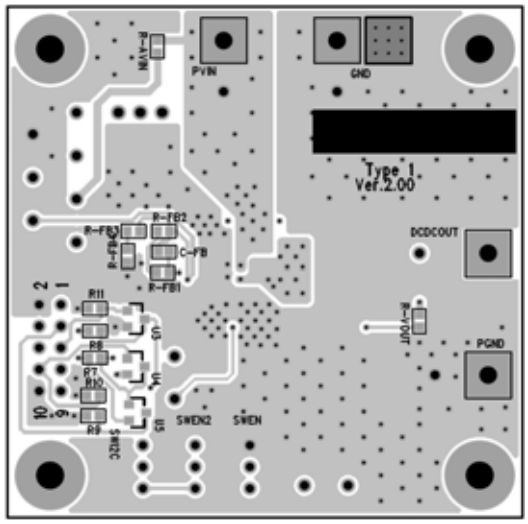

Figure : Bottom Layer with silk screen
(Bottom View) with Evaluation board

Note : The application circuit diagram and layout diagram explained in this section, should be used as reference examples. The operation of the mass production set is not guaranteed. Sufficient evaluation and verification is required in the design of the mass production set. The Customer is fully responsible for the incorporation of the above illustrated application circuit and the information attached with it, in the design of the equipment.

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APPLICATION INFORMATION (Continued)

2. Layout recommendations

Board layout considerations are necessary for stable operation of the DC-DC regulator. The following precautions must be used when designing the board layout.

(a) The Input capacitor C_{IN} must be placed in such a way that the distance between PVIN and PGND is minimum, in order to suppress the switching noise. Stray inductance and impedance should be reduced as indicated by loop (1) in the figure below.

(b) A single point ground connection (2) must be used to connect PGND and AGND to improve operation stability.

(c) Output current line I_{OUT} and the output sense line VOUT must have small common impedance to reduce output load variations. Output sense line VOUT must be close to the output condenser C_O as indicated by (3) below.

(d) Power Loss and output ripple voltage can be reduced by placing the inductor L_O and output capacitor C_O such that the stray inductance and the impedance of loop (4) is minimum. This is realized by :
  i) Minimizing distance between inductor L_O and LX pin.
  ii) Reducing distance between output capacitor C_O and (2) / (3)

(e) Thick lines in the application circuit example represent lines with large current flow. These lines should be designed as thick as possible.

(f) VFB / SS lines should be placed far away from LX line, BST line and inductor L_O to reduce the effects of switching noise. These lines should be designed as short as possible. This is especially true for the VFB line, which is a high impedance line.

(g) R_{FB1} / R_{FB2} should also be placed as far away as possible from LX line, BST line and inductor L_O to minimize the effects of switching noise. R_{FB1} / R_{FB2} should be placed close to the VFB pin.

(h) LX / BST lines are noisy lines. They should be designed as short as possible.

Note : The application circuit diagram and layout diagram explained in this section, should be used as reference examples. The operation of the mass production set is not guaranteed. Sufficient evaluation and verification is required in the design of the mass production set. The Customer is fully responsible for the incorporation of the above illustrated application circuit and the information attached with it, in the design of the equipment.

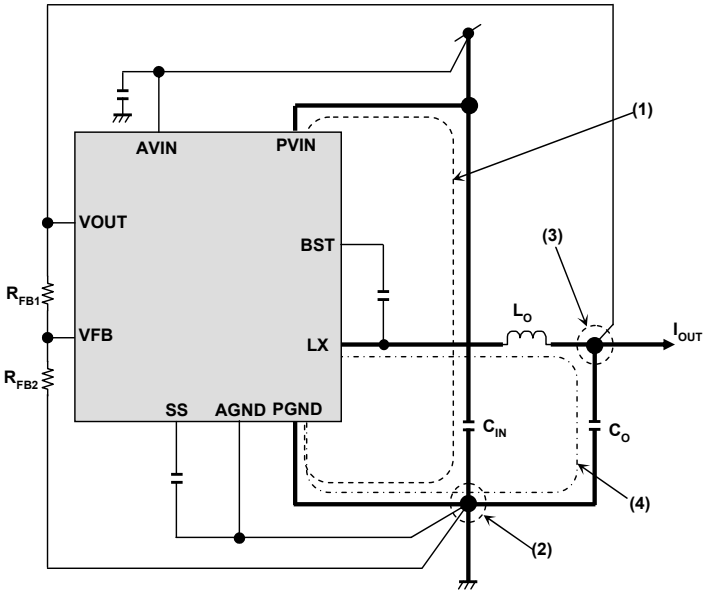

Figure : Application circuit diagram

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APPLICATION INFORMATION (Continued)

3. Recommended components

Reference Designator	QTY	Value	Manufacturer	Part Number
C-AVIN1	1	10 µF	Murata	GRM21BR71A106KE51L
C-AVIN2	1	0.1 µF	Murata	GRM188R72A104KA35L
C-BST	1	0.1 µF	Murata	GRM188R72A104KA35L
C-DCDCOUT	2	22 µF	Murata	GRM31CR71A226KE15L
C-PVIN1	1	0.1 µF	Murata	GRM188R72A104KA35L
C-PVIN2, C-PVIN3	2	22 µF	Murata	GRM31CR71A226KE15L
C-SS	1	10 nF	Murata	GRM188R72A103KA01L
L-LX	1	1.0 µH	Panasonic	ETQP3W1R0WFN
R-AVIN	1	0 Ω	Panasonic	ERJ3GEY0R00V
R-FB1, R-FB4 *1	2	0 Ω	Panasonic	ERJ3GEY0R00V
R-FB2 *1	1	1.0 kΩ	Panasonic	ERJ3EKF1001V
R-FB3 *1	1	1.5 kΩ	Panasonic	ERJ3EKF1501V
R-PG	1	100 kΩ	Panasonic	ERJ3EKF1003V

Note : *1 : The indicated values are for V_{OUT} = 1.0 V setting
For different VOUT setting, refer to the explanations in " OPERATION " section under " 2. Output Voltage Setting "

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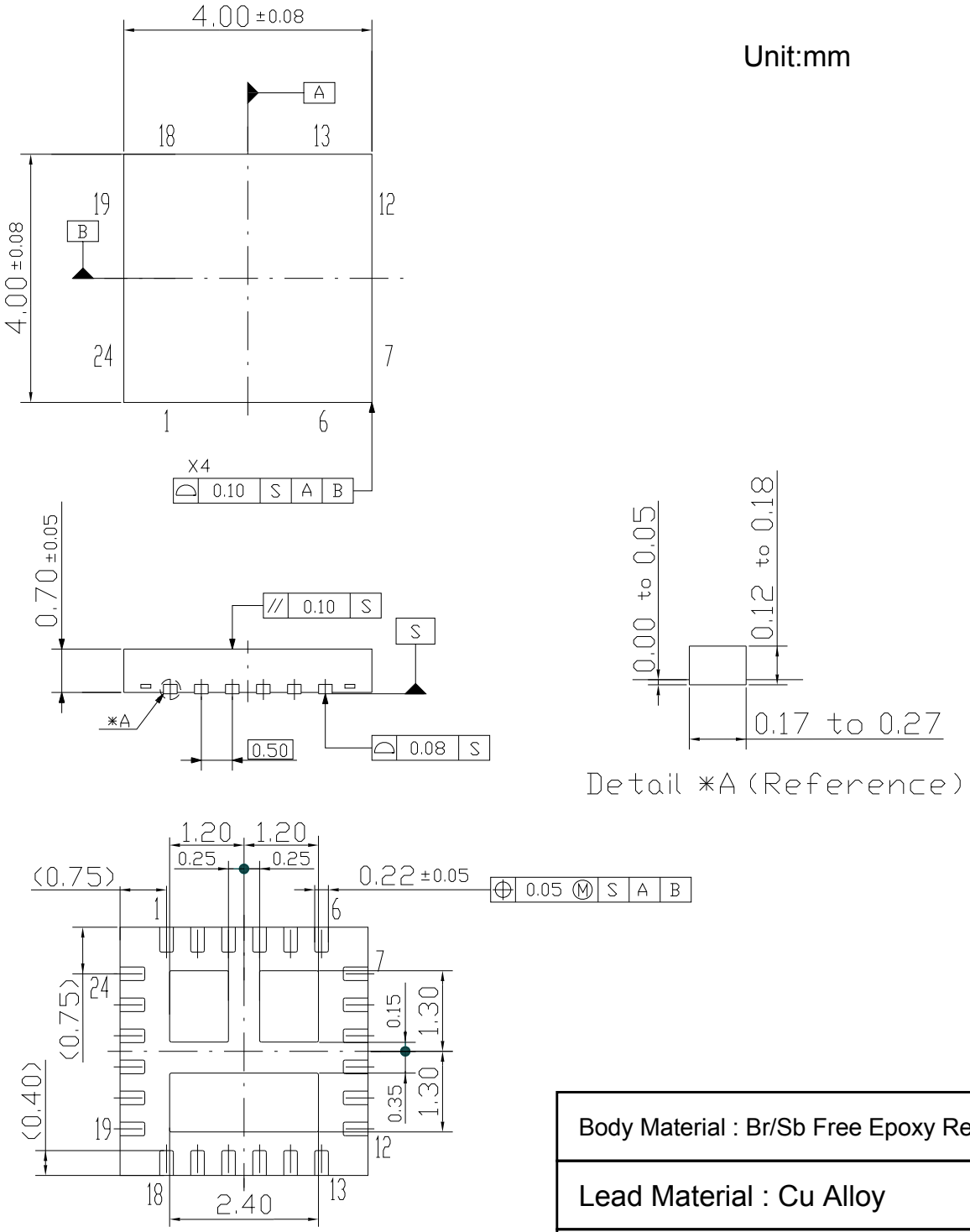
Panasonic NN30295A

PACKAGE INFORMATION

Outline Drawing

Package Code : HQFN024-A3-0404A

Unit:mm



Body Material : Br/Sb Free Epoxy Resin
Lead Material : Cu Alloy
Lead Finish Method : Pd Plating

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IMPORTANT NOTICE

1. When using the IC for new models, verify the safety including the long-term reliability for each product.
2. When the application system is designed by using this IC, please confirm the notes in this book.
   Please read the notes to descriptions and the usage notes in the book.
3. This IC is intended to be used for general electronic equipment.
   Consult our sales staff in advance for information on the following applications: Special applications in which exceptional quality and reliability are required, or if the failure or malfunction of this IC may directly jeopardize life or harm the human body.
   Any applications other than the standard applications intended.
   (1) Space appliance (such as artificial satellite, and rocket)
   (2) Traffic control equipment (such as for automotive, airplane, train, and ship)
   (3) Medical equipment for life support
   (4) Submarine transponder
   (5) Control equipment for power plant
   (6) Disaster prevention and security device
   (7) Weapon
   (8) Others : Applications of which reliability equivalent to (1) to (7) is required
   Our company shall not be held responsible for any damage incurred as a result of or in connection with the IC being used for any special application, unless our company agrees to the use of such special application.
   However, for the IC which we designate as products for automotive use, it is possible to be used for automotive.
4. This IC is neither designed nor intended for use in automotive applications or environments unless the IC is designated by our company to be used in automotive applications.
   Our company shall not be held responsible for any damage incurred by customers or any third party as a result of or in connection with the IC being used in automotive application, unless our company agrees to such application in this book.
5. Please use this IC in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Our company shall not be held responsible for any damage incurred as a result of our IC being used by our customers, not complying with the applicable laws and regulations.
6. Pay attention to the direction of the IC. When mounting it in the wrong direction onto the PCB (printed-circuit-board), it might be damaged.
7. Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins. In addition, refer to the Pin Description for the pin configuration.
8. Perform visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as solder-bridge between the pins of the IC. Also, perform full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the IC during transportation.
9. Take notice in the use of this IC that it might be damaged when an abnormal state occurs such as output pin-VCC short (Power supply fault), output pin-GND short (Ground fault), or output-to-output-pin short (load short). Safety measures such as installation of fuses are recommended because the extent of the above-mentioned damage will depend on the current capability of the power supply.
10. The protection circuit is for maintaining safety against abnormal operation. Therefore, the protection circuit should not work during normal operation.
    Especially for the thermal protection circuit, if the area of safe operation or the absolute maximum rating is momentarily exceeded due to output pin to VCC short (Power supply fault), or output pin to GND short (Ground fault), the IC might be damaged before the thermal protection circuit could operate.
11. Unless specified in the product specifications, make sure that negative voltage or excessive voltage are not applied to the pins because the IC might be damaged, which could happen due to negative voltage or excessive voltage generated during the ON and OFF timing when the inductive load of a motor coil or actuator coils of optical pick-up is being driven.
12. Product which has specified ASO (Area of Safe Operation) should be operated in ASO
13. Verify the risks which might be caused by the malfunctions of external components.
14. Connect the metallic plates (fins) on the back side of the IC with their respective potentials (AGND, PVIN, LX). The thermal resistance and the electrical characteristics are guaranteed only when the metallic plates (fins) are connected with their respective potentials.

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- Special applications (such as for airplanes, aerospace, automotive equipment, traffic signaling equipment, combustion equipment, life support systems and safety devices) in which exceptional quality and reliability are required, or if the failure or malfunction of the products may directly jeopardize life or harm the human body.

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(4) The products and product specifications described in this book are subject to change without notice for modification and/or improvement. At the final stage of your design, purchasing, or use of the products, therefore, ask for the most up-to-date Product Standards in advance to make sure that the latest specifications satisfy your requirements.

(5) When designing your equipment, comply with the range of absolute maximum rating and the guaranteed operating conditions (operating power supply voltage and operating environment etc.). Especially, please be careful not to exceed the range of absolute maximum rating on the transient state, such as power-on, power-off and mode-switching. Otherwise, we will not be liable for any defect which may arise later in your equipment.
Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damages, for example, by using the products.

(6) Comply with the instructions for use in order to prevent breakdown and characteristics change due to external factors (ESD, EOS, thermal stress and mechanical stress) at the time of handling, mounting or at customer's process. When using products for which damp-proof packing is required, satisfy the conditions, such as shelf life and the elapsed time since first opening the packages.

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