## **DMC5610M**

### Silicon NPN epitaxial planar type

For digital circuits

#### ■ Features

- ullet Low collector-emitter saturation voltage  $V_{\text{CE(sat)}}$
- Halogen-free / RoHS compliant
   (EU RoHS / UL-94 V-0 / MSL: Level 1 compliant)

#### ■ Marking Symbol: S2

#### ■ Basic Part Number

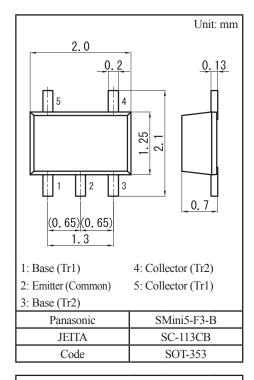
Dual DRC2123J (Common emitter)

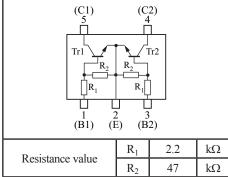
#### ■ Packaging

DMC5610M0R Embossed type (Thermo-compression sealing): 3 000 pcs / reel (standard)

#### ■ Absolute Maximum Ratings $T_a = 25$ °C

	Parameter	Symbol	Rating	Unit
Tr1 Tr2	Collector-base voltage (Emitter open)	V <sub>CBO</sub>	50	V
	Collector-emitter voltage (Base open)	V <sub>CEO</sub>	50	V
	Collector current	$I_{C}$	100	mA
Overall	Total power dissipation	P <sub>T</sub>	150	mW
	Junction temperature	T <sub>j</sub>	150	°C
	Operating ambient temperature	T <sub>opr</sub>	-40 to +85	°C
	Storage temperature	T <sub>stg</sub>	-55 to +150	°C



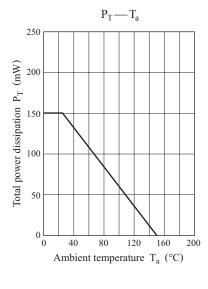


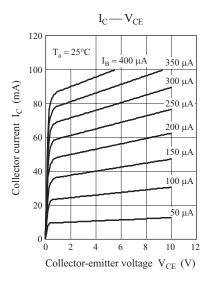
### ■ Electrical Characteristics $T_a = 25$ °C±3°C

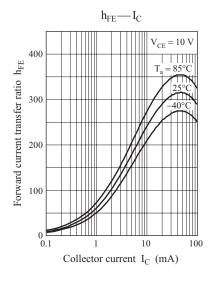
Parameter	Symbol	Conditions	Min	Тур	Max	Unit
Collector-base voltage (Emitter open)	V <sub>CBO</sub>	$I_C = 10 \mu A, I_E = 0$	50			V
Collector-emitter voltage (Base open)	V <sub>CEO</sub>	$I_{\rm C} = 2 \text{ mA}, I_{\rm B} = 0$	50			V
Collector-base cutoff current (Emitter open)	$I_{CBO}$	$V_{CB} = 50 \text{ V}, I_{E} = 0$			0.1	μΑ
Collector-emitter cutoff current (Base open)	I <sub>CEO</sub>	$V_{CE} = 50 \text{ V}, I_{B} = 0$			0.5	μΑ
Emitter-base cutoff current (Collector open)	$I_{EBO}$	$V_{EB} = 6 \text{ V}, I_C = 0$			0.2	mA
Forward current transfer ratio	$h_{FE}$	$V_{CE} = 10 \text{ V}, I_{C} = 5 \text{ mA}$	80			_
h <sub>FE</sub> ratio *1	h <sub>FE</sub> (Small/Large)	$V_{CE} = 10 \text{ V}, I_{C} = 5 \text{ mA}$	0.50	0.99		_
Collector-emitter saturation voltage	V <sub>CE(sat)</sub>	$I_C = 10 \text{ mA}, I_B = 0.5 \text{ mA}$			0.25	V
Input voltage (ON)	V <sub>I(on)</sub>	$V_{CE} = 0.2 \text{ V}, I_{C} = 5 \text{ mA}$	1.2			V
Input voltage (OFF)	V <sub>I(off)</sub>	$V_{CE} = 5 \text{ V}, I_{C} = 100 \mu\text{A}$			0.4	V
Input resistance	$R_1$		-30%	2.2	+30%	kΩ
Resistance ratio	$R_1/R_2$		0.037	0.047	0.057	_

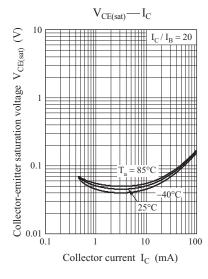
Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

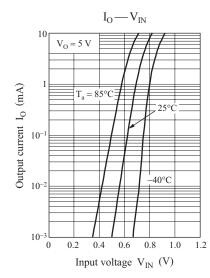
2. \*1: Ratio between 2 elements

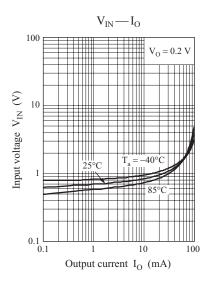








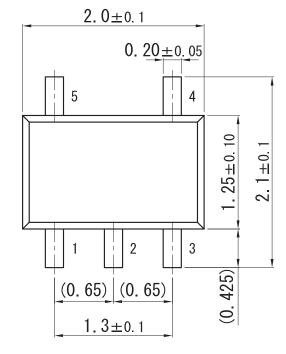


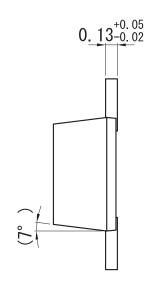


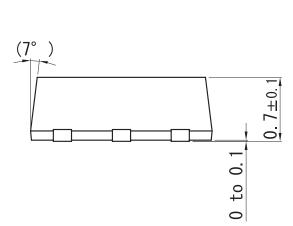
Ver. DED 2

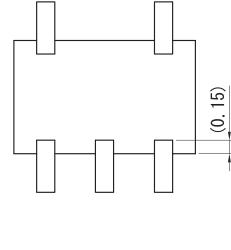
## SMini5-F3-B

Unit: mm

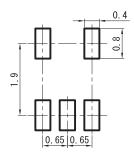








#### ■ Land Pattern (Reference) (Unit: mm)



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