

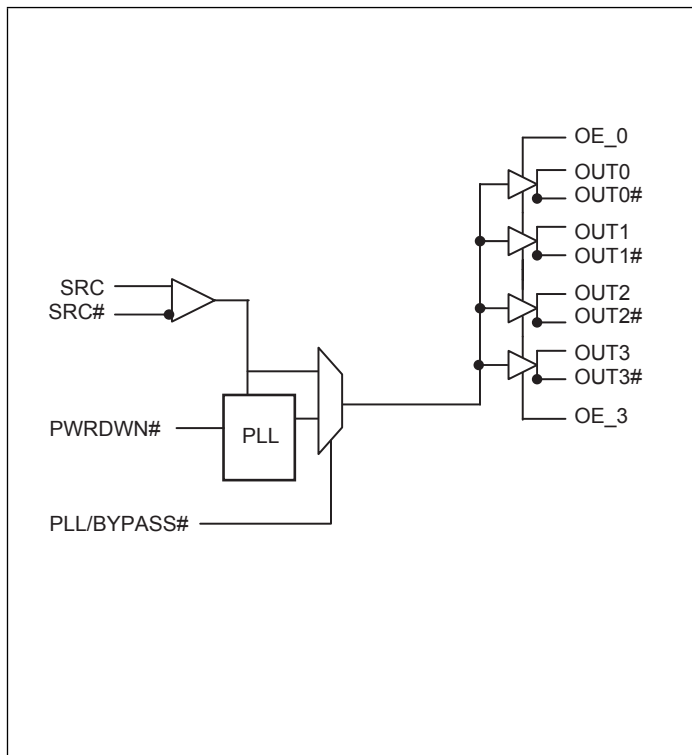
### Features

- Phase jitter filter for PCIe® 2.0 application
- Four pairs of HCSL PCIe 2.0 Differential Clocks
- Prop delay  $< \pm 250\text{ps}$  (in PLL mode)
- Low skew  $< 50\text{ps}$
- Low jitter  $< 50\text{ps}$  cycle-to-cycle
- $< 1\text{ps}$  additive RMS phase jitter
- 100 MHz PLL Mode operation
- 3.3V operation
- Packaging (Pb-free and Green):
  - 20-Pin 4.0mm x 4.0mm x0.75mm TQFN (ZD20)

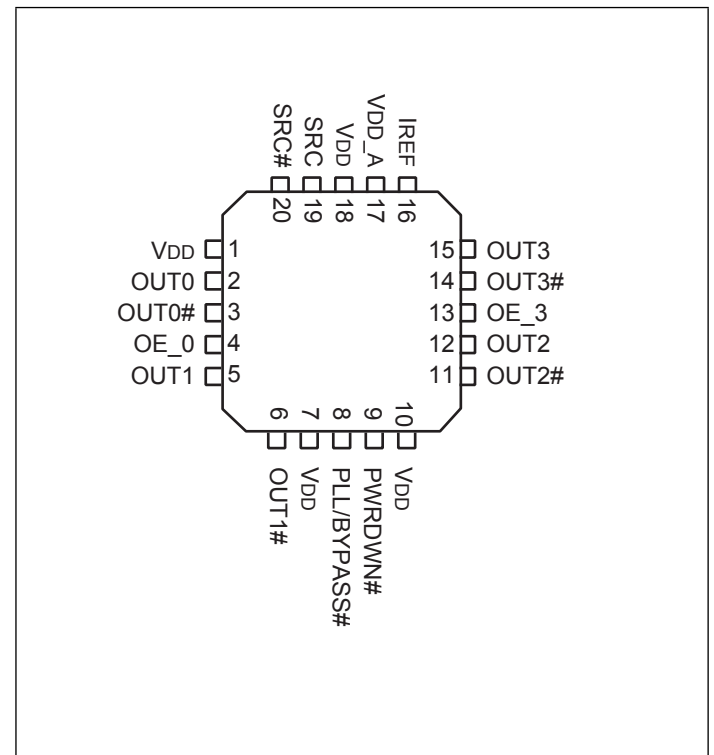
### Description

Pericom Semiconductor's PI6PCIEB24 is a PCI Express® (PCIe) 2.0 compliant high-speed, low-noise differential clock buffer. The device distributes the input differential PCIe clock to four differential pairs of clock outputs with zero delay PLL.

### Block Diagram



### Pin Configuration



**Pin Descriptions**

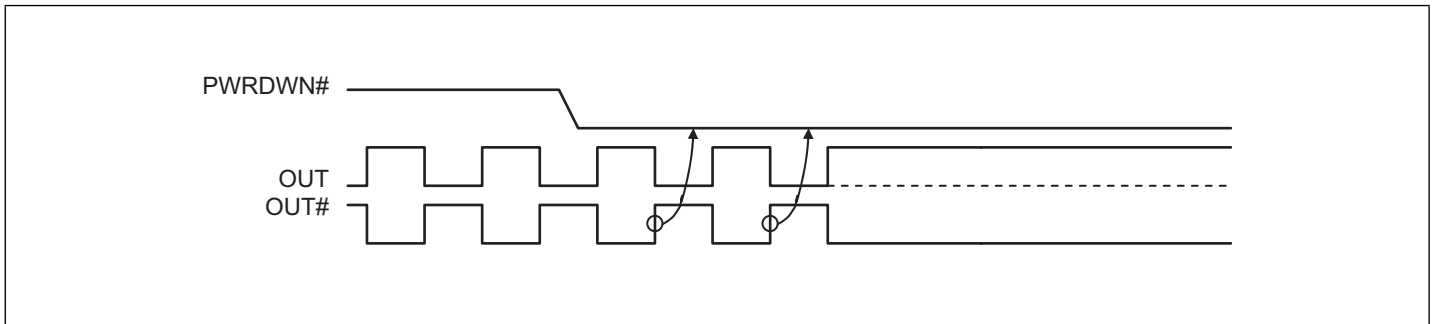
| Pin Name             | Type   | Pin No                     | Description                                                         |
|----------------------|--------|----------------------------|---------------------------------------------------------------------|
| SRC & SRC#           | Input  | 19, 20                     | 0.7V Differential SRC input from PI6C410 clock synthesizer          |
| OUT[0:3] & OUT[0:3]# | Output | 2, 3, 5, 6, 12, 11, 15, 14 | 0.7V Differential outputs                                           |
| IREF                 | Input  | 16                         | External resistor connection to set the differential output current |
| V <sub>DD</sub>      | Power  | 1, 7, 10, 18               | 3.3V Power Supply for Outputs                                       |
| PWRDWN#              | Input  | 9                          | 3.3V LVTTTL active LOW input for power down operation               |
| VDD_A                | Power  | 17                         | 3.3V Power Supply for PLL                                           |
| PLL/BYPASS#          | Input  | 8                          | When HIGH, PLL is enabled, When LOW, PLL is bypassed.               |
| OE_0, OE_3           | Input  | 4, 13                      | When HIGH, enables corresponding OUT0, OUT3 respectively.           |

Ground connection is through the package metal plate underneath.

**Functionality**

| PWRDWN# | OUT                | OUT#   |
|---------|--------------------|--------|
| 1       | Normal             | Normal |
| 0       | $I_{REF} \times 2$ | Low    |

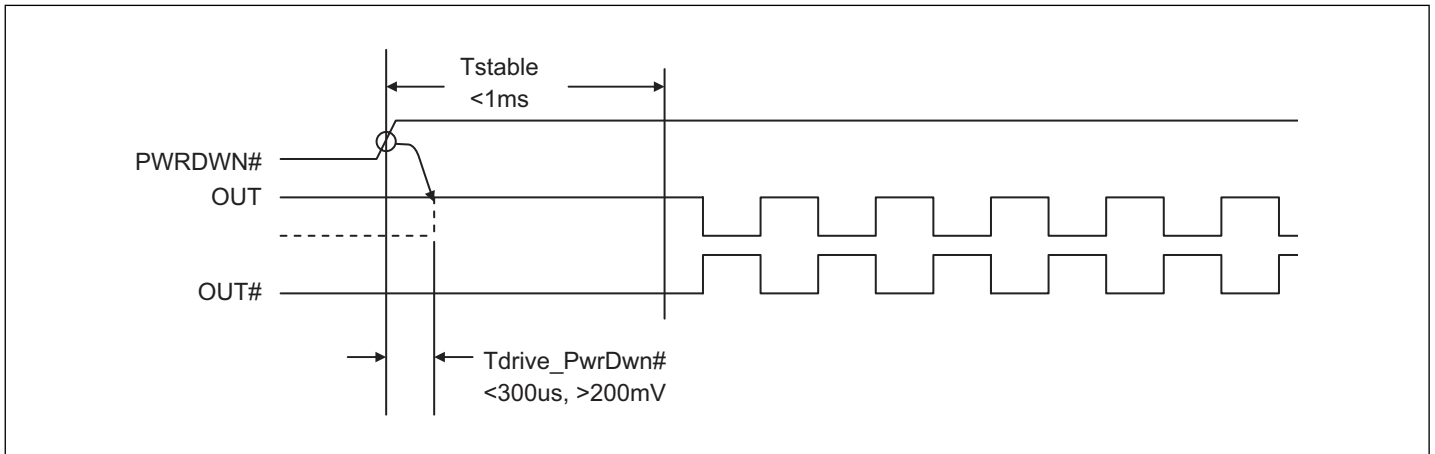
**Power Down (PWRDWN# assertion)**



**Figure 1. Power down sequence**

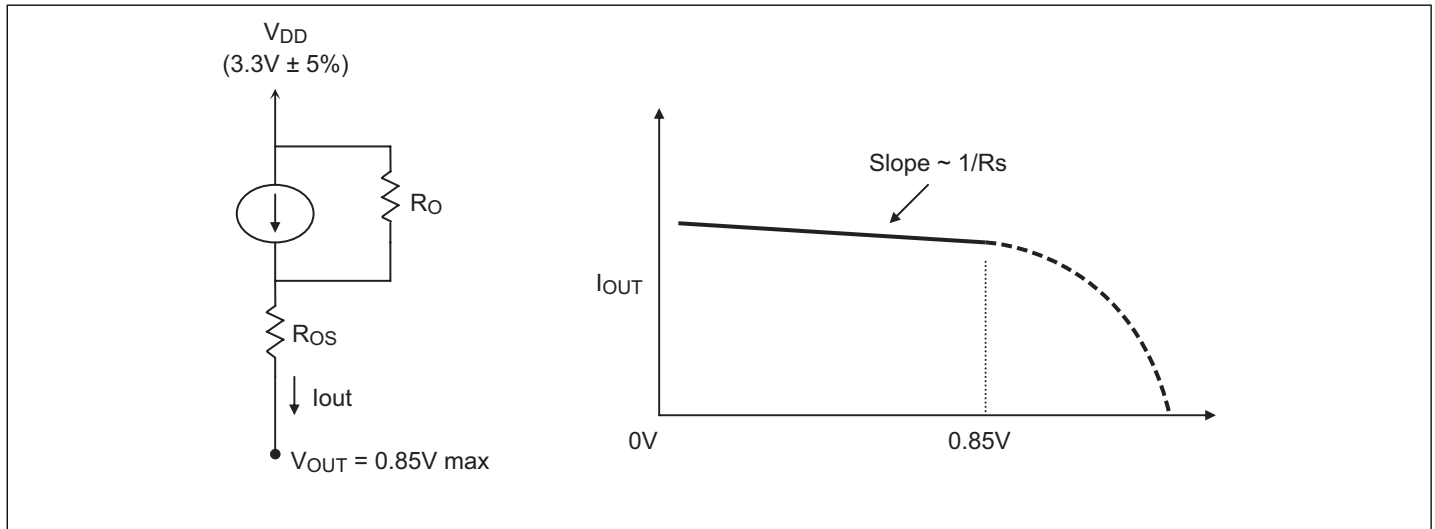
When PWRDWN# is asserted (Low),  $2xI_{REF}$  current flows through OUT pin.

**Power Down (PWRDWN# De-assertion)**



**Figure 2. Power down de-assert sequence**

**Current-mode output buffer characteristics of OUT[0:3], OUT[0:3]#**



**Figure 2. Simplified diagram of current-mode output buffer**

**Differential Clock Buffer characteristics**

| Symbol | Minimum     | Maximum     |
|--------|-------------|-------------|
| RO     | 3000Ω       | N/A         |
| ROS    | unspecified | unspecified |
| VOUT   | N/A         | 850mV       |

**Current Accuracy**

| Symbol | Conditions     | Configuration                   | Load                                      | Min.          | Max.          |
|--------|----------------|---------------------------------|-------------------------------------------|---------------|---------------|
| IOUT   | VDD = 3.30 ±5% | RREF = 475Ω 1%<br>IREF = 2.32mA | Nominal test load for given configuration | -12% INOMINAL | +12% INOMINAL |

INOMINAL refers to the expected current based on the configuration of the device.

**Differential Clock Output Current**

| Board Target Trace/Term Z                        | Reference R, Iref = VDD/(3xRr)   | Output Current | VOH @ Z   |
|--------------------------------------------------|----------------------------------|----------------|-----------|
| 100Ω<br>(100Ω differential ≈ 15% coupling ratio) | RREF = 475Ω 1%,<br>IREF = 2.32mA | IOH = 6 x IREF | 0.7V @ 50 |

**Absolute Maximum Ratings** (Over operating free-air temperature range)

| Symbol            | Parameters               | Min. | Max. | Units |
|-------------------|--------------------------|------|------|-------|
| V <sub>DD_A</sub> | 3.3V Core Supply Voltage | -0.5 | 4.6  | V     |
| V <sub>DD</sub>   | 3.3V I/O Supply Voltage  | -0.5 | 4.6  |       |
| V <sub>IH</sub>   | Input High Voltage       |      | 4.6  |       |
| V <sub>IL</sub>   | Input Low Voltage        | -0.5 |      |       |
| T <sub>s</sub>    | Storage Temperature      | -65  | 150  | °C    |
| V <sub>ESD</sub>  | ESD Protection           | 2000 |      | V     |

Stress beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device.

**DC Electrical Characteristics** (V<sub>DD</sub> = 3.3±5%, V<sub>DD\_A</sub> = 3.3±5%)

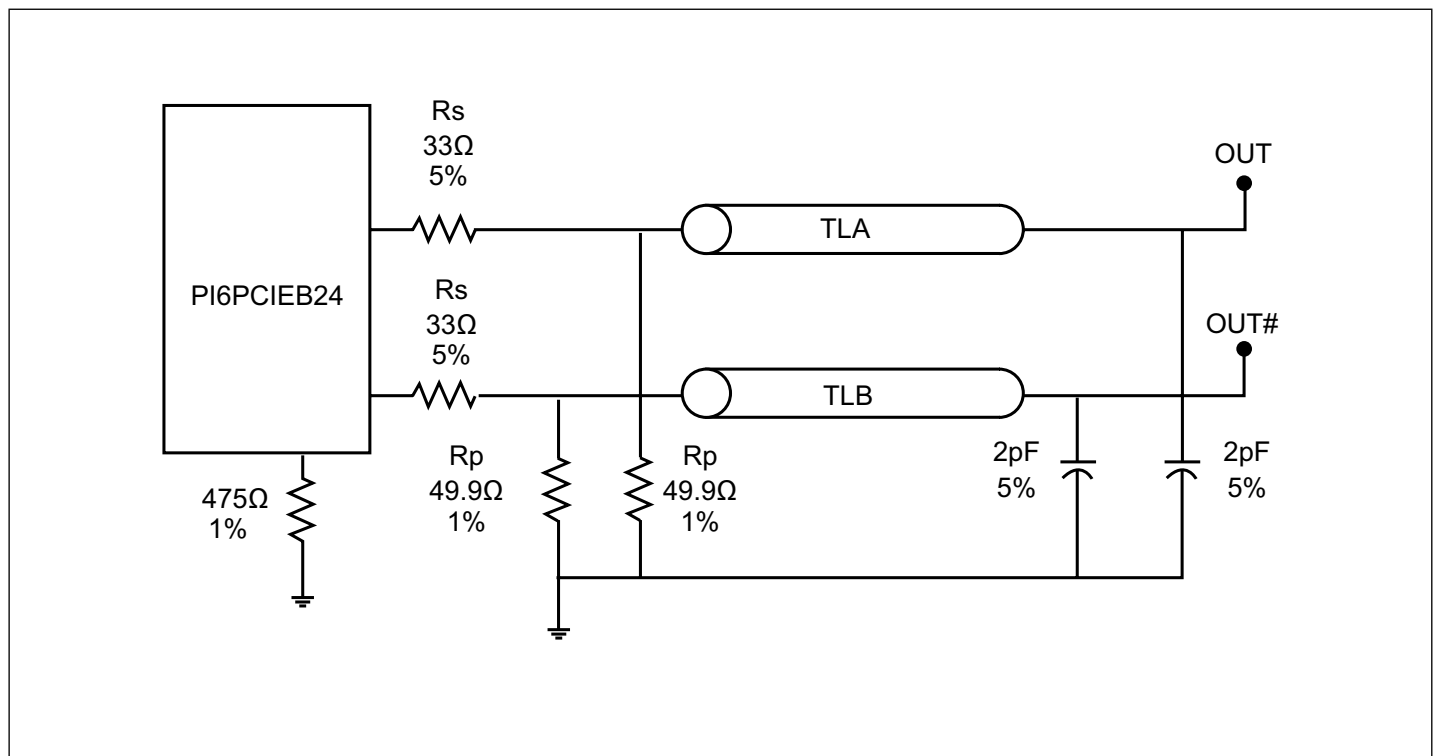
| Symbol            | Parameters               | Condition                                                             | Min.                  | Max.                  | Units |
|-------------------|--------------------------|-----------------------------------------------------------------------|-----------------------|-----------------------|-------|
| V <sub>DD_A</sub> | 3.3V Core Supply Voltage |                                                                       | 3.135                 | 3.465                 | V     |
| V <sub>DD</sub>   | 3.3V I/O Supply Voltage  |                                                                       | 3.135                 | 3.465                 |       |
| V <sub>IH</sub>   | 3.3V Input High Voltage  | V <sub>DD</sub>                                                       | 2.0                   | V <sub>DD</sub> + 0.3 |       |
| V <sub>IL</sub>   | 3.3V Input Low Voltage   |                                                                       | V <sub>SS</sub> - 0.3 | 0.8                   |       |
| I <sub>IK</sub>   | Input Leakage Current    | 0 < V <sub>IN</sub> < V <sub>DD</sub>                                 | -5                    | +5                    | μA    |
| I <sub>OH</sub>   | Output High Current      | I <sub>OH</sub> = 6 x I <sub>REF</sub> ,<br>I <sub>REF</sub> = 2.32mA | 12.2                  | 15.6                  | mA    |
| C <sub>IN</sub>   | Input Pin Capacitance    |                                                                       | 3                     | 5                     | pF    |
| C <sub>OUT</sub>  | Output Pin Capacitance   |                                                                       |                       | 6                     |       |
| LPIN              | Pin Inductance           |                                                                       |                       | 7                     | nH    |
| I <sub>DD</sub>   | Power Supply Current     | V <sub>DD</sub> = 3.465V, F <sub>CPU</sub> = 100MHz                   |                       | 200                   | mA    |
| I <sub>SS</sub>   | Power Down Current       | Driven outputs                                                        |                       | 40                    |       |
| T <sub>A</sub>    | Ambient Temperature      |                                                                       | -45                   | 85                    | °C    |

**AC Switching Characteristics** ( $V_{DD} = 3.3 \pm 5\%$ ,  $V_{DD\_A} = 3.3 \pm 5\%$ )

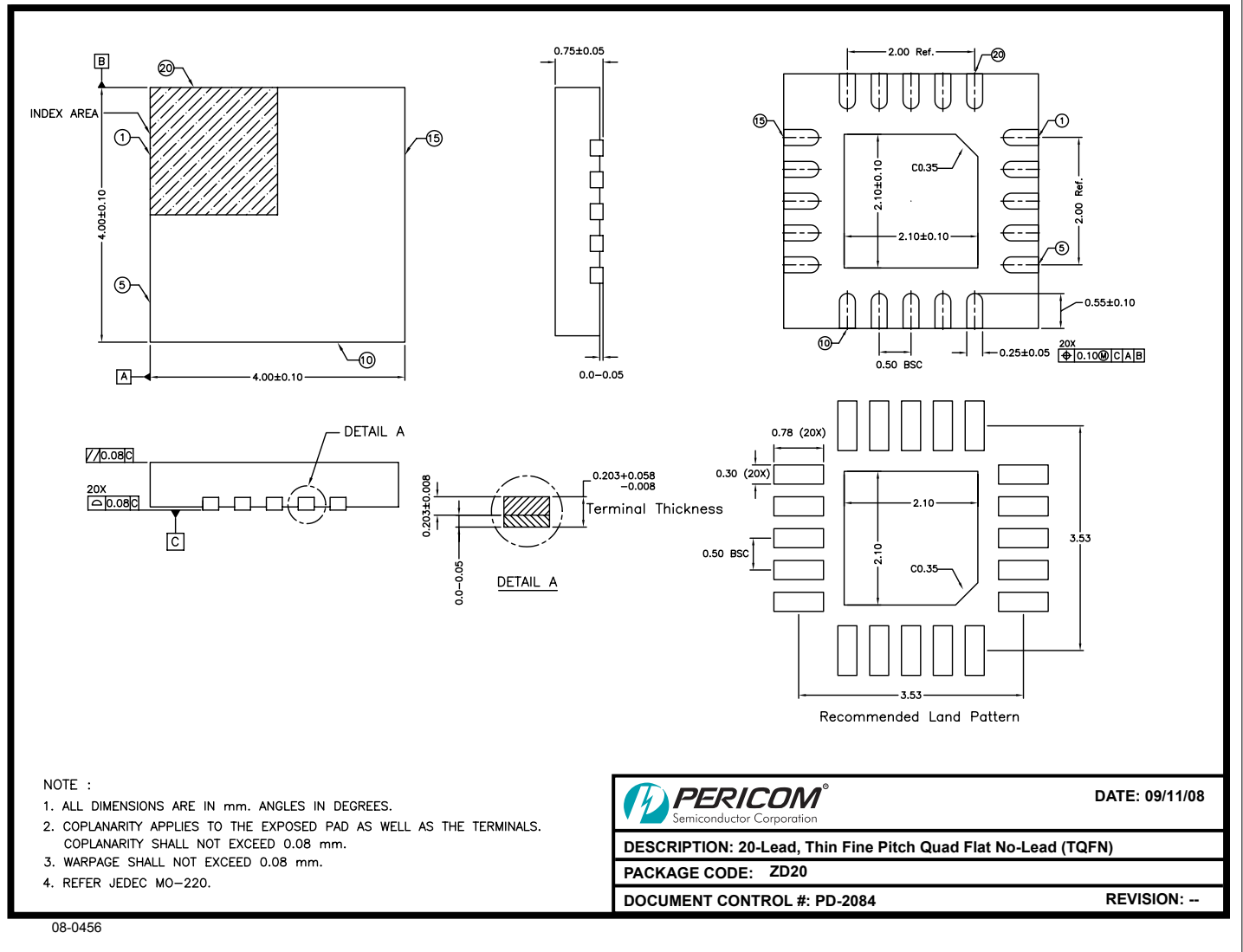
| Symbol                  | Parameters                                             | Min  | Max.      | Units | Notes |
|-------------------------|--------------------------------------------------------|------|-----------|-------|-------|
| $F_{IN}$                |                                                        | 95   | 105       | MHz   |       |
| $T_{rise} / T_{fall}$   | Rise and Fall Time (measured between 0.175V to 0.525V) | 175  | 700       | ps    | 2     |
| $DT_{rise} / DT_{fall}$ | Rise and Fall Time Variation                           |      | 125       | ps    | 2     |
|                         | Rise/Fall Matching                                     |      | 20        | %     | 2     |
| $T_{pd}$                | PLL Mode (PLL/BYPASS# = 1)                             |      | $\pm 250$ | ps    |       |
| $T_{jitter}$            | Cycle - Cycle Jitter                                   |      | 50        | ps    | 3, 4  |
| $V_{HIGH}$              | Voltage High including overshoot                       | 660  | 1150      | mV    | 2     |
| $V_{LOW}$               | Voltage Low including undershoot                       | -300 |           | mV    | 2     |
| $V_{cross}$             | Absolute crossing point voltages                       | 250  | 550       | mV    | 2     |
| $\Delta V_{cross}$      | Total Variation of $V_{cross}$ over all edges          |      | 140       | mV    | 2     |
| $T_{DC}$                | Duty Cycle                                             | 45   | 55        | %     | 3     |
| $T_{jadd}$              | Additive RMS phase jitter for PCIe GenII               | <0   | 1         | ps    | 5     |
| $T_{pd}(bypass)$        | Bypass mode (PLL/BYPASS# = 0)                          | 2.5  | 6.5       | ns    |       |

1. Test configuration is  $R_s = 33.2\Omega$ ,  $R_p = 49.9\Omega$ , and 2pF.
2. Measurement taken from Single Ended waveform.
3. Measurement taken from Differential waveform.
4. Measurement taken using M1 data capture analysis tool.
5. Additive jitter is calculated from input and output RMS phase jitter using PCIe 2.0 filter by  $T_{jadd} = \sqrt{(\text{output jitter})^2 - (\text{input jitter})^2}$

**Configuration Test Load Board Termination**



**Packaging Mechanical: 20-Pin TQFN (ZD)**



**Ordering Information<sup>(1-3)</sup>**

| Ordering Code | Package Code | Package Description                            |
|---------------|--------------|------------------------------------------------|
| PI6PCIEB24ZDE | ZD           | 20-pin, 4.0mm x 4.0mm, TQFN, Pb-Free and Green |

1. Thermal characteristics can be found on the company web site at [www.pericom.com/packaging/](http://www.pericom.com/packaging/)
2. E = Pb-free and Green
3. Adding an X suffix = Tape/Reel